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P1.44: Test-beam timing characterisation of monolithic pixel sensors produced in modified CMOS imaging processes

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Several advanced silicon pixel-detector technologies are under study within the strategic R&D programme on technologies for future experiments pursued by CERN's Experimental Physics department (EP R&D), reaching excellent spatial (1-4 μm) and sub-nanosecond temporal resolution.

FASTPIX is a monolithic pixel sensor demonstrator targeting sub-nanosecond timing precision and is designed in a modified 180 nm imaging process. It contains 32 mini-matrices with 68 hexagonal pixels each, with a pixel pitch ranging from 8.6 μm to 20 μm and differing in sensor design features. 4 pixels provide an analogue signal, while the other 64 pixels are connected to the digital readout.

The Digital Pixel Test Structure (DPTS) is a prototype monolithic pixel sensor fabricated in a 65 nm CMOS technology and aims to demonstrate the feasibility of using a 65 nm process in a monolithic sensor while testing custom digital cells and a new digital readout scheme. It is the most complex design on the first 65 nm test production run by EP R&D with a full sensor, analog front-end and digital readout. It consists of 32x32 square pixels with 15 μm pitch. The design and testing was part of a larger effort in EP R&D and the ALICE collaboration.

Both FASTPIX and DPTS utilise an asynchronous digital encoding of hit position, Time over Threshold, and Time of Arrival on one (DPTS) or three (FASTPIX) differential channels, which are read out using a fast oscilloscope or a custom time to digital converter on the FPGA of the readout system.

The characterisation of FASTPIX and DPTS devices was performed in the CLICdp Timepix3 telescope at CERN SPS, which was extended with a microchannel plate photomultiplier tube (MCP-PMT) as a precise timing reference with a resolution of better than 10 ps.

For FASTPIX, a time resolution between 100 ps and 200 ps after time-walk correction is obtained depending on the pixel pitch and sensor design parameters. The operating point of the DPTS was optimised to reach a sub-nanosecond time resolution after time-walk correction. This contribution introduces the monolithic FASTPIX and DPTS chips and presents the timing measurements and results.

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