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P1.72: 50.3ps time resolution and an 11-channel time measuring chip for Topmetal detectors

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Pixel detectors are widely used in the inner tracking detectors of high-energy physics experiments due to their superior position resolution. With the development of detector systems, pixel detectors and associated readout electronics are required to conduct high-precision time measurements along with positions.
This paper aims to elaborate on a new front-end ASIC design to expand Topmetal pixel detectors for time measurement. The front-end circuit for each pixel mainly consists of two reverse delay chains and 11 edge acquisition circuits. The inverter is used as the base unit of the delay chain to effectively increase the transmission bandwidth, and the acquisition circuit uses two reverse clocks to generate 22 sets of time-stamped signals. The position and time information of the hit pixels is obtained by the time difference between the two ends of the delay chain. The function of time measurement based on time interpolation is achieved by TDC, which includes Time-to-Amplitude Converter (TAC), analog gate, weight count module, and Wilkinson Analog-to-Digital Converter (ADC). Coarse time measurement is implemented based on an 8-bit counter with a working frequency of 500 MHz, and fine time measurement is achieved by the combination of TAC and ADC. The TAC converts the time difference values into voltages which are stored in a capacitor. Multiple voltage signals are sampled sequentially via an analog selector. The ADC consists of a ramp generator, a comparator, and a 10-bit Gray code counter. The corresponding time difference values are obtained via the coarse and fine counters.
The design prototype was taped out with the GSMCR130 nm technology. Test results show that this circuit can handle up to 11 consecutive cases, with the minimum time interval of adjacent cases being 500 ps, the bin size up to 2 ps, and Differential Non-Linearity (DNL) is between -0.8 to +1.4 LSB. The time measurement accuracy is better than 50.24 ps RMS, and the PVT robustness of the input delay chain circuit is validated, showing the stable performance of the design.

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