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P2.17: Enhanced Readout System for Timepix3 Detectors in Large-Scale Scientific Facilities

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The Timepix3 ASIC readout chip [1] has already proven great results and benefits for a lot of projects [2, 3, 4]. It was used as a radiation monitor in the ATLAS Experiment (CERN) [5, 6], its good performance in various low-power modes [7] was also demonstrated. However, the utilization of a higher number (well synchronized) of Timepix3 detectors in environments with large research infrastructures (typically accelerators) is still challenging. We developed a novel readout system dedicated to applications where high data rates, long distances, and harsh radiation fields are expected.

The presented system deals with all aspects of the modern measurement chain (see Figure 1) –from hardened chipboard to fast data transfer to computer. The system consists of several fundamental elements: Chipboards, Data Concentrator, Back-End unit and computer/server.

Dual-stack (a pair of Timepix3 detectors) chipboard carries a pair of Timepix3 detectors. It ensures very stable power supplies for readout ASICs by means of radiation hardened voltage regulators. The housing was designed with high emphasis on good heat dissipation, which is important for the thermal stability of sensors.

Data concentrator unit (DC; front-end) controls up to three chipboards (6 pieces of Timepix3 detectors) via a metallic (cable) connection. The unit accumulates pixel data and translates it into two common data streams that are sent to Back-End unit by means of two 10 Gbps fiber connections. Apart from this data accumulation/translation functionality, the data concentrator also implements three independent power supplies for chipboards and high-voltage bias sources with a range of 25 V –500 V in both polarities; leakage current measurement is included as well.

In the final stage, data are received by the Back-End unit (BE). This device implements the main functionality (DC implements only data transfers) of the readout system. It produces configuration streams for detectors, controls internal DACs, sets bias, etc. Fundamental data processing is implemented directly in the FPGA. Back-End unit is controlled via a 1G Ethernet interface. However, due to high data rates, the PCI Express Gen3 4x interface is used as the main data channel into the computer or server (although the user can also use Ethernet for data acquisition).

The system's designed architecture makes it possible to use it in a radiation field. The chipboard consists only of the Timepix3 ASIC and power supplies; no radiation-sensitive components are used. The Data Concentrator uses more complex and sensitive components, making it more susceptible to upsets caused by radiation. However, Data Concentrator can be placed up to 20 meters away from chipboards, which can decrease the expected dose and reduce the probability of failure. Flash-based FPGA devices also increase hardness. The most sensitive element of the system - Back-End unit –should be placed in a safe area because it is based on commercial components. However, due to fiber connectivity, the distance between Data Concentrator and Back-End is almost unlimited (hundreds of meters are considered in real applications).

The system is designed to be able to process a high data rate. Each of the chipboards can produce up to 2x40 Mhit/s, which corresponds to a pure data rate of over 12 Gbps between the Data Concentrator and Back-End unit. This is why a pair of 10 Gbps fibers is used. Final data transfer to the computer is implemented as a PCI Express Gen3 4x interface featuring a rate up to 3.5 GB/s. The chain can also offer precise and uniform timing over the whole system by means of clock shift measurements in individual nodes.

[1] T. Poikela et al., 2014 JINST 9 C05013.
[2] X. Wu et al., Advances in Space Research, 63 (2019), Issue 8, pp 2672-2682.

[3] Bergmann, B., Jelínek, J.: Measurement of the 212Po, 214Po and 212Pb half-life time with Timepix3. Eur. Phys. J. A 58, 106 (2022). https://doi.org/10.1140/epja/s10050-022-00757-z

[4] P. Burian et al., 2018 JINST 13 C01002 .

[5] P. Burian et al., 2018 JINST 13 C11024.

[6] B. Bergmann et al., 2020 JINST 15 C01039.

[7] P. Burian et al., 2019 JINST 14 C01001.

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