Contribution ID: **84** Type: **Poster**

P1.71: A 12x16-Gbps/ch VCSEL array driving ASIC in 130-nm SiGe BiCMOS for heavy-ion physics experiments

Monday, 26 June 2023 16:02 (1 minute)

The Heavy Ion Research Facility at Lanzhou (HIRFL) and the High-Intensity heavy-ion Accelerator Facility (HIAF) are the leading heavy-ion physics centers. Since the scale of experiments at HIRFL and HIAF are significantly increased, the High-speed and the high-density data transmission links have become urgent requirements for the heavy-ion physics experiments. VCSEL-based array optical transmission system with advantages of high data throughput, compact size and low power consumption is an effective solution for transmission links in these heavy-ion physics experiments. As a key component for optical transmission links, a 12-channel, anode-driving, 16G-per-channel VCSEL array driver ASIC has been designed for VCSEL-based array optical transmitters.

The VCSEL driving ASIC is fabricated in a 130-nm SiGe BiCMOS technology and its block diagram is shown in the Figure 1. The chip consists of an I2C module and 12 independent channels. The power supply for the whole chip is 3.3 V and we use a Low Dropout regulator (LDO) to generate 1.2 V power supply for I2C module. In each channel [1], it consists of an equalier, a limiting amplifier, and an output driver. The equalizer is used to compensate high frequency attenuation of the input signal at PCB traces. And we employ a signal detector to monitor the input data stream. The signal detector will generates an system interrupt when the received data amplitude is very low. In the limiting amplifier design, the function of polarity inversion is equipped. Polarity inversion allows the user to implement the equivalent of a board level crossover without additional via impedance discontinuities that degrade the high frequency integrity of the signal path. In the output driver stage design, the output driver translates the differential signals into switching single-end current to drive the VCSEL array. We use a programmable pre-emphasis to enhance the bandwidth of the output driver and a VCSEL supervisor to monitor the voltage at VCSEL anode. The modulation current and bias current for VCSEL is adjustable via I2C module. The power consumption of the channel is 48mW when it operates at 16-Gbps data rate. The die area of the whole chip is 3.6x2 mm2. The design have been verified in simulation and submitted for prototype fabrication. We will test the chips in this June.

Primary author: ZHOU, wei (China Electronics Technology Group Corporation 58th Research Institute)

Co-authors: Mr ZOU, Jiaxuan (China Electronics Technology Group Corporation 58th Research Institute); WANG, Wei (China Electronics Technology Group Corporation 58th Research Institute); WANG, Zhanfeng (China Electronics Technology Group Corporation 58th Research Institute); Mr LIU, Shiquan (China Electronics Technology Group Corporation 58th Research Institute)

Presenter: ZHOU, wei (China Electronics Technology Group Corporation 58th Research Institute)

Session Classification: Poster (incl. coffee)