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P1.3: Firmware implementation of a displaced muon reconstruction algorithm for the Phase-2 Upgrade of the CMS muon system

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This study presents the firmware implementation of an algorithm to reconstruct displaced muons for the Overlap Muon Track Finder (OMTF) of the Level-1 Trigger System (L1T) targeting the Compact Muon Solenoid (CMS) experiment upgrades for the High Luminosity Large Hadron Collider (HL-LHC). The firmware response is also compared to that of the software emulator.

The Upgrade L1T system of the CMS experiment, foreseen for the HL-LHC is fully described in a Technical Design Report (TDR) [1]. The foreseen system should greatly extend the throughput and capabilities of the current system despite the harsher environment. The L1T system has been designed to process 63 Tb/s input bandwidth with state-of-the-art commercial Field Programable Gate Arrays (FPGAs) and high-speed optical links reaching up to 28 Gb/s using generic-processing cards based on Advanced Telecommunications Computing Architecture (ATCA) technology.

The OMTF has been previously implemented both in VHDL [2] and HLS [3]. Neither of this versions includes a solution for displaced muons. The HLS version was developed as an assessment of the suitability of high-level synthesis for the design of complex hardware systems and and neither includes the latest design changes in the algorithm, nor is it optimized. This version is used as a starting point to add the displaced muon algorithm, include the latest design changes for the current run and also improve the design in terms of latency and area.

Displaced muons are an important signature of new physics beyond the standard model (BSM). There are models [4] that predict long lived muons that can be produced in the LHC collisions. These long-lived particles can decay inside the detector and produce displaced muons. For this task, the CMS trigger system should be updated to be able to trigger on these particular events.

Algorithm development in software and its subsequent implementation in hardware will allow to establish a comparison between both approaches efficiencies and help to trace the suitability of this hardware/software design method for the development of complex hardware systems in the field of particle detector physics.

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