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P1.16: The SparkPix-S ASIC for the sparsified readout of 1 MHz Frame-Rate X-ray Cameras at LCLS-II: pixel design and simulation results

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Exploiting the “sparse” nature of the information in XPCS and XSVS experiments, we present the SparkPix-S, a 3-sides buttable Application Specific Integrated Circuit (ASIC) based on a sparsified readout strategy for large-format hybrid detectors. The SparkPix-S architecture, based on the successful ePix family, will be composed as follows: a front-end 2-D matrix of 384×352 square pixels with $50 \mu\text{m}$ pitch is arranged to match the dimensions of a PIN Si-sensor matrix; charge readout, signal shaping and amplitude discrimination is performed at pixel-level, by means of a low-power ($<18 \mu\text{W}$) analog processor, which, in case of an event, negotiates access to an analog bus placed every other column; on the chip periphery (balcony), the information on each bus is digitized by an array of successive approximation analog-to-digital converters (SAR-ADCs) running at 10 Msps; on the digital back-end the global logic will generate the output data stream using low-voltage differential signalling (LVDS).

A first prototype of the SparkPix-S, with a reduced matrix size of 96×96 pixels, is currently under production on a 130 nm CMOS technology. Simulated performance results show an equivalent noise charge <60 el. r.m.s. at 1 MHz repetition rate, with a maximum input energy of 60 keV and capability to discriminate charge signals with equivalent energy as low as 900 eV.

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