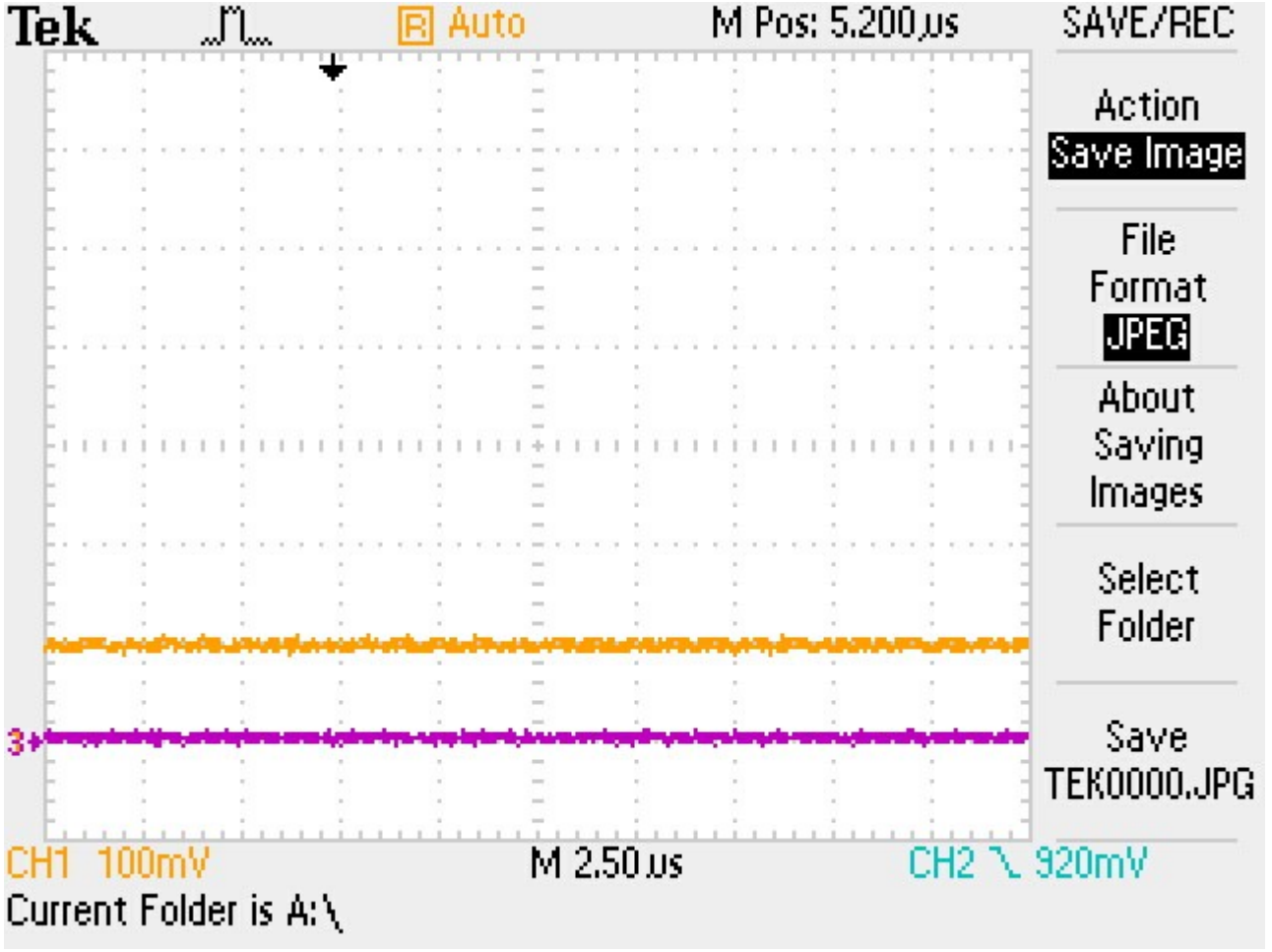
RD50-MPW3 NOISE MEASUREMENTS

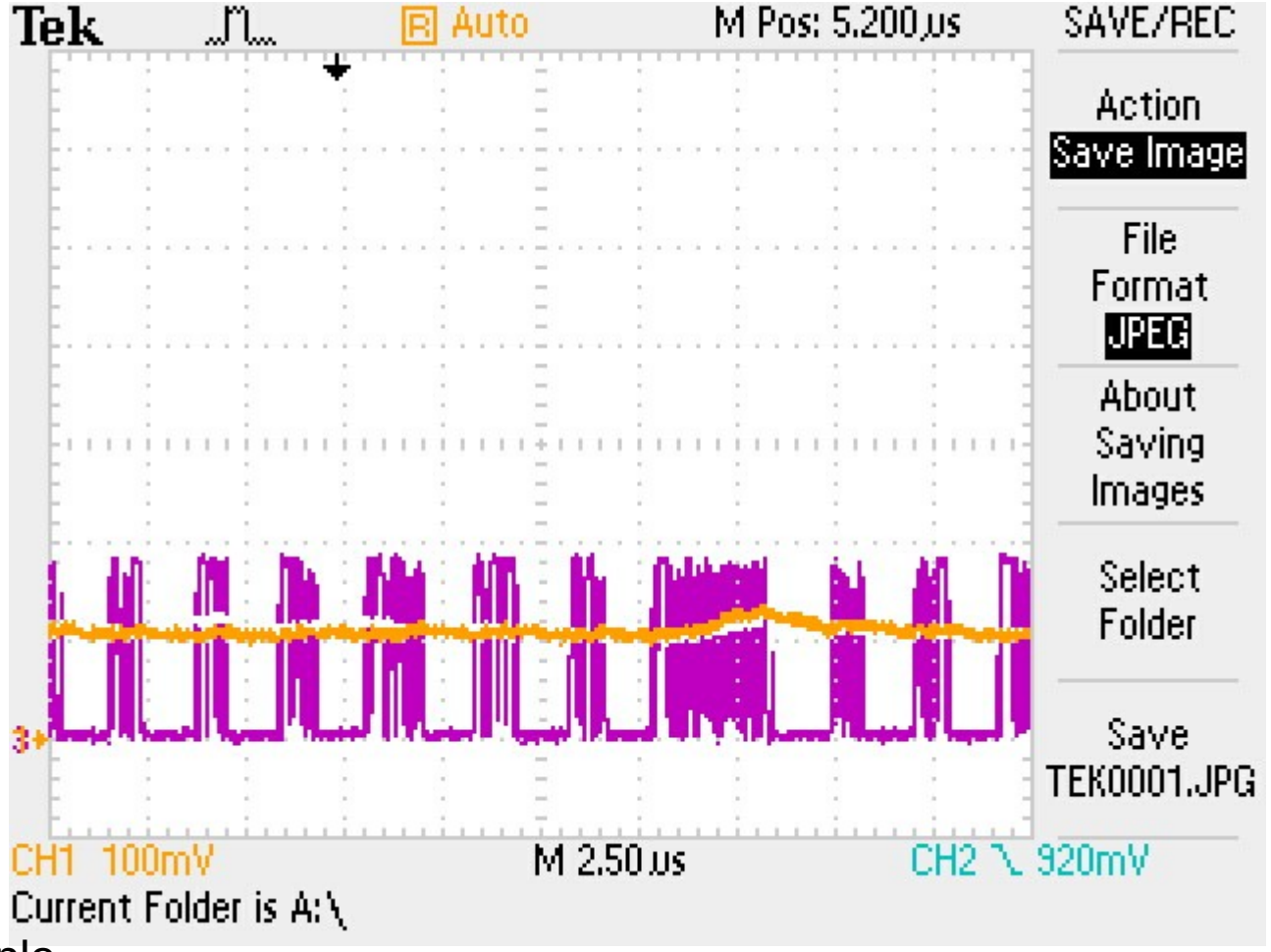
02/02/23

RD50-MPW3 – No clock and no comparator activity



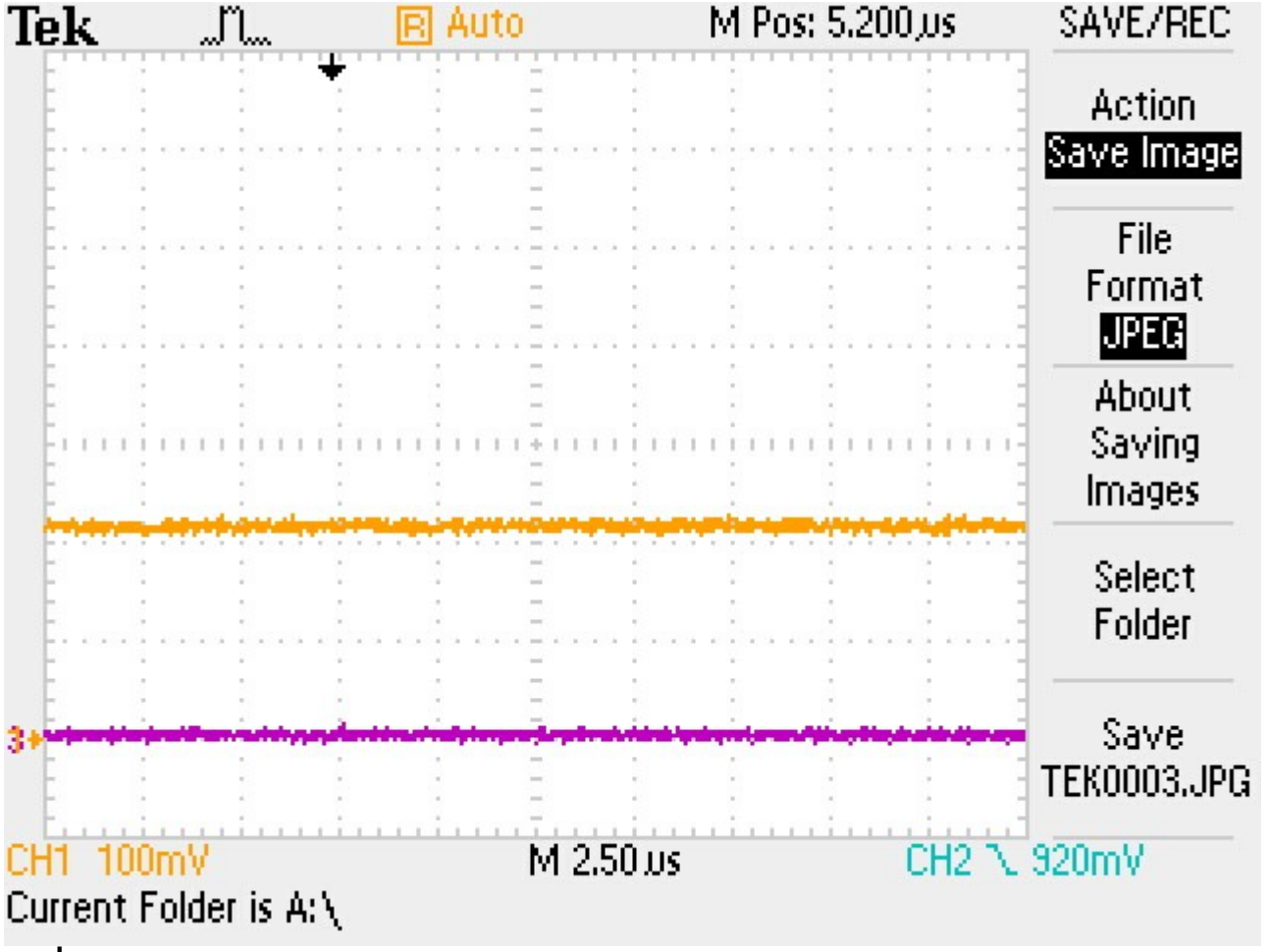
- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 100mV

RD50-MPW3 – No clock with comparator activity



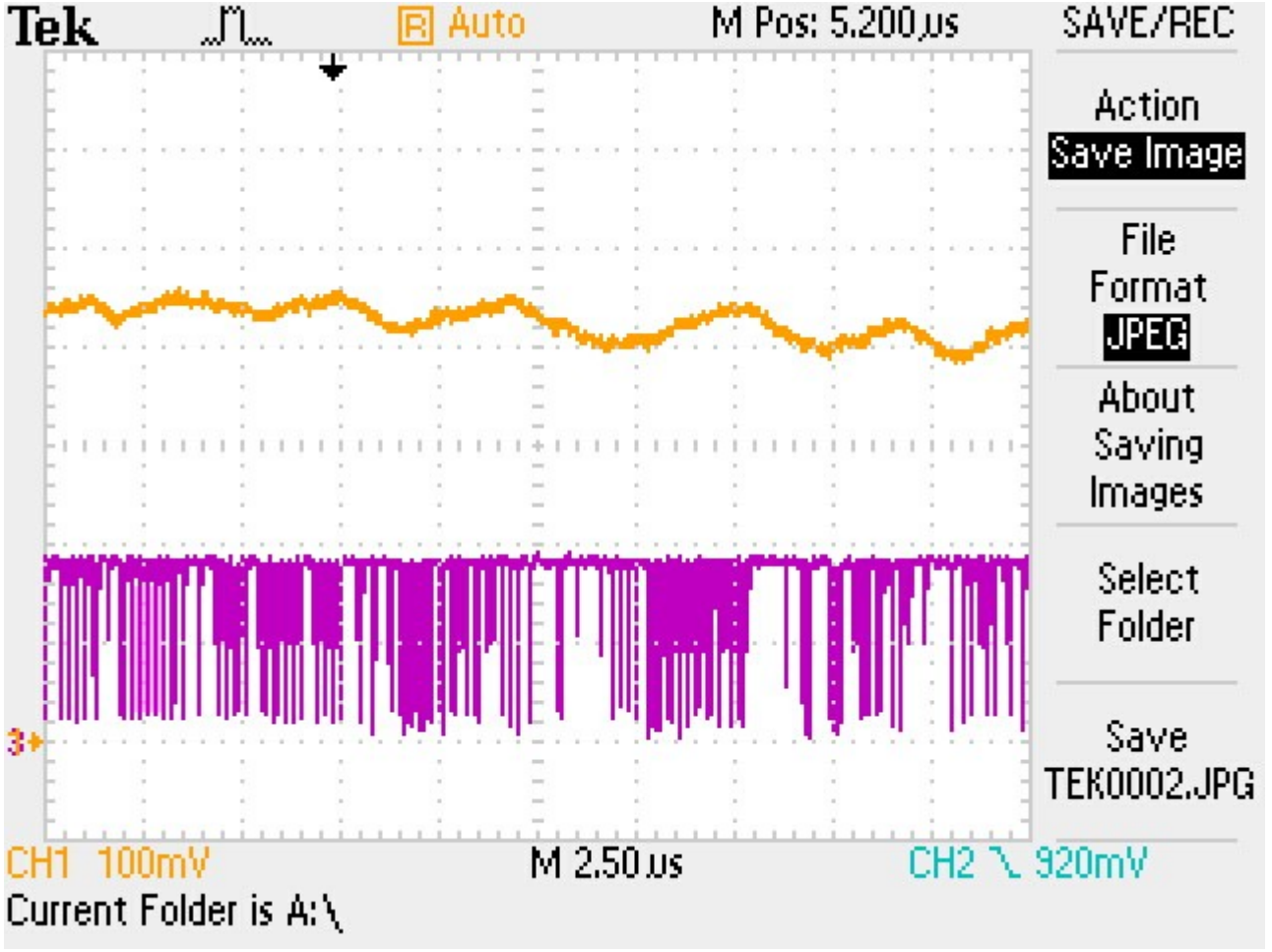
- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 100mV (no significant change but some “charging” of SFOUT during comparator activity)

RD50-MPW3 – With clock and no comparator activity



- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 220mV (increase in offset compared with no clock)

RD50-MPW3



- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 420mV

RD50-MPW3

- DC offset of SFOUT without clock = 98mV
- DC offset of SFOUT without clock and comparator activity = 101mV
- DC offset of SFOUT with clock = 240mV
- DC offset of SFOUT with clock and comparator activity = 430mV
- No ground rise observed when probing GND close to the chip (with respect to true chassis ground of power supply). If a ground rise is the cause it may be internal to chip
- No difference observed when using external 40MHz clock enable
- Is this ground rise or capacitative pickup??
- Suggested experiment… Changing the duty cycle of the clock should tell us if the issue is capacitative coupling or not. A greater duty cycle would increase the DC offset. Suggest monitoring current draws while changing duty cycle of the clock and observing DC offset.
- If the increased offset is caused by a high current from digital section going through a resistance to ground it should increase with frequency (increased switching frequency increases current draw). Would be nice to try with multiple frequencies (already attempted but ongoing..).
- Simple test would be to program the chip and then switch to external clock with jumper select for external 40MHz clock (requires few firmware changes if just outputting different frequencies on external clock pin and looking at analogue outputs).