The ATLAS Central Trigger from Phase-1 to Phase-2

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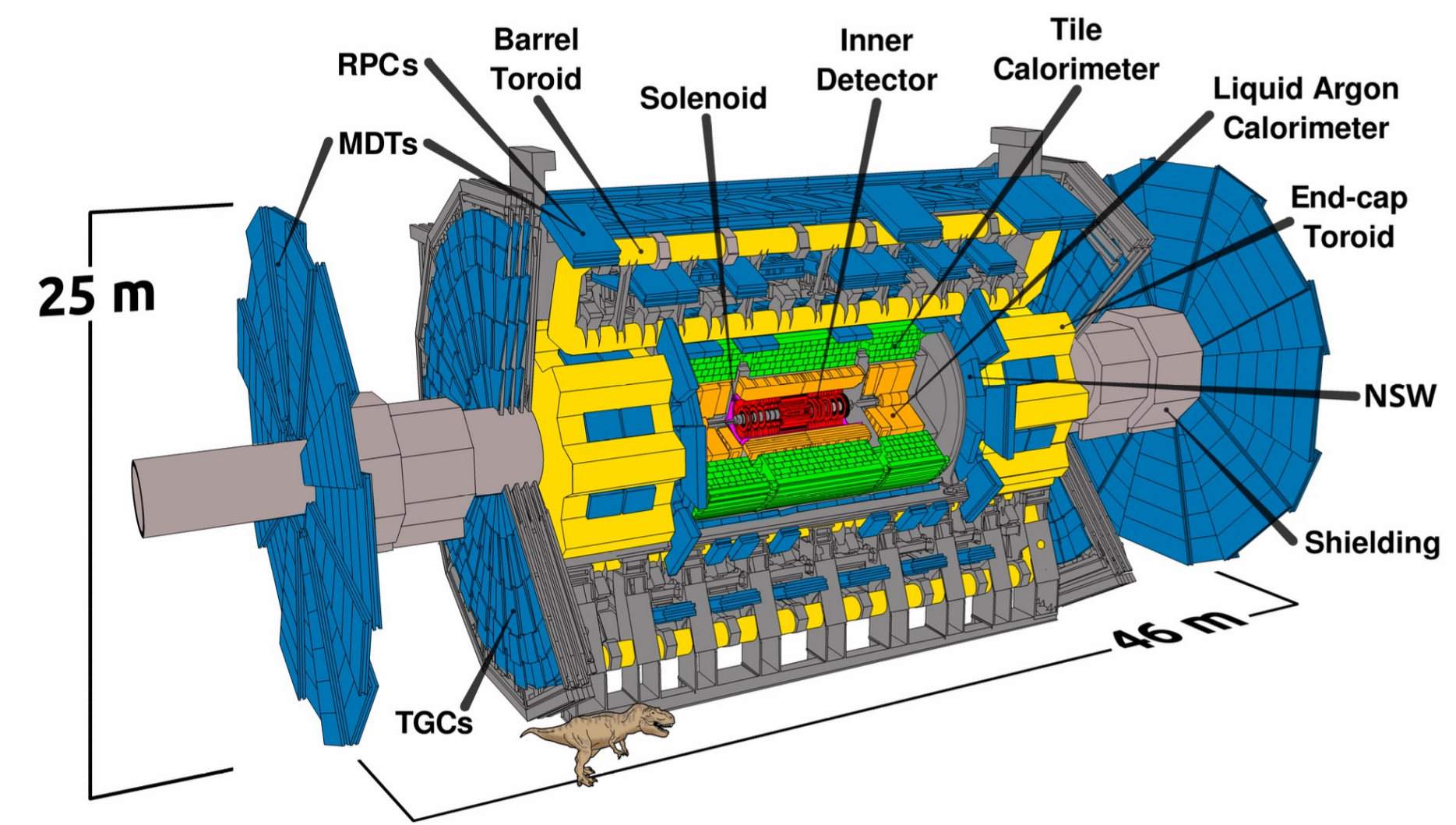
The ATLAS detector

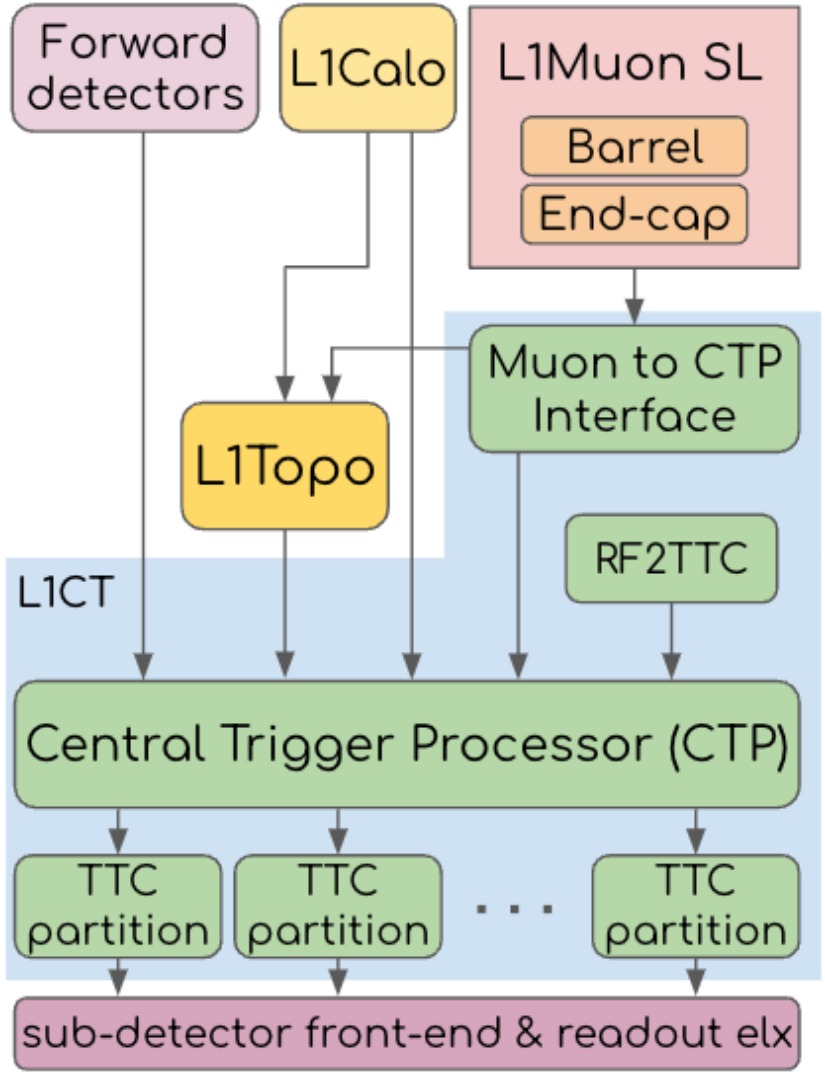


Some facts that are nice to remember

- Bunch crossing (BC) every **25ns** (40 MHz clock)
- **3564** bunch crossings are organized in **trains**
- Each train has a clock of 11.2455 kHz, and this is called **ORBIT**
- Interesting interactions are rare and come together with other common interactions, that we call **pile-up**. Run-3 values are ~60
- The record of all the physics data from a BC is what we call **event**
- Data taking is a challenge. Handling throughput and storing data is useless and impossible

@ 13 TeV: inclusive $\sigma_H \approx$ 60 pB, $\sigma_{tot} \approx$ 100 mB $\rightarrow \sigma_{tot}/\sigma_H$ =1.6 10^9

Phase-1 Level-1 Trigger system

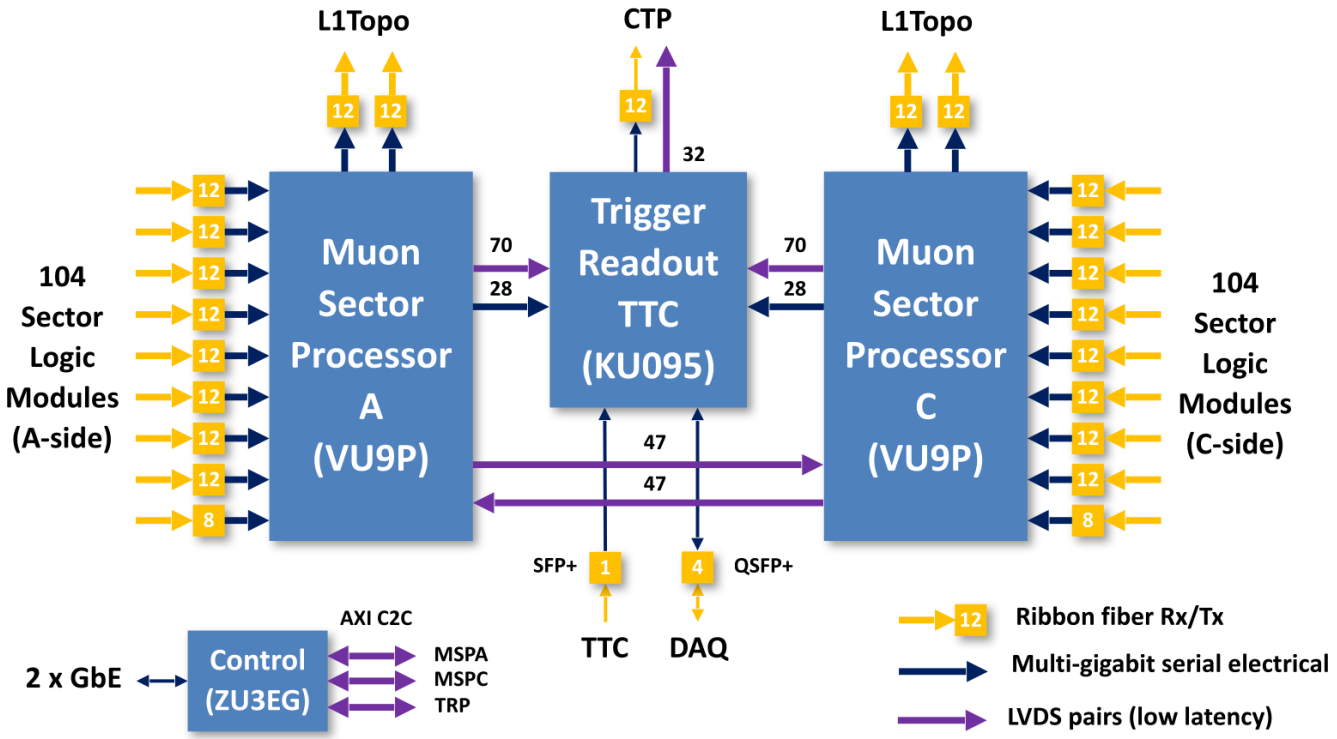


Thanks to Dr. Koulouris for the figure source file.

1. Trigger information comes from the Muon Spectrometer and the Calorimeter
2. This is elaboarated in Level-1 Calo and Muon systems. Objects like electrons, photons, taus, jets, and muons are identified
3. The Central Trigger Processor receives trigger inputs and take the L1 accept decision (L1A)
4. The L1A signal propagates back to the F.E. electronics for the readout
5. L1A max rate: 100 kHz
6. Average output rate: 1 kHz (limited by storage)
7. The total maximum latency is **2.5 μs**

Muon-to-Central Trigger Processor Interface (MUCTPI)

The MUCTPI aggregate the muon candidates from all 208 muon sectors, resolve overlaps, perform multiplicity summing, and send candidates to L1Topo.



- Single ATCA blade.
- 104 + 104 optical inputs from muon sectors of side A and C.
- 2+1 processing FPGAs.
- SoC for board configuration, control and monitoring.
- ATLAS Run Control monitoring applications run on the SoC.
- C++ API to read/write FPGA registers.

Central Trigger Processor (CTP)

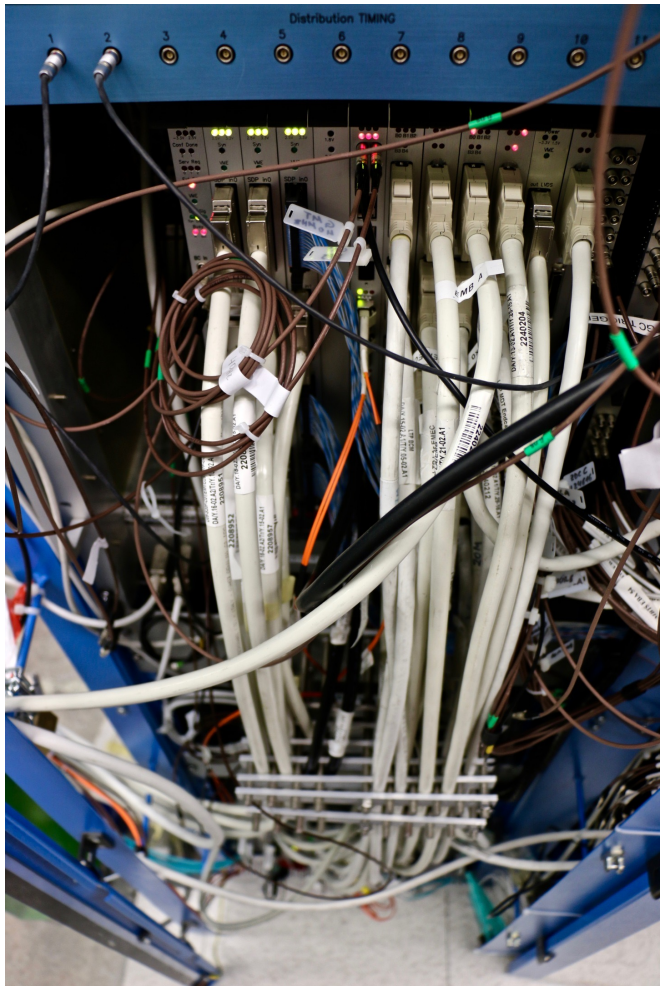
The CTP aggregate trigger signals from all trigger detectors and make the L1A decision based on a programmable trigger menu.

The CTP consists in 13 boards housed in a 9U VME crate. Its inputs are:

- 320 inputs from Pattern-In-Time (PIT) backplane (dedicated bus for synchronized and aligned trigger inputs)
- 192 direct low-latency electrical inputs
- 480 optical links

However, the CTP can use only **512 inputs**, which are selected with a switch matrix.

After L1A, the CTP is responsible to introduce simple and complex **deadtime** (more in the backup).



Trigger and Timing Control (TTC)

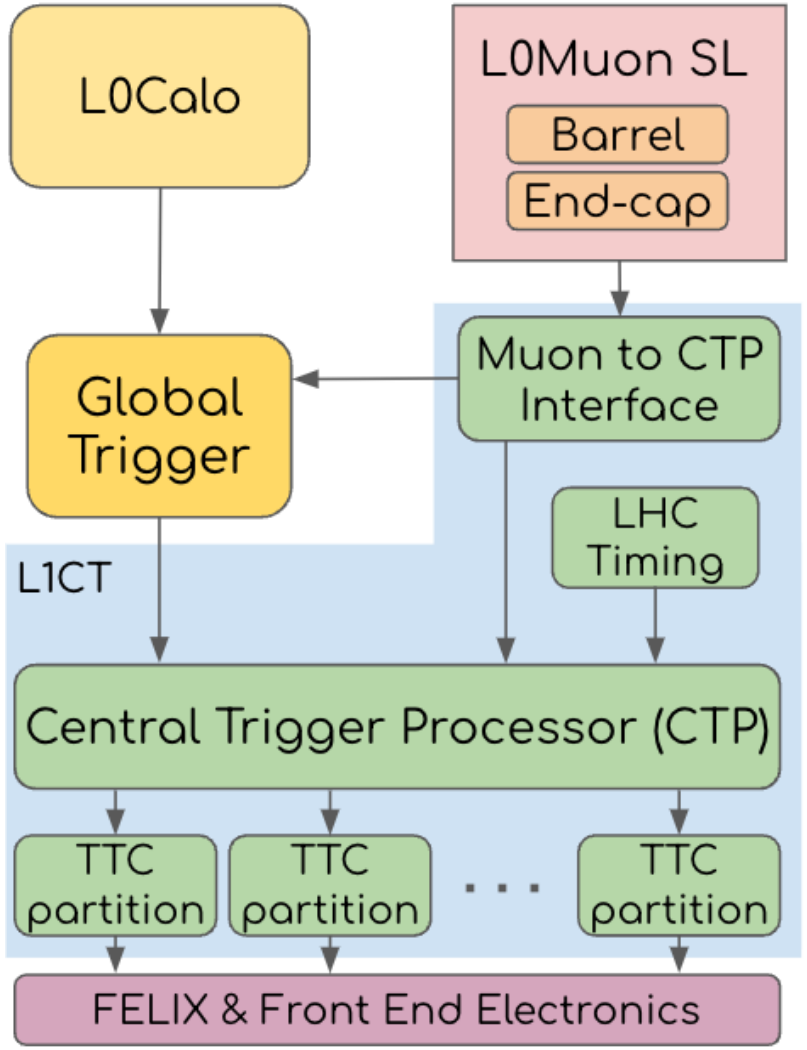
The TTC system fan out and distribute trigger and timing signals to the readout electronics. Typical signals are:

- LHC and ORBIT clock.
- L1A.
- Test and calibration signals.
- Synchronisation (Event Counter Reset, Bunch Counter Reset).

The TTC is partitioned for each sub-detector, where the interface is the **ALTI** board.

ALTI is the interface to the CTP, replacing the CTP in standalone runs, user interface for local TTC actions.

Phase-2 Level-0 Trigger System



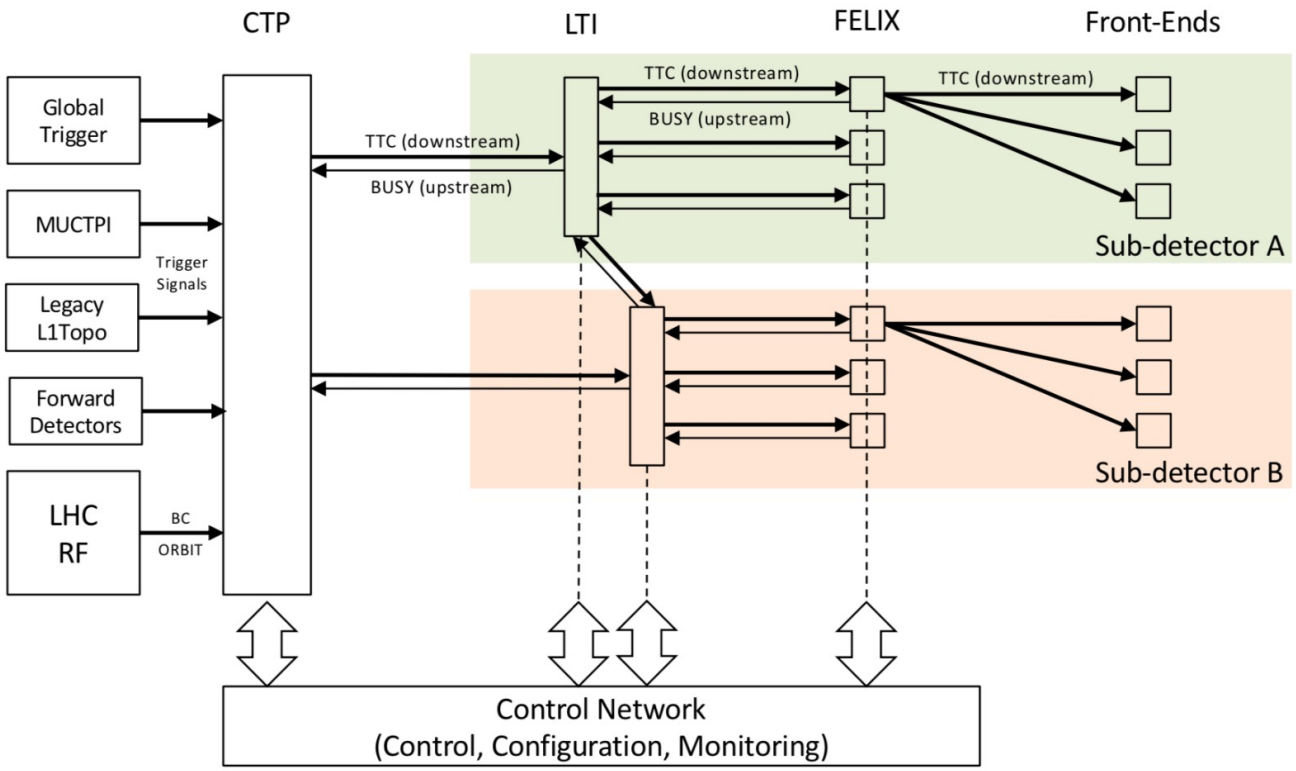
- Organised in Level-0 Trigger + HLT.
- Output rate x10: **1 MHz** L0, **10 kHz** on disk.
- New **Global Trigger** system. It will run algorithms on calo, muon, and LAr data and identify topological signatures.
- L0Calo and L0Muon will receive upgrades like “forward FEX”, and inclusion of precise MDT measurements.
- New latency limit for L0A is **10 μs**.

Phase-2 MUCTPI

- ATLAS will operate with two Phase-1 MUCTPI modules. There will be **one module per detector side**, doubling the available bandwidth.
- New firmware is required, and this implies that current configuration, control and monitoring applications will need an update.
- New interface with the Global Trigger, that will receive muon candidates for further processing.
- Multiplicities for different p_T thresholds will still be sent to the CTP.

Phase-2 CTP

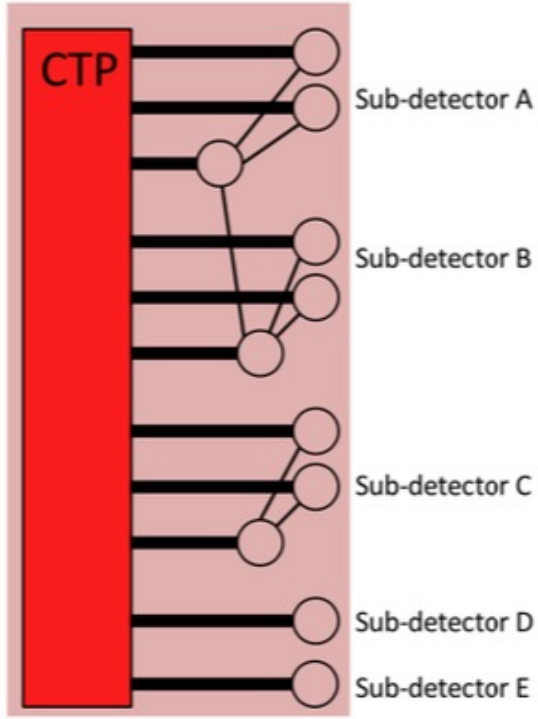
- The Phase-2 CTP will be completely renewed with custom ATCA blades.
- 1500 optical inputs, and 1024 trigger items.
- The TTC links will interface with the new Local Trigger Interface (LTI), which replaces ALTI.
- The LTI will provide downlink (TTC) and uplink (BUSY) interface between CTP and FELIX.
- The interface with the readout system will be only the FELIX board.
- New hardware, new firmware, and new software will be needed.



Phase-2 TTC

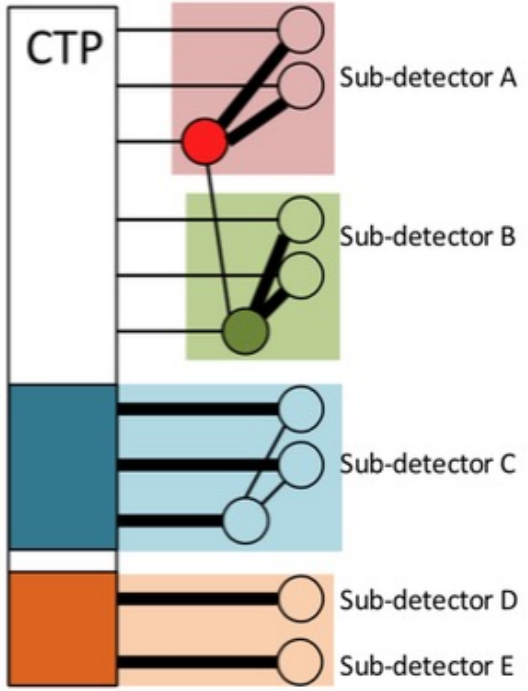
- The TTC network will be completely renewed, with the use of optical fibers.
- Configurable TTC network.

Active links in bold.



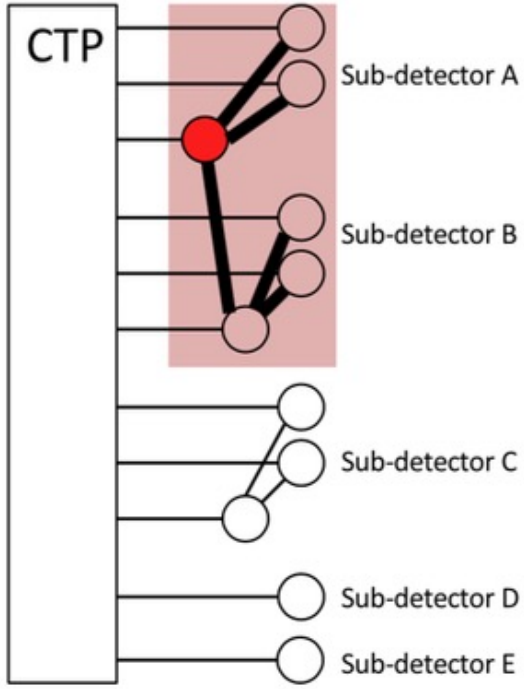
Only ATLAS partition (physics data-taking).

CTP is TTC master.



CTP-combined partition. For testing and sub-detector calibrations.

CTP is TTC master of several partitions.



Standalone partition.

LTI is the TTC master.

Other LTIs from other sub-detectors can be slaves.

Phase-2 Local Trigger Interface (LTI)

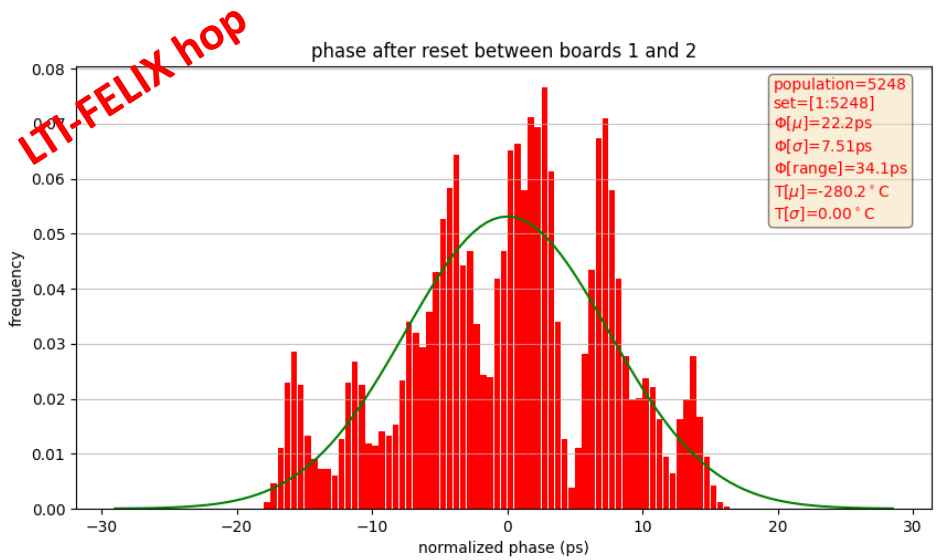
- Each LTI is implemented as a single ATCA blade.
- 74 bi-directional optical links.
- 8 electrical inputs for standalone tests and calibration requests.
- Each LTI can operate emulating the CTP.
- For physics runs the LHC clock is recovered from the CTP downlink, and it needs to have **good phase stability and low jitter**.
- Phase-II High-Granularity Timing Detector will need a phase stability of better than 30 ps for the full chain to digitize detector signals with good precision.
- Currently we are fighting problems with phase determinism of different FPGA families and transceiver technologies (GTY and GTH). We are working on an algorithm for phase compensation.

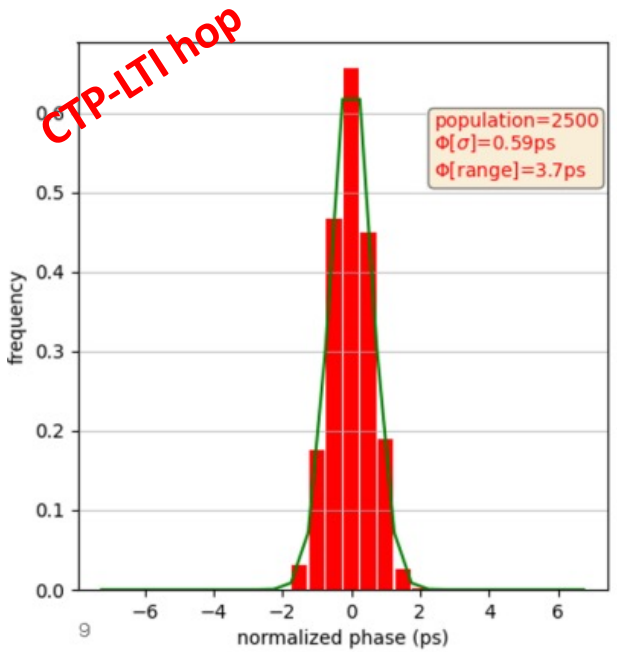
Phase determinism problem

After full reset of the links.

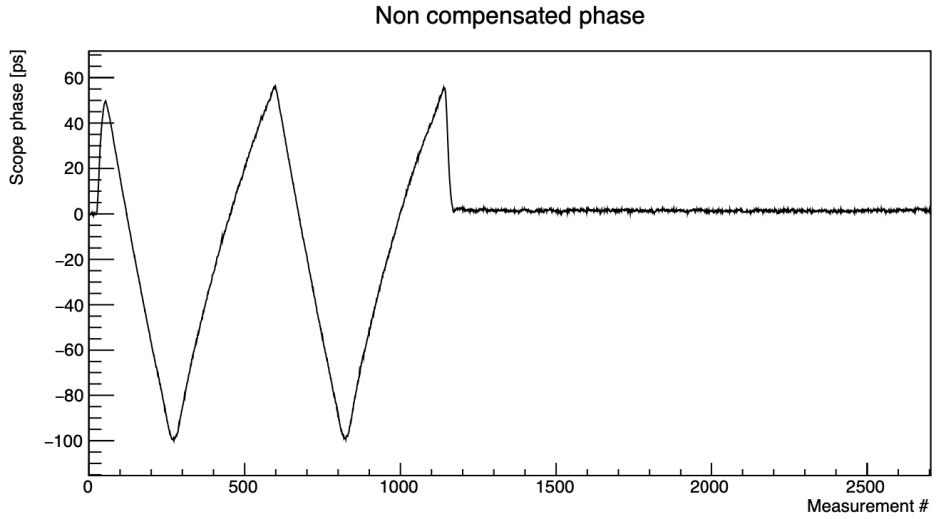
- Solved for the CTP-LTI hop.
- Not solved for the LTI-FELIX hop.

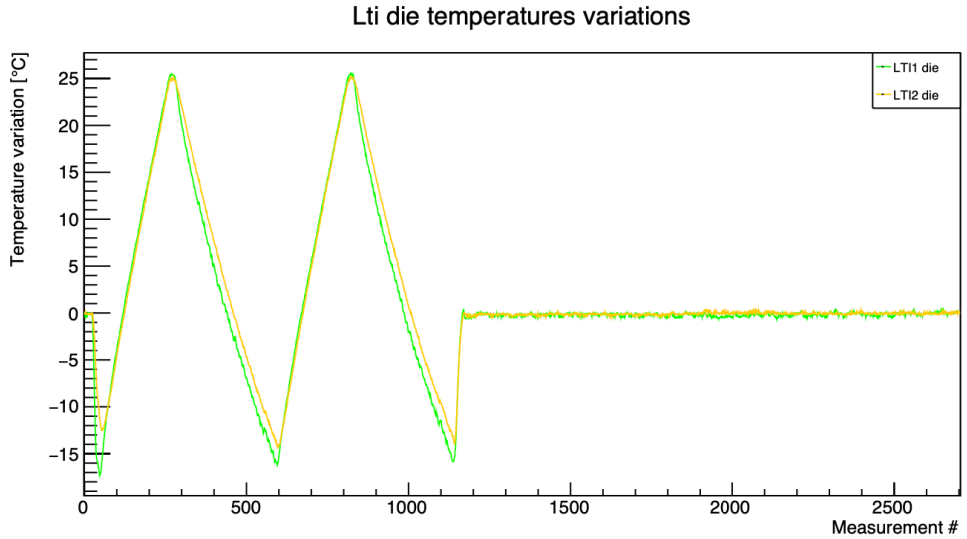
FELIX Versal FPGAs and GTY transceivers are problematic.





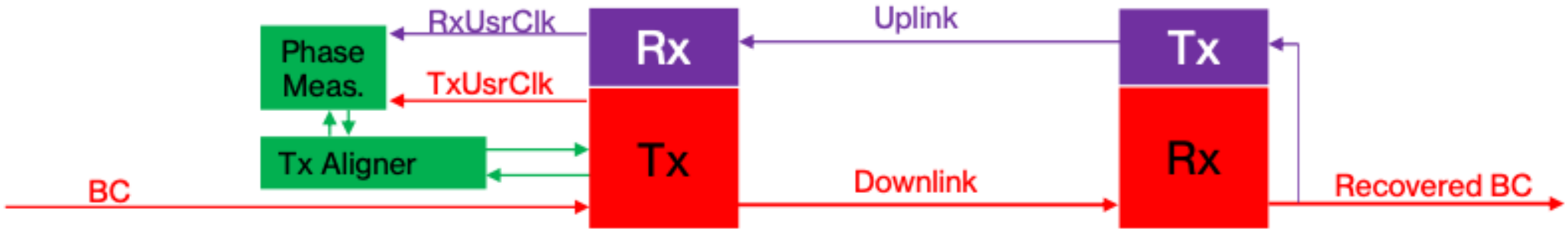
With LTI silicon die temperature variations (and also fibers temperature).





Timing Compensated Link (TCLink)

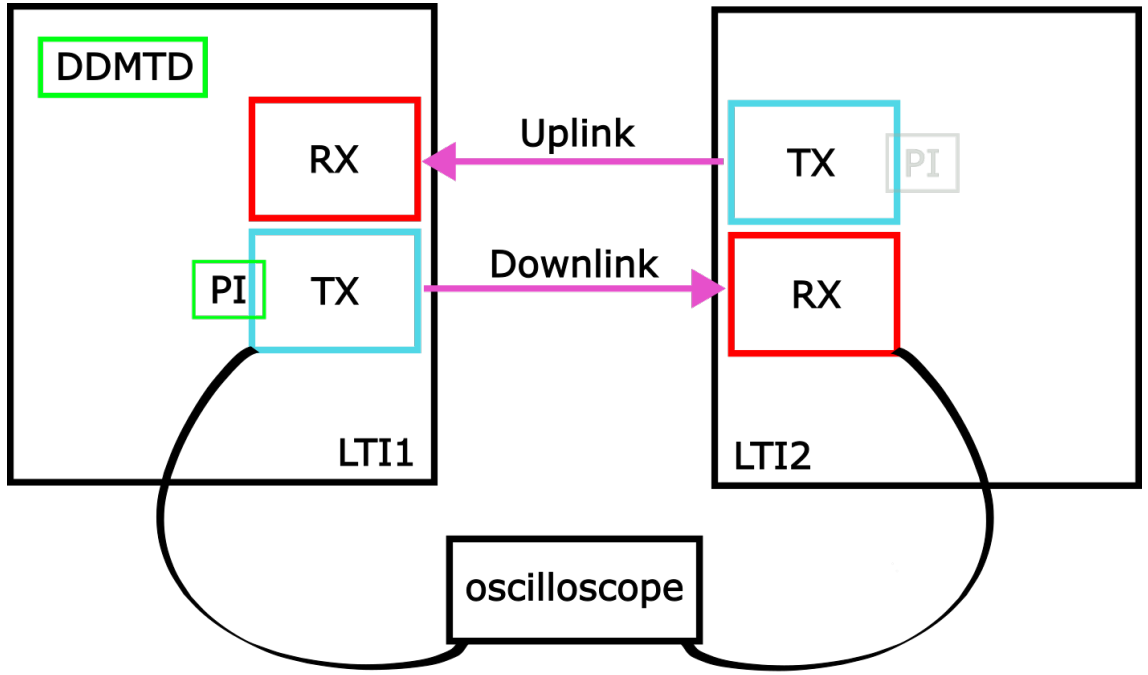
For long-term stability of the phase it is required a system that compensates the changes in environment conditions. **TCLink** is an FPGA-agnostic core developed at CERN with the purpose of compensate phase variations at a picosecond level.



The TCLink can measure the phase of the clock via the Digital Dual Mixer Time Difference (DDMTD) with a resolution of around 4 ps, and then it can shift the phase with the Tx Aligner (Phase Interpolator core). The shift is done in units of ~1.6 ps.

LTI lab setup

LTI used for tests: Zynq UltraScale+ MPSoC ZCU102 + GTH transceiver (both TX and RX).

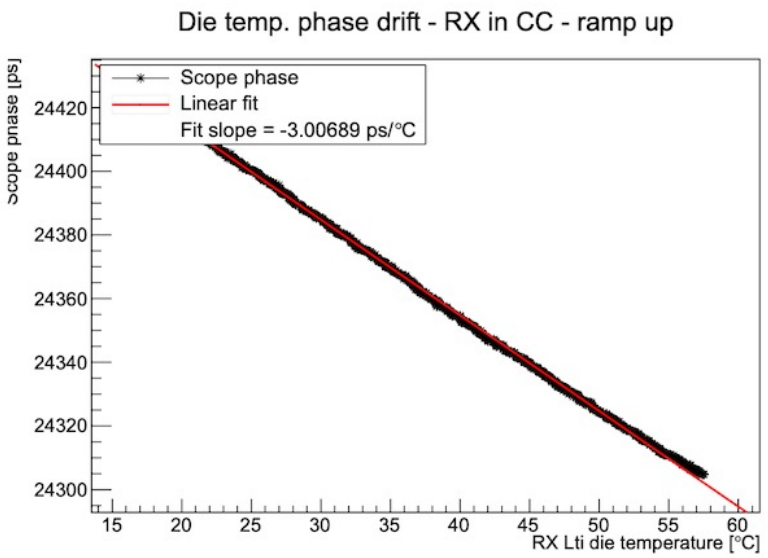


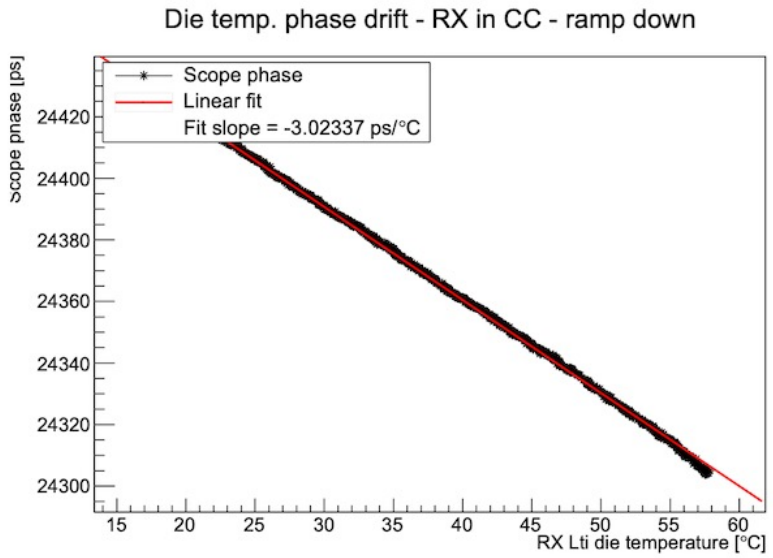
During operations it’s not practical to use a scope for each LTI. However for lab tests an oscilloscope is used as oracle that gives true phase.

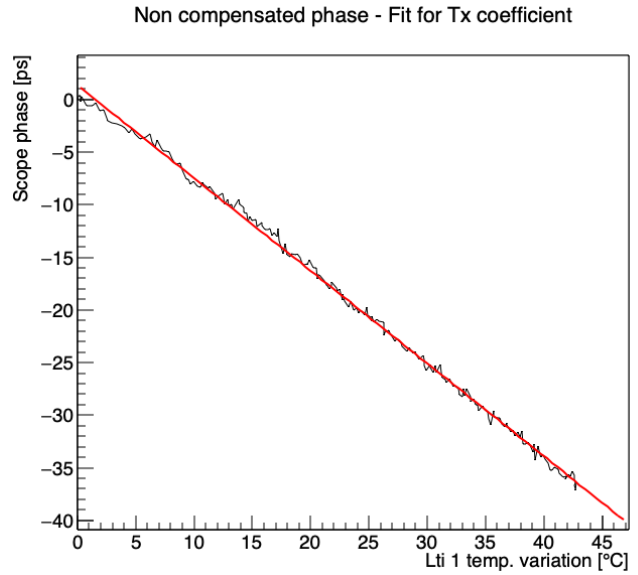
Temperature is controlled with a climatic chamber.

Climatic chamber tests

With linear fit over climate chamber data we found 3.02 ps/°C for Rx and 0.88 ps/°C for Tx.

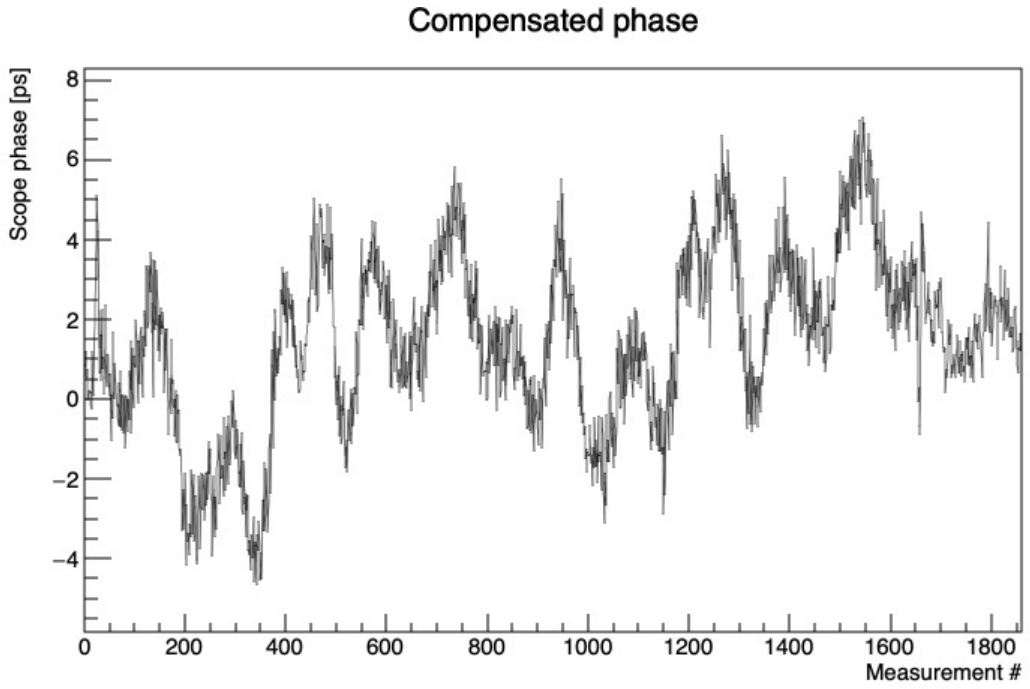


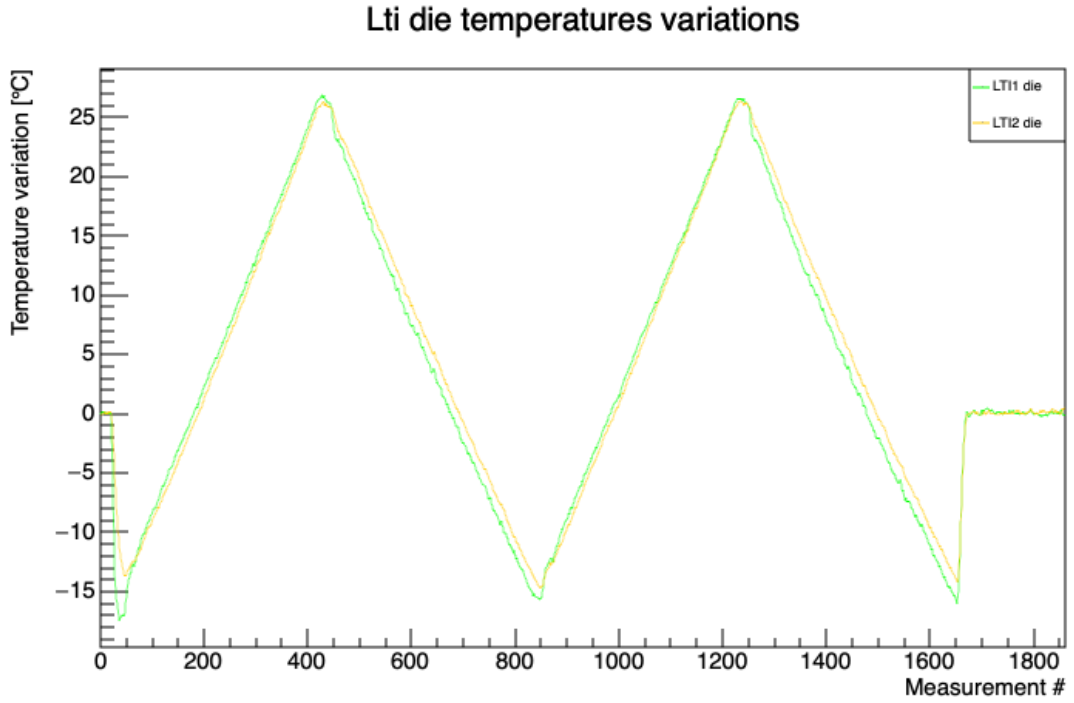




Compensation algorithm – first outcome

- Compensation algorithm based on LTI die temperature variations.
- Resolution of die temperature sensor: 0.5 °C.
- DDMTD here it is not used, but for the next iteration of the algorithm it will be integrated.



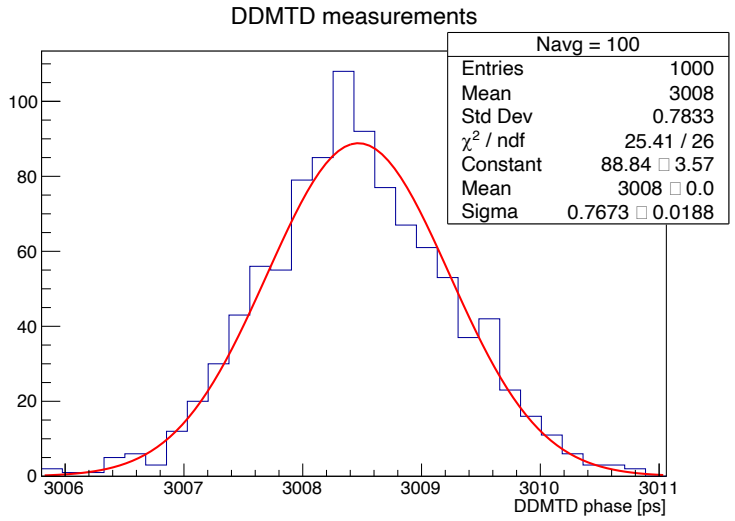


The relative phase is approx. between -4 ps and +7 ps. Still a lot to improve.
Other tests are ongoing to improve the DDMTD resolution by varying some parameters.

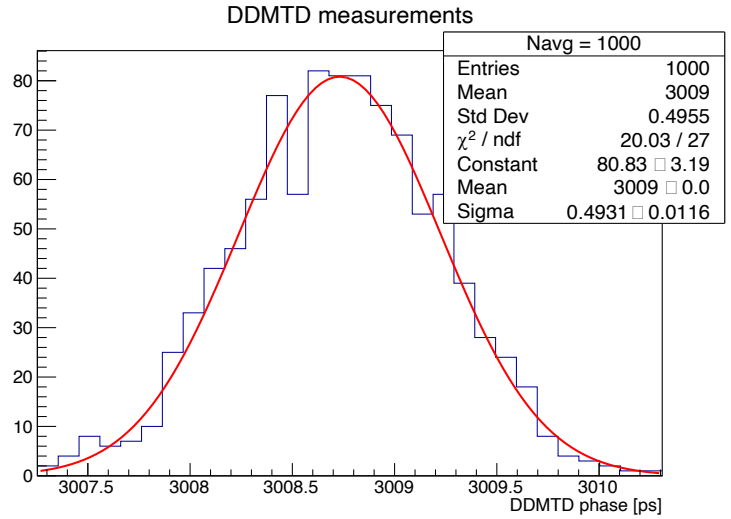
DDMTD resolution tests – **preliminary** (from this morning)

The low-level functions that permit to get the DDMTD value can accept a parameter Navg to iterate over DDMTD measurements, and return the average.

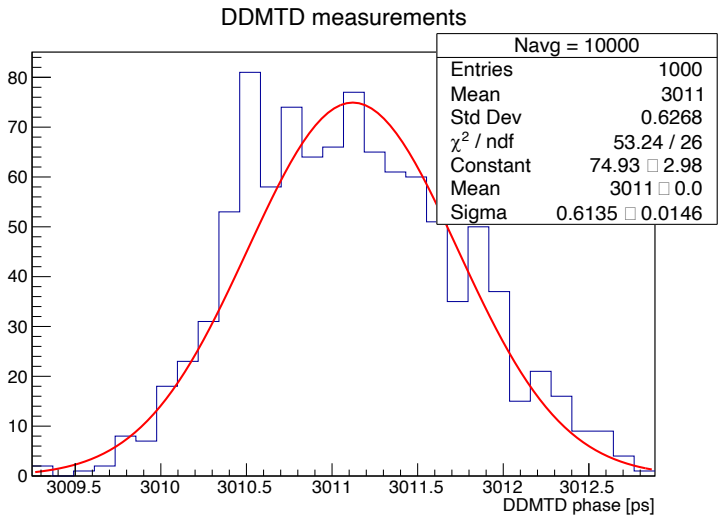
We vary this parameter from 1 to 10000. The test was executed at room temperature. We monitored the scope phase at the beginning and the end.



Scope phase shift: 0.77ps



Scope phase shift: -0.4ps



Scope phase shift: 0.4ps

It might be that a too big Navg is actually not the best option, if the computation time is too large and the phase can drift.

Summary

- Overview of the Central Trigger, for the current Phase-1 and for the next Phase-2 upgrades.

- The Preliminary Design Review of the LTI took place few days ago (12th Oct). The production of first prototypes is starting.

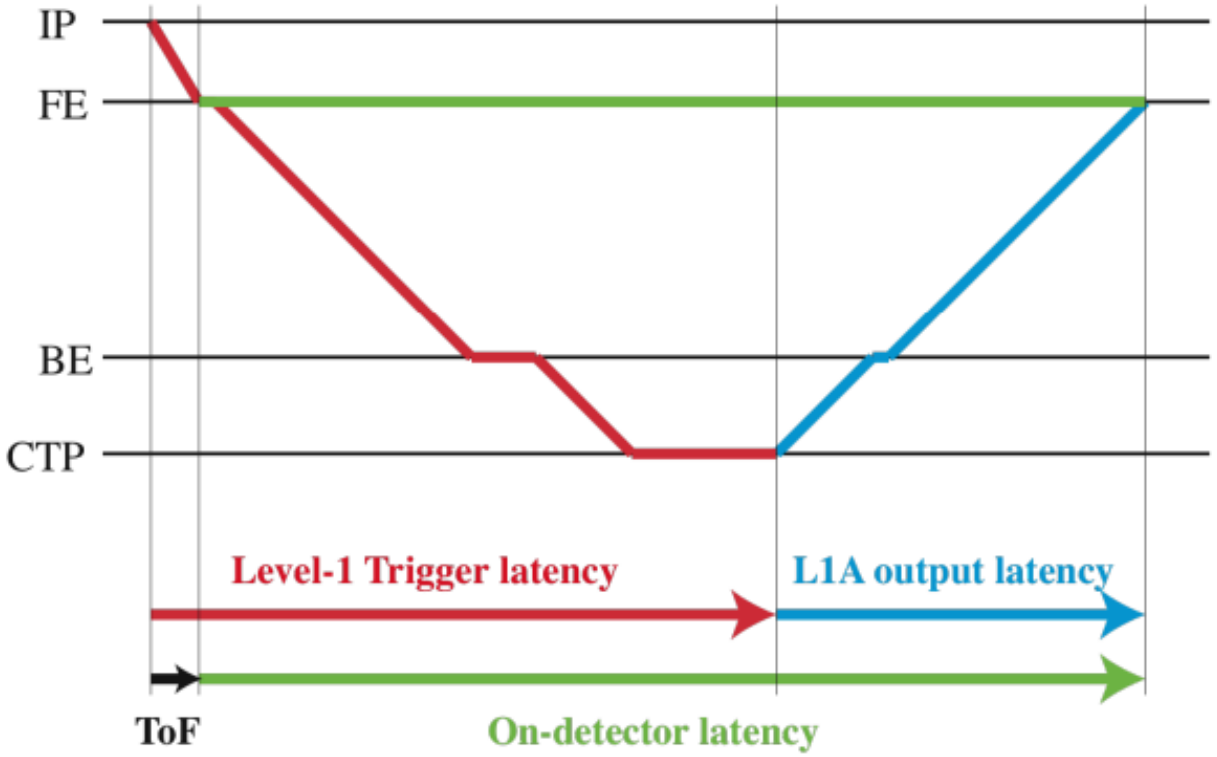
- The problem of phase stability after transceiver reset and LTI die temperature variation has been addressed with hardware tests, which are still ongoing.

Thank you for your attention

Thanks as well to all the L0CT people for the continuous help.

Backup

Latency of Level-1 Trigger



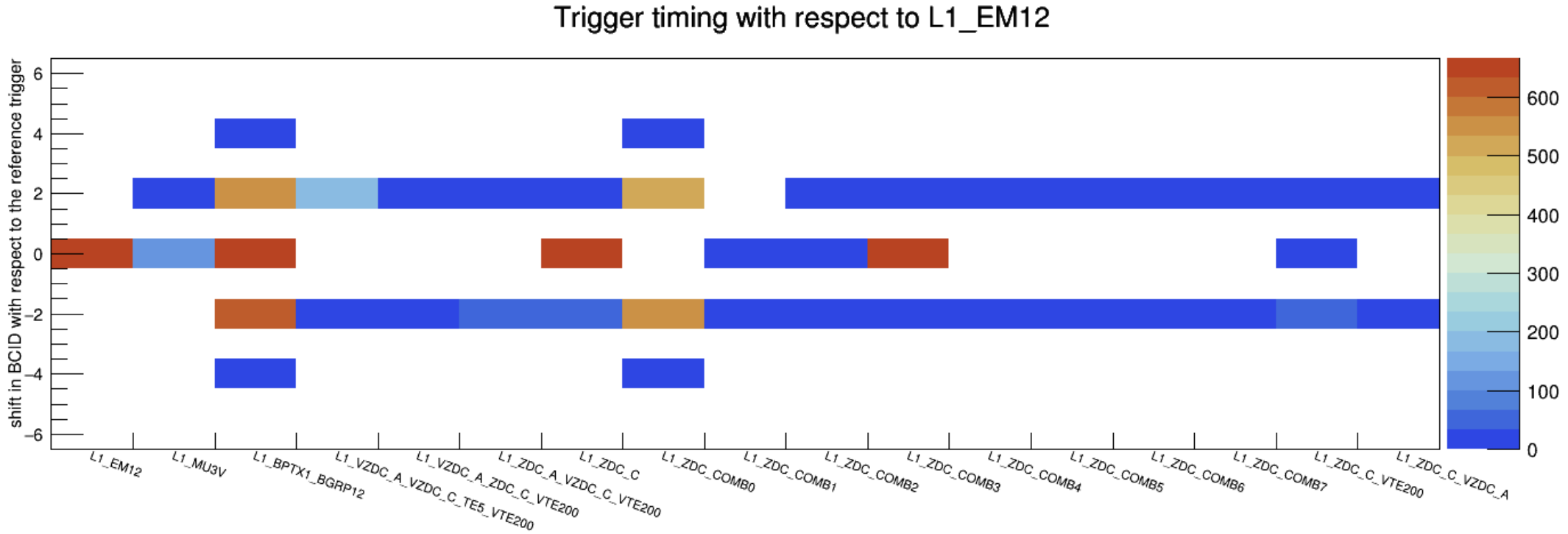
L1 Trigger latency is 84 BC, while for the entire L1 system considering also Readout latency the value is 100 BC.

Deadtime

The deadtime is the time where a L1A cannot be issued. It has two components:

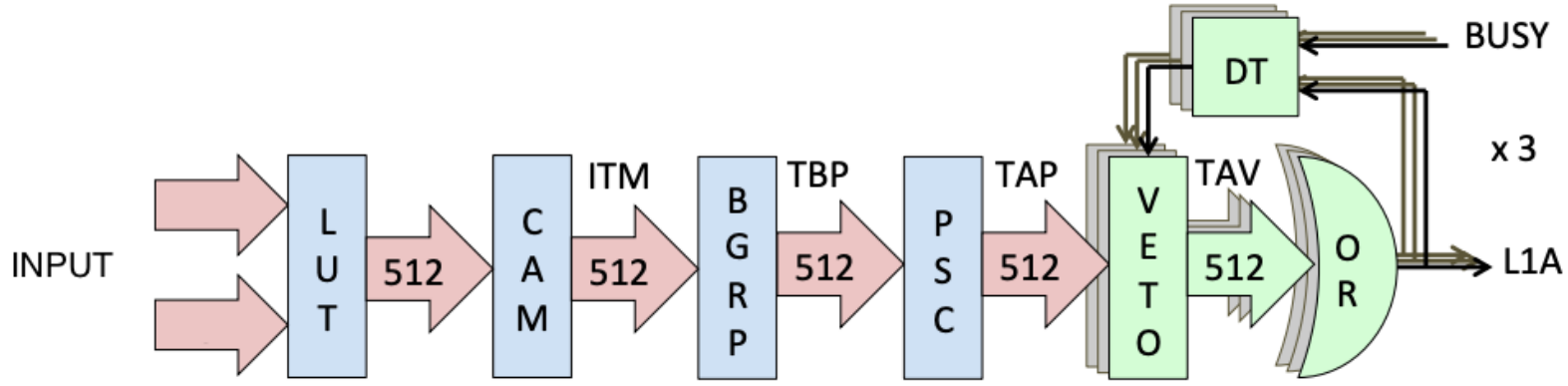
- Simple: Every L1A is followed by 100 ns (4 BC) of deadtime to take in consideration front-end busy.
- Complex: The number of L1As occurring in a time window are limited to prevent L1 buffers to overflow.
- Complex deadtime algorithms are implemented as “leaky bucket” algorithm. The bucket has a size B, and inverse leak rate R. Every time a L1A is issued the bucket free size reduces by one. Eventually when it gets full the CTP must issue a deadtime of at least 1/R.
- Currently there are 4 buckets: L1Calo, TRT, LAr, and L1Topo.

Deadtime – Operations example



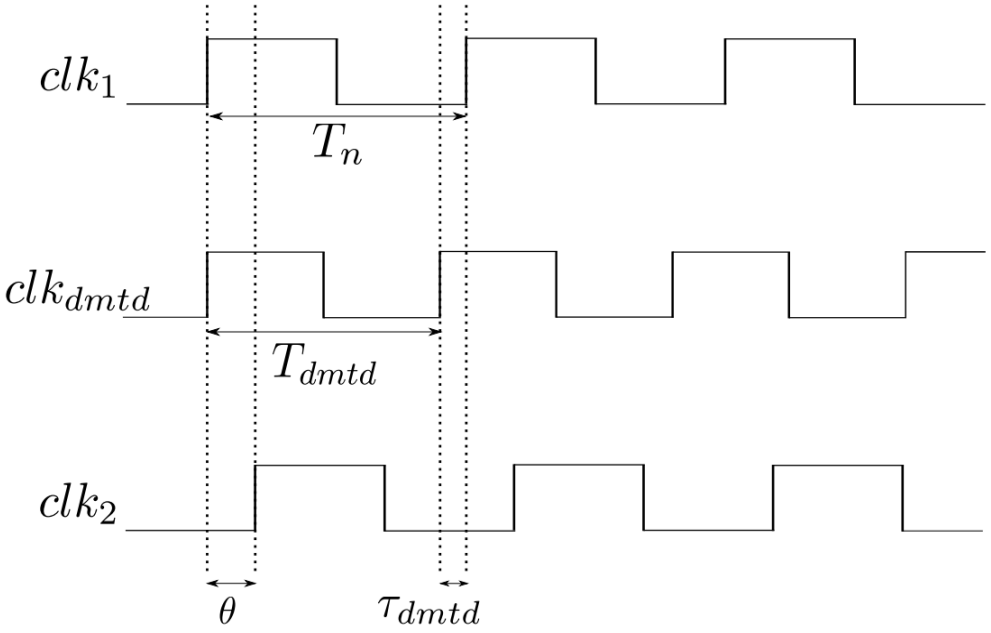
- October 3rd – In ATLAS the item used for the live fraction changed to L1_EM12 for stability reasons.
- Since then, we started to see a higher deadtime not in accordance with the simulations (5% vs 1.5%)
- ZDC items are designed to not trigger when L1_EM12 is triggering, however:
- The ZDC items can still trigger 2 BCs before since they have a large input signal, and this induces simple deadtime.

L1A formation



1. An array of LUTs that decode trigger multiplicities and do OR operations. This creates trigger conditions (e.g. at least 2 muons).
2. Trigger conditions are fed into a CAM, which can do AND and NOT AND operations. The combination of conditions form trigger items.
3. Programmable bunch group masks can be applied, specifying which BCID is allowed to fire per ORBIT.
4. Individual prescales can be applied to each item.
5. A Veto gate imposing deadtime is followed by OR of all items

Digital Dual Mixer Time Difference (DDMTD)



- We want to measure the phase shift between two input clocks clk_1 and clk_2.
- A third clock clk_{DDMTD} is also used. This is few Hz shifted from the two input clocks and provides a small beat frequency.
- Smaller the beat, smaller the DDMTD time step τ, which gives the unit in which the clk_{DDMTD} is moving away from input clocks.
- The phase shift \Delta\varphi between the clocks can be measured as:

$$\Delta\varphi = 2\pi\Delta t_{dmtd} \times \frac{1}{T_{beat}}$$

Where \Delta t_{dmtd} is the time between two edge-transitions in the output of DDMTD flip flops, and T_{beat} is the beat period.