OAK RIDGE National Laboratory

Controls and Interlocks

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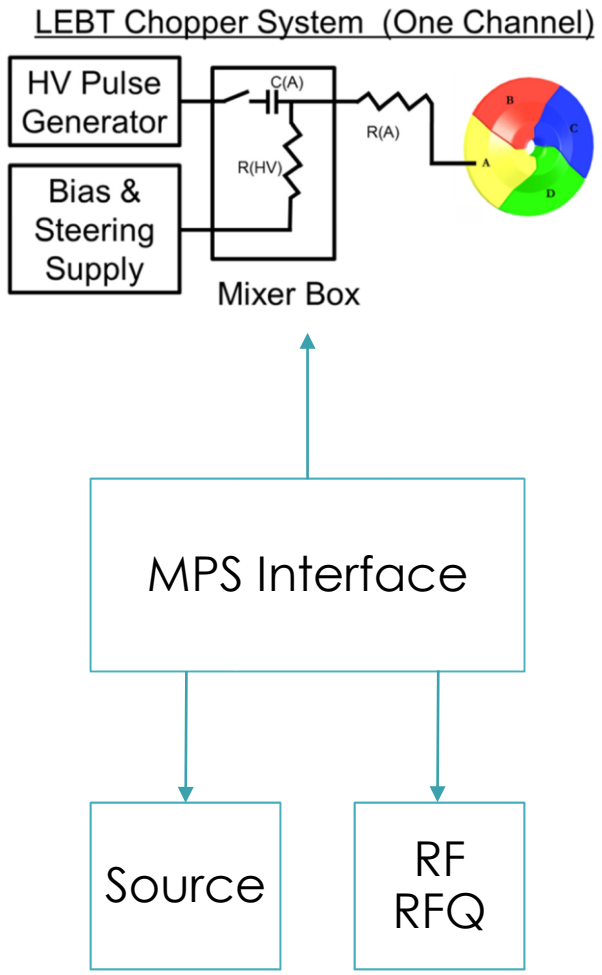
U.S. DEPARTMENT OF ENERGY

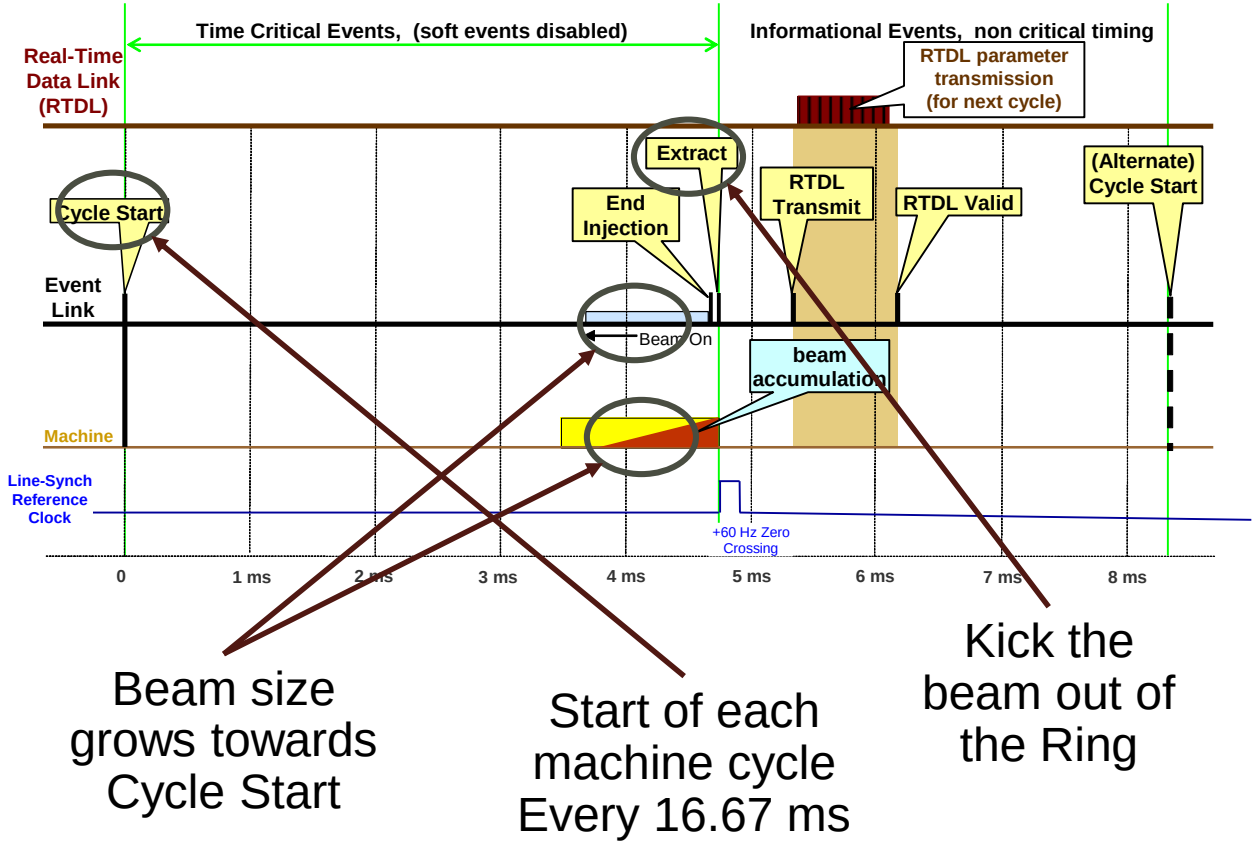
Terminating beam

- Methods for terminating beam in a Linac
  - Choppers
  - Faraday Cups
  - Shutters
  - Kickers
  - Terminate cavity and source RF
- A pulsed machine like SNS it is easy to “steal” 7-10 cycles – then return to full power
- Facilities with CW beam and cryogenic targets may not be so lucky – a slow ramp can be required to establish “production” beam again



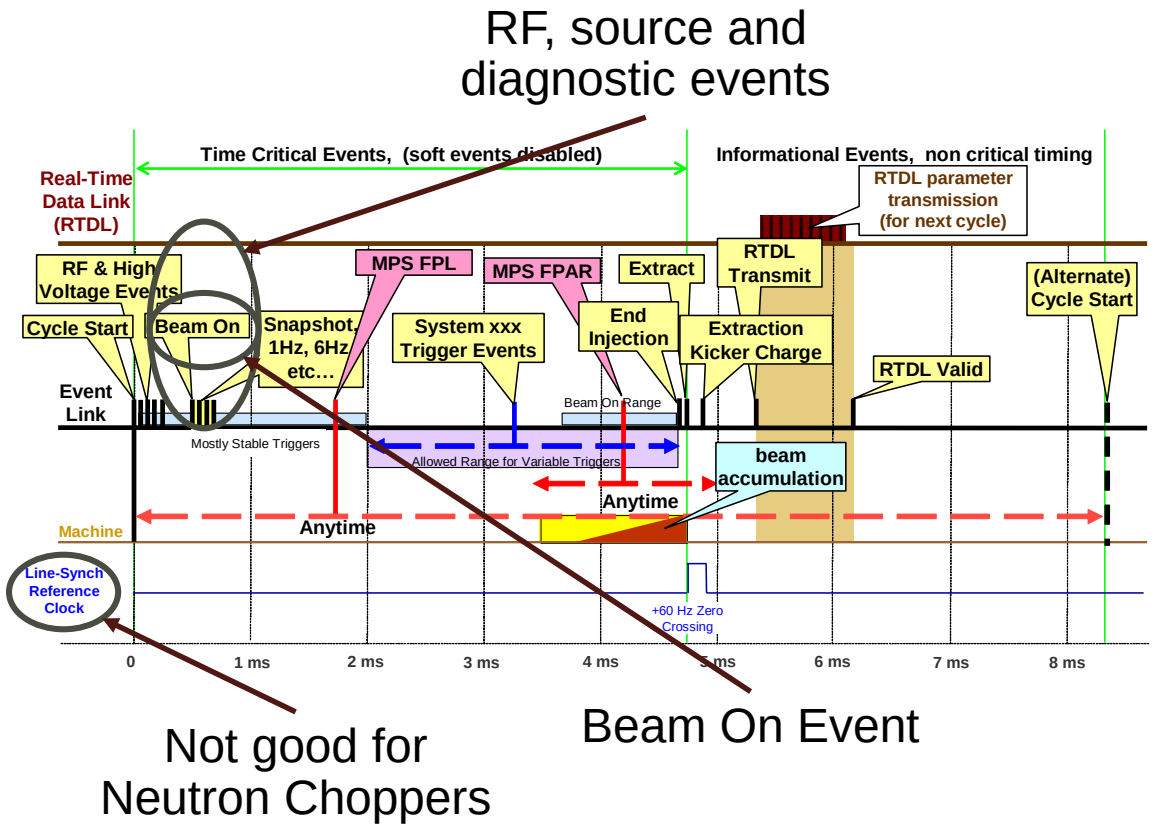
The "Machine Cycle"

- 60 Hz beam pulses
  - 16.67ms defines 1 cycle
  - A Turn is dependent on beam energy
    - 973 ns @ 850 MeV
    - 911 ns @ 1.3 GeV
- Cycle Start is t = 0
- Ring Extract is t = 5050
- Beam production stops at End of Inject, t = 5048
- Beam is extracted from the Ring at turn 5050



The machine cycle

- Beam On notifies subsystems, “this cycle is a beam cycle”
- Power grid line synchronization was terminated after commissioning
  - Caused neutron smearing at the instruments because the Neutron Choppers couldn’t keep up with the load demands at the power plants



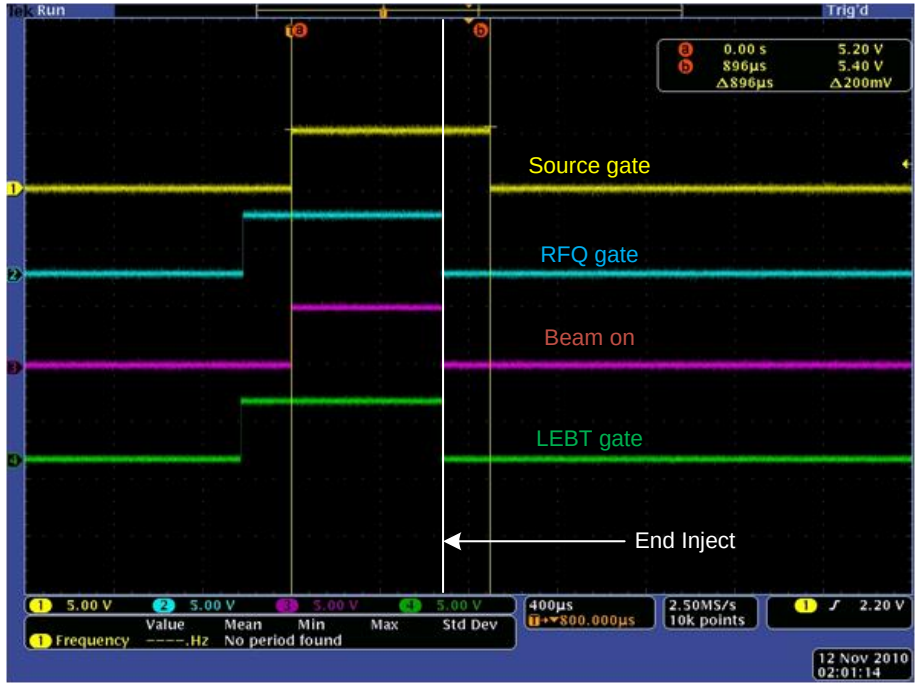
- The Event Link is a biphase mark coded bit stream that is derived from the ring clock.
  - This allows CDR (Clock and Data Recovery) circuits to create a local copy of the ring clock at the subsystem nodes for synchronization

Beam controls

- Operate source and RFQ during non-beam cycles
  - Maintain thermal stability
  - DO NOT generate beam
    - "Blanking cycles"
      - i.e. < 60 Hz
    - MPS "faulted" states
  - Shift gates in time
    - Pulsed machine
  - Kickers/shutters
    - CW machine

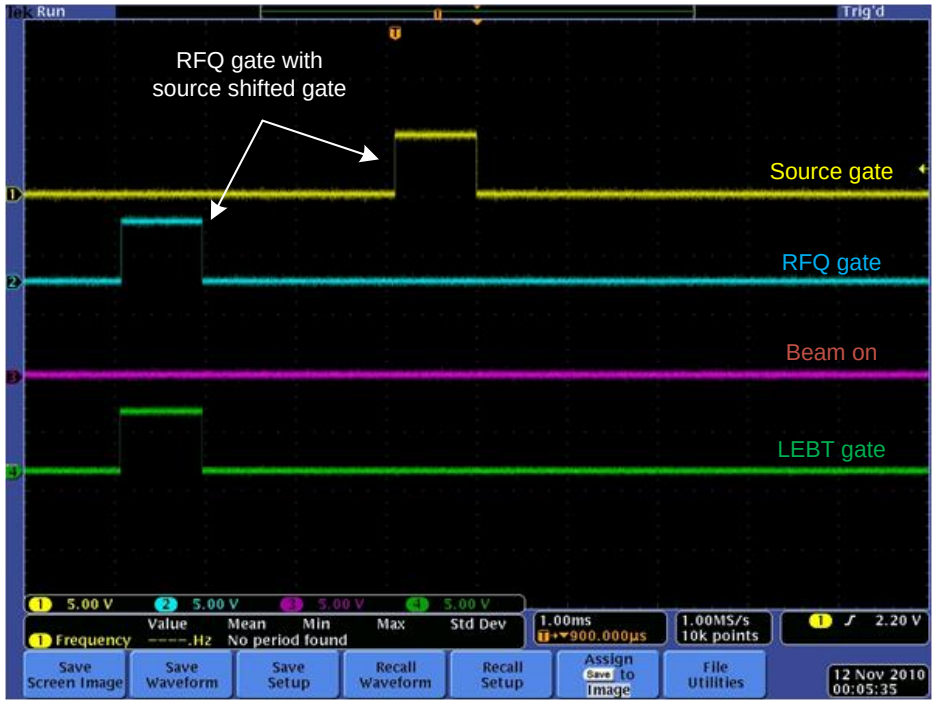
Normal beam operations "Beam On"

Source operates while the RFQ is active, beam is accelerated through the RFQ and into the Linac



Source shifted operations "Beam Off"

Source operates almost 3 ms after the RFQ is active, beam is not accelerated and is lost in the RFQ structure



End of Inject: Timing Event that determines the "end" of an SNS Machine Cycle

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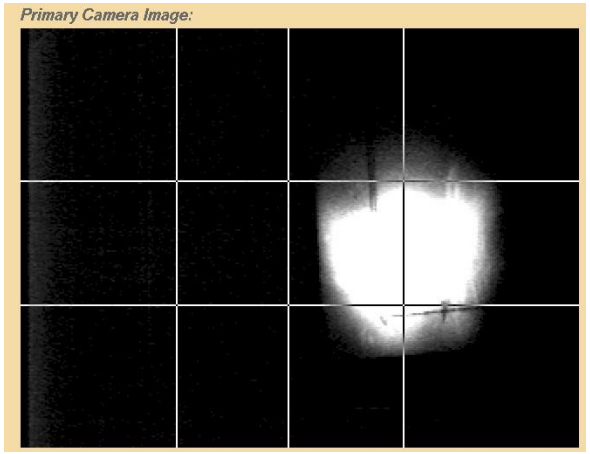
Beam controls

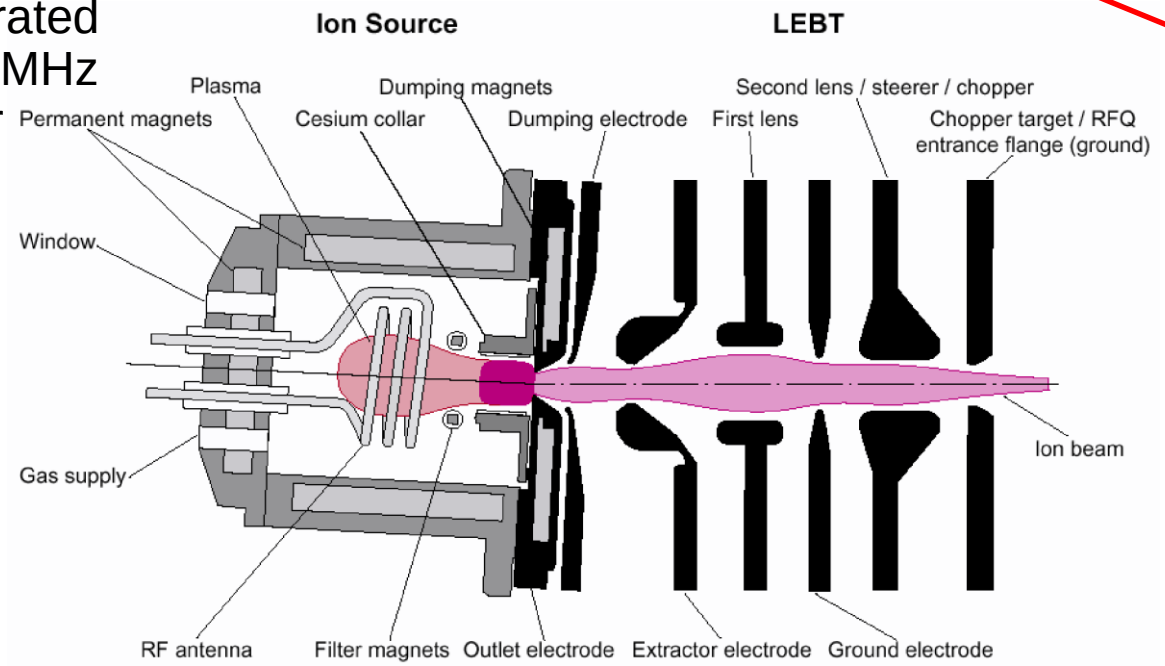
- DTL1 180° phase shift
  - Mitigate accelerating low leakage currents in the Linac, ~3 uA while the RFQ is on
  - Reduces heating in the SCL cavities
  - Eliminated in the 1st warm RF structure

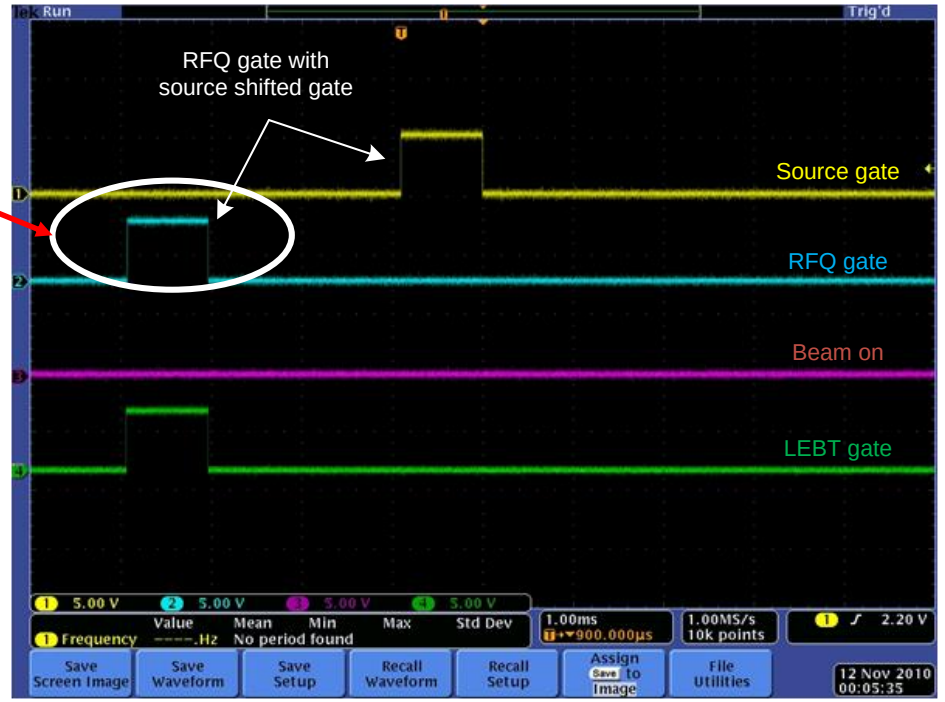


Dark current seen using a view screen

~300 W 13.56 MHz continuous RF generates a low power plasma

High beam current pulses are generated by a 50-70 kW 2MHz RF amplifier





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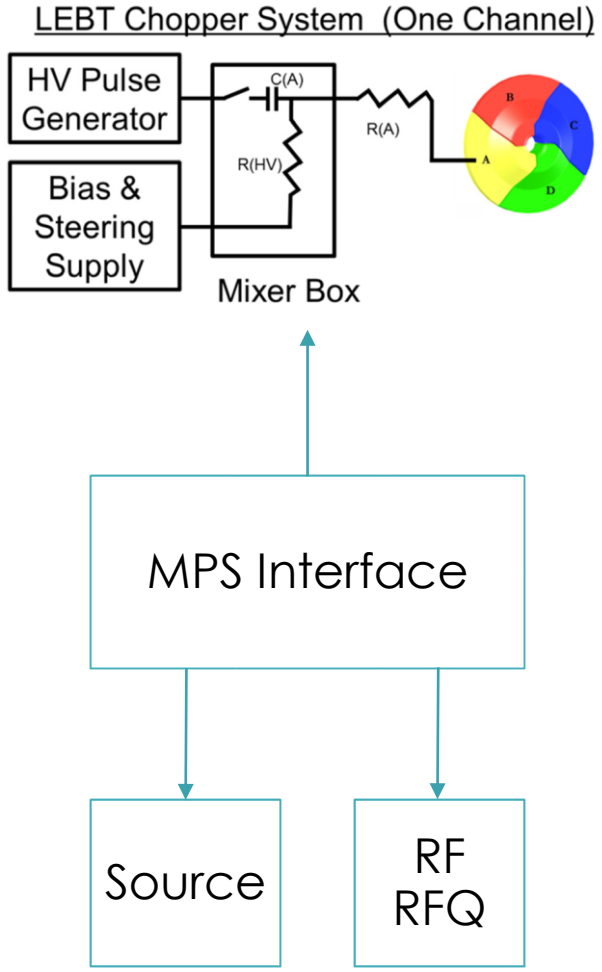
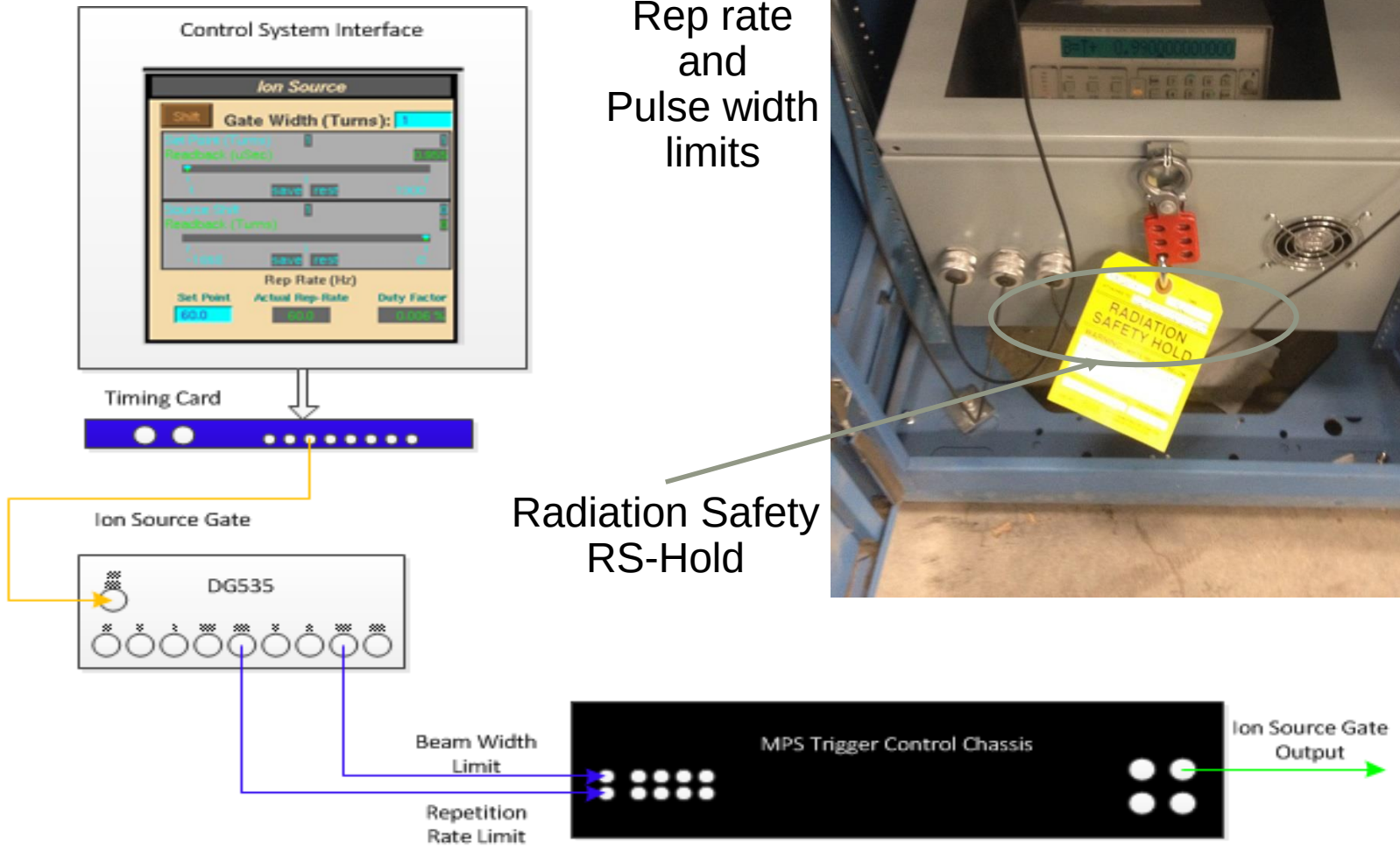
Beam controls



- Set Chopper to ”full chop” during beam blanking cycles
  - Use the LEBT Chopper to “blank” out shifted Ion Source pulses, up to 20 Hz
    - >20 Hz increases the likelihood of damaging LEBT Chopper Target with increased heat load
  - Reduce contamination of the RFQ

Protection by equipment lock-down

- Another method to limit beam pulse is to lock down certain control parameters
- At SNS, operations staff manually set a gate generator in the Front-end building to limit the ion source beam pulse length
  - The pulse can be < but not > than this setting, truncated by the DG535

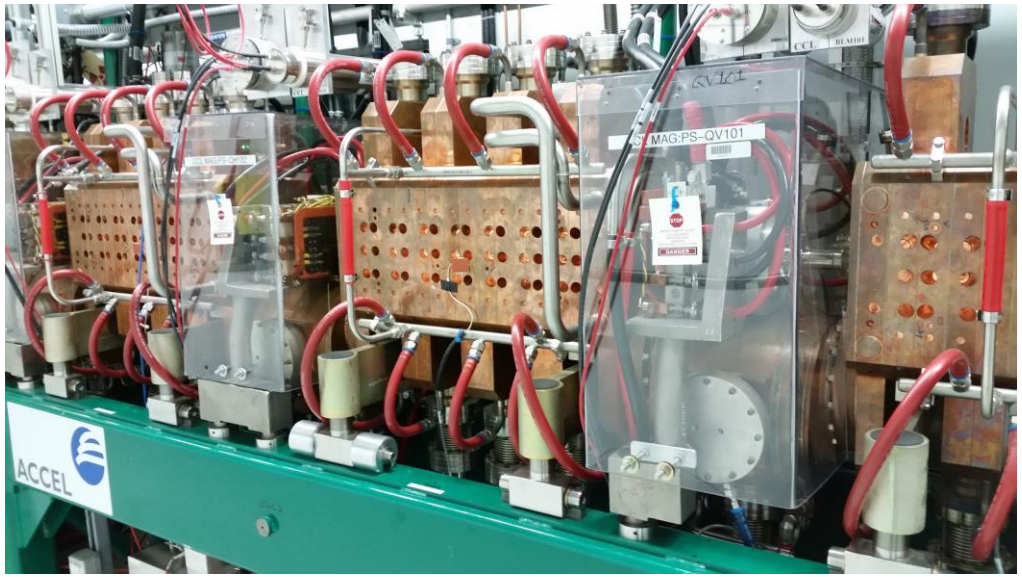


DG535
Rep rate
and
Pulse width
limits

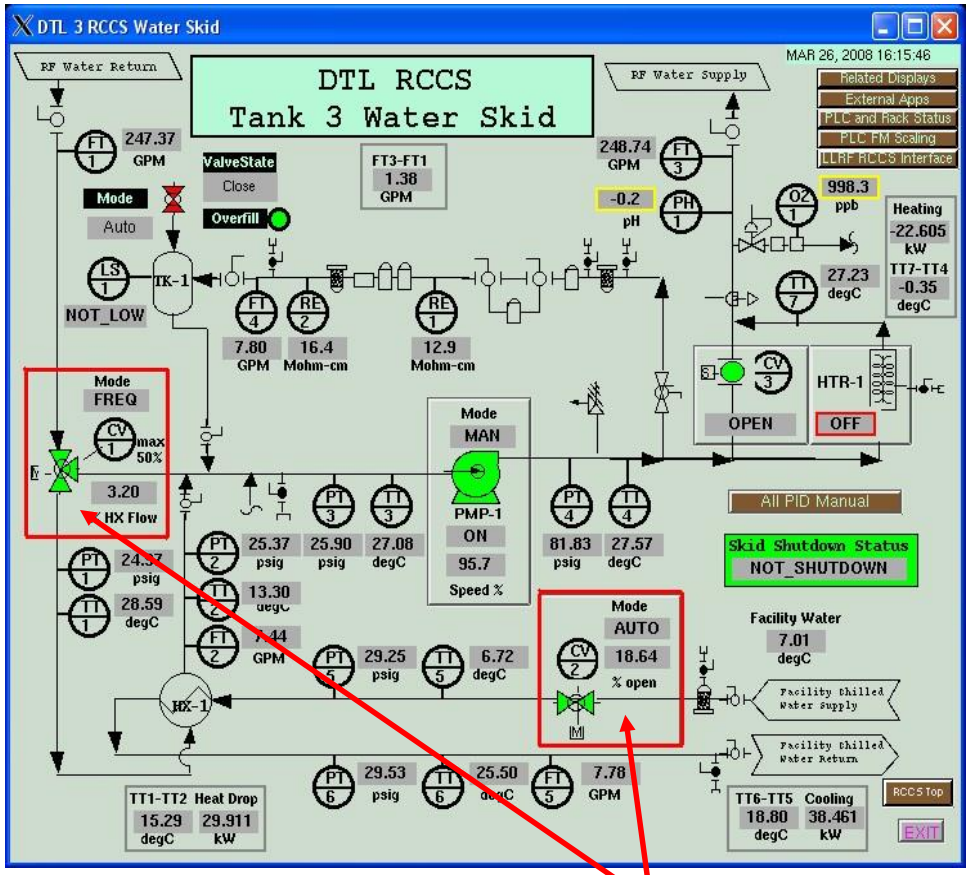
Radiation Safety
RS-Hold

Beam Controls

- Warm Linac Resonance Control Cooling System (RCCS)
- Provide thermal stability for resonance control to reduce beam losses
- 10 system, one for each set of warm cavities
  - 6 DTL
  - 4 CCL



SNS CCLs



Hot and cold flow valves

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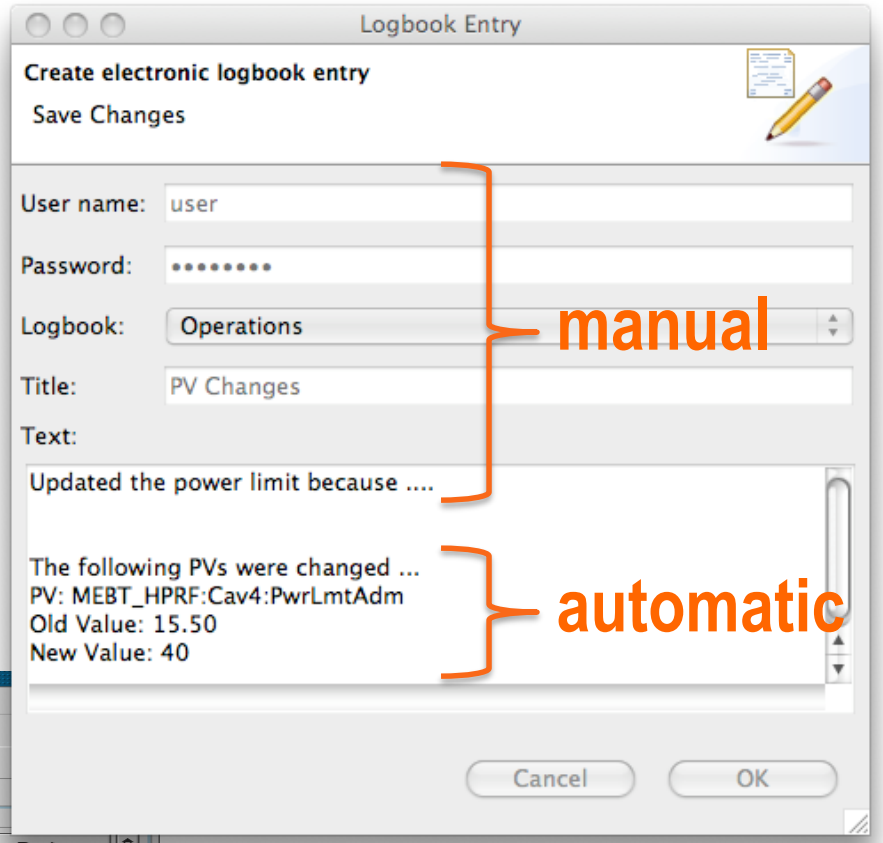
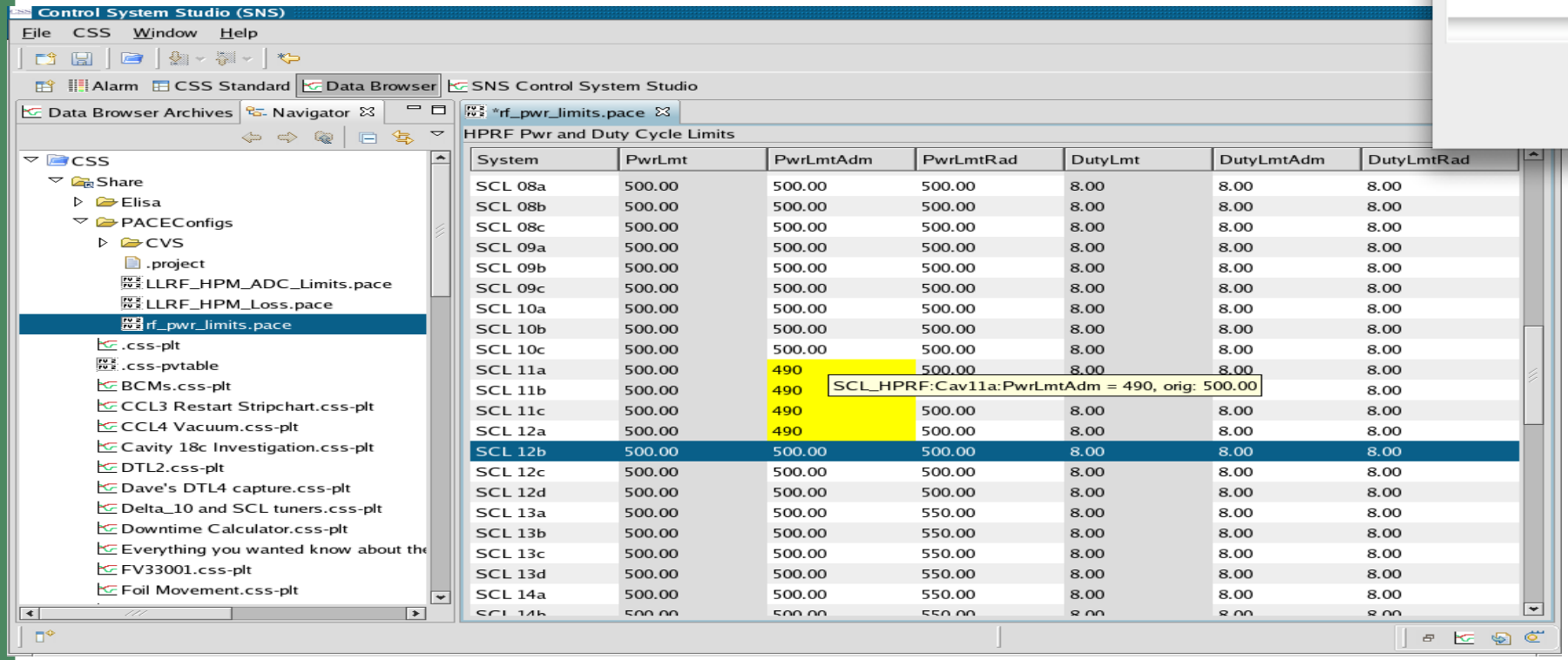
PACE

- PACE (PV Adjust Confirm E-log)
  - EPICS (Experimental Physics and Industrial Control System)
  - Applied to critical control parameters

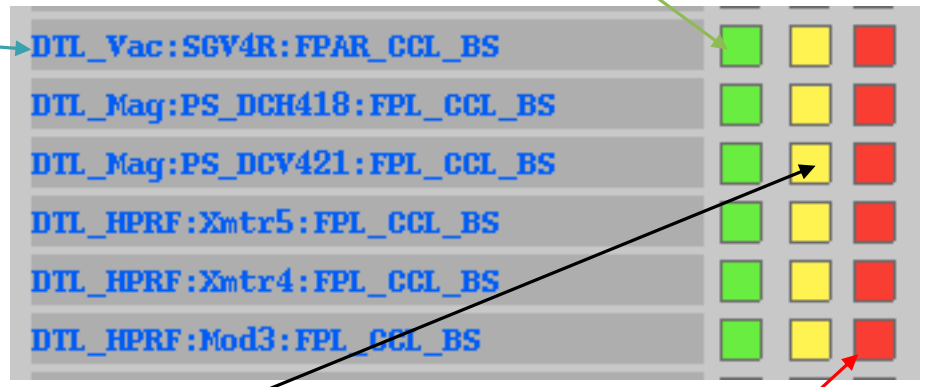




System	PwrLmt	PwrLmtAdm	PwrLmtRad	DutyLmt	DutyLmtAdm	DutyLmtRad
SCL 08a	500.00	500.00	500.00	8.00	8.00	8.00
SCL 08b	500.00	500.00	500.00	8.00	8.00	8.00
SCL 08c	500.00	500.00	500.00	8.00	8.00	8.00
SCL 09a	500.00	500.00	500.00	8.00	8.00	8.00
SCL 09b	500.00	500.00	500.00	8.00	8.00	8.00
SCL 09c	500.00	500.00	500.00	8.00	8.00	8.00
SCL 10a	500.00	500.00	500.00	8.00	8.00	8.00
SCL 10b	500.00	500.00	500.00	8.00	8.00	8.00
SCL 10c	500.00	500.00	500.00	8.00	8.00	8.00
SCL 11a	500.00	490	500.00	8.00	8.00	8.00
SCL 11b	500.00	490	500.00	8.00	8.00	8.00
SCL 11c	500.00	490	500.00	8.00	8.00	8.00
SCL 12a	500.00	490	500.00	8.00	8.00	8.00
SCL 12b	500.00	500.00	500.00	8.00	8.00	8.00
SCL 12c	500.00	500.00	500.00	8.00	8.00	8.00
SCL 12d	500.00	500.00	500.00	8.00	8.00	8.00
SCL 13a	500.00	500.00	550.00	8.00	8.00	8.00
SCL 13b	500.00	500.00	550.00	8.00	8.00	8.00
SCL 13c	500.00	500.00	550.00	8.00	8.00	8.00
SCL 13d	500.00	500.00	550.00	8.00	8.00	8.00
SCL 14a	500.00	500.00	550.00	8.00	8.00	8.00

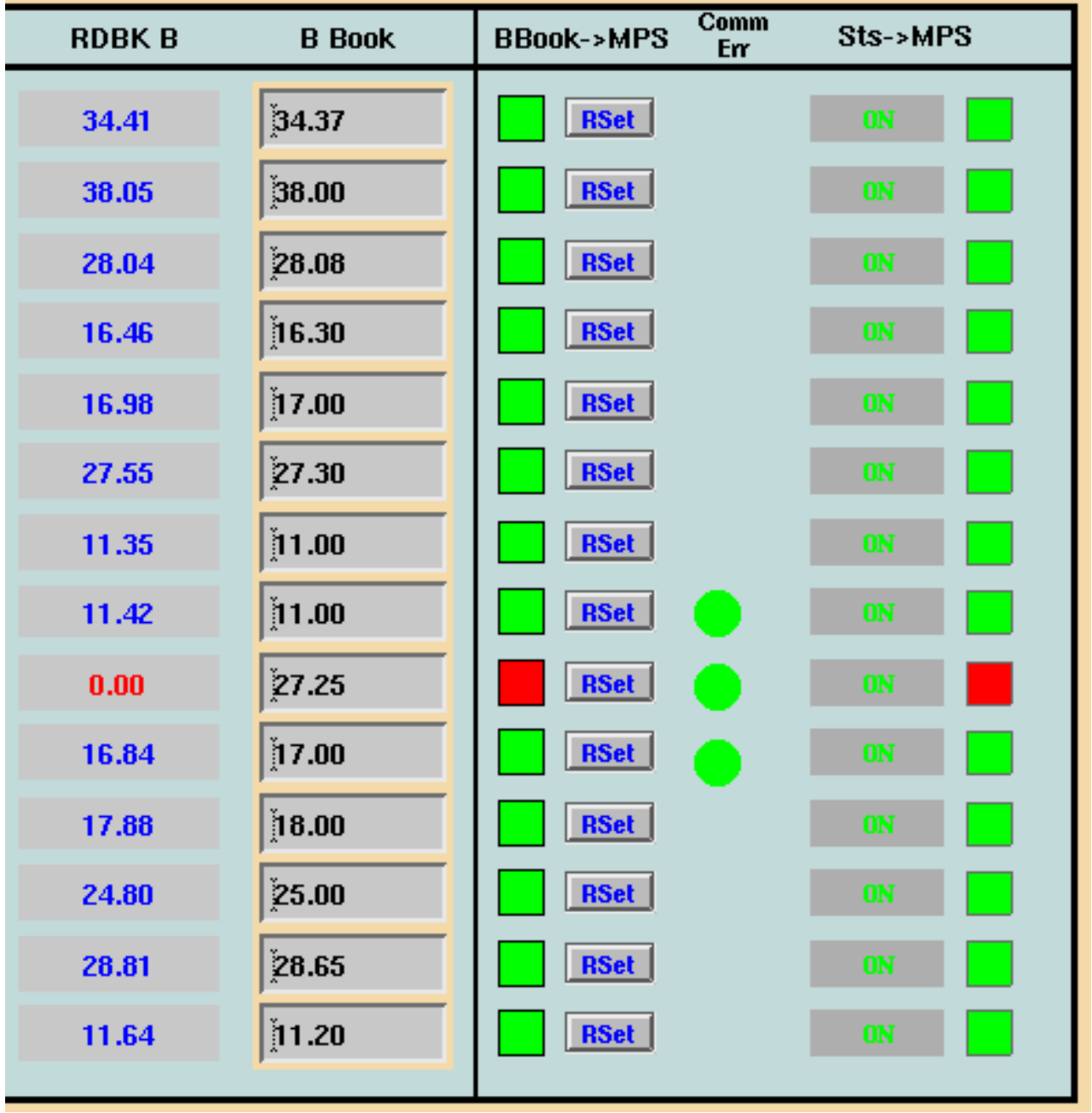
Configuration control

- SNS Beam Modes
  - 50, 100, 1mS, Full Power, Off and Standby
- SNS Machine Modes
  - MEBT BS, CCL BS, L-Dump, I-Dump, E-Dump and Target
- Configured via MPS PLC
  - Located in the main Control Room
  - Read by the Timing Master and broadcast to each node at 60 Hz
  - Verified against database before every machine cycle



Software interlocks

- Magnets
- Power Supplies
  - HV levels for BLMs
  - Power supply settings
- Chatter Fault limits
  - Auto recovery → manual recovery
- Dump Power limits
  - Combined with administrative controls
  - Injection Dump uses fast protect hardware “Nano-coulomb detector”
    - Soft interlocks are too slow in the event of a Primary Stripper foil failure



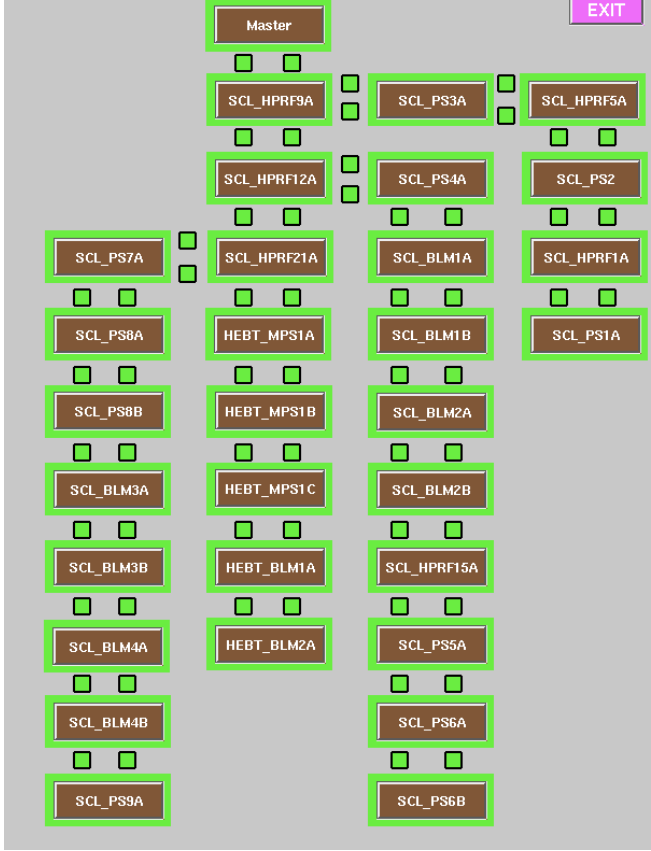
Protection by alarms

- Control system can monitor many parameters, and alert operators when these parameters stray outside of pre-defined limits
- These are separate from the automatic interlocks.
- Alarms do not automatically turn off the beam.
- Alarms may be set to alert operators before parameters reach the interlock limits, or may be set on some less rigorous parameters

User screens

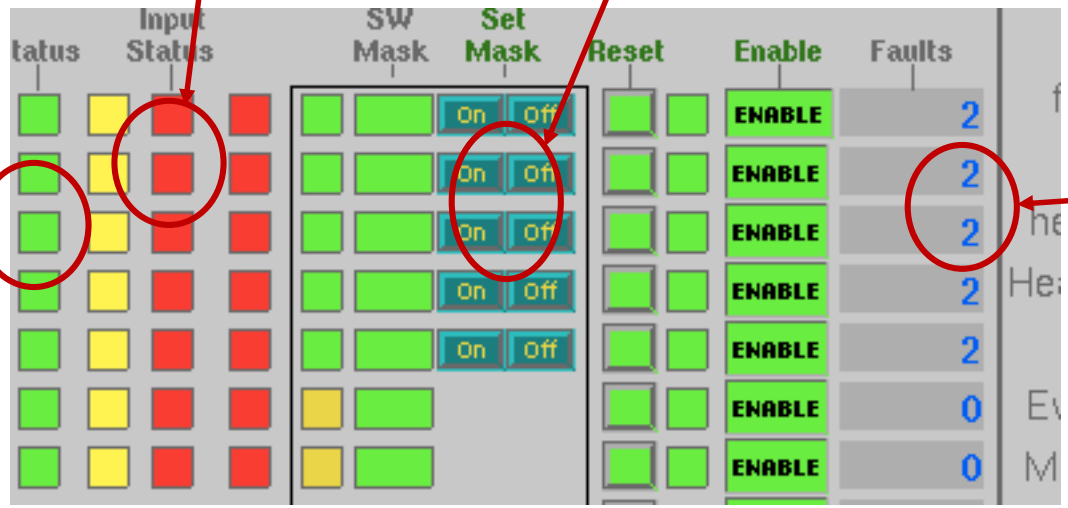
- Approximately 110 nodes at SNS
  - Without interface screens, it would be difficult to know which system reported the fault
  - Also allows operations to establish bypass settings

Overview of the SCL



The input status reflects faulted Input channel

Bypass Enable/disable



Fault counters

The channel status is green because the Machine Mode is upstream of this location

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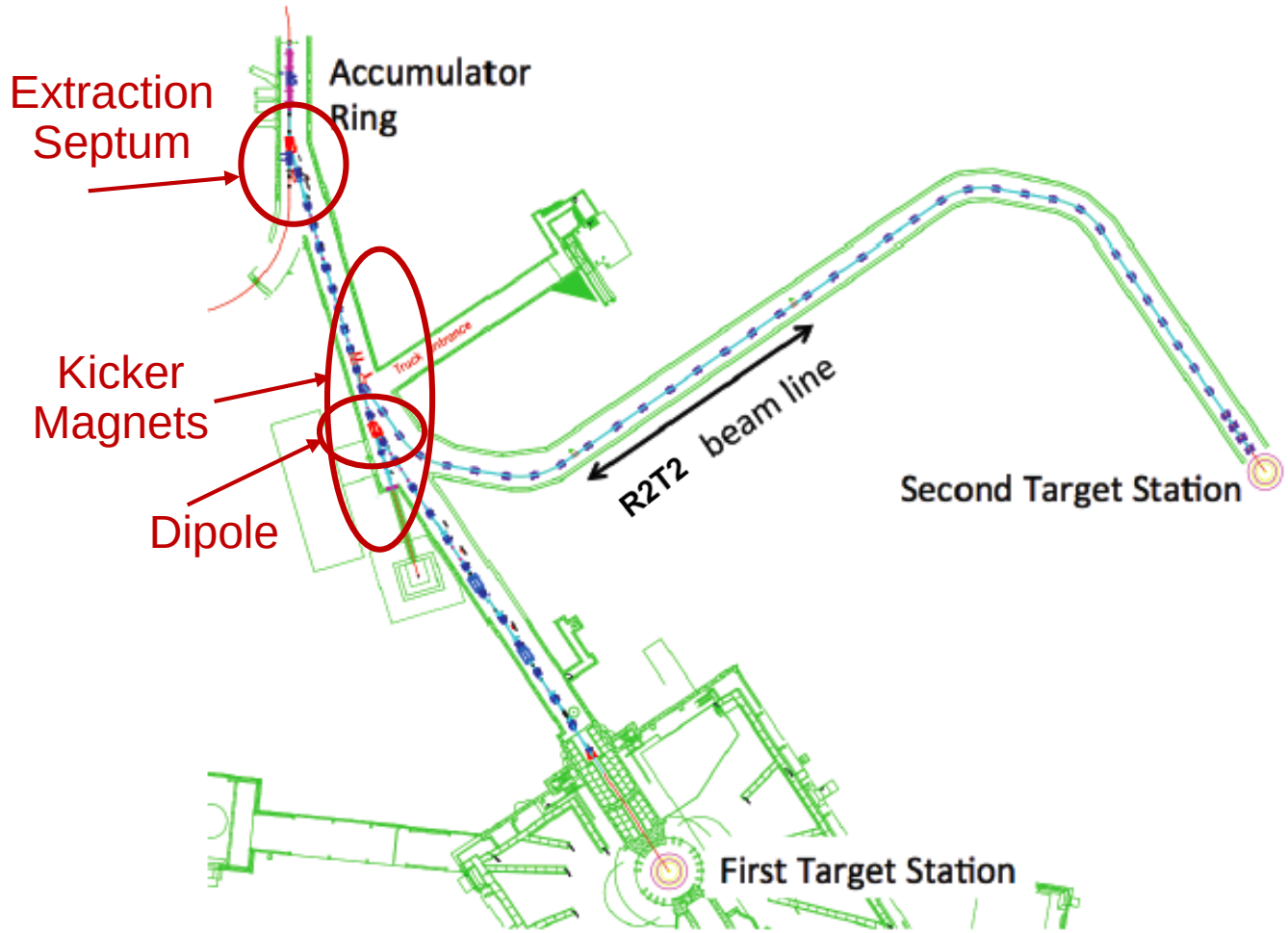
Moving forward STS

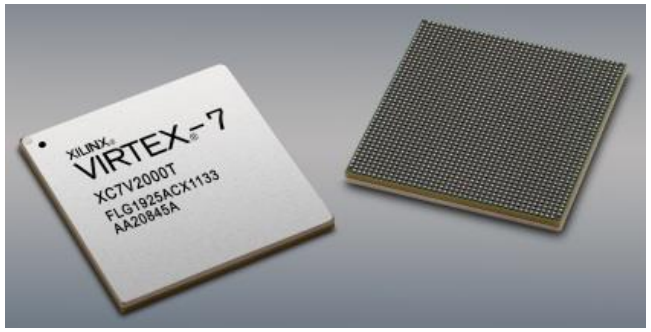
- Second Target Station (STS)
- Single pulse configuration
  - Two pulse configuration for STS (Second Target Station)
  - STS 10-20 Hz
    - 47 kJ per pulse
- Kicker magnet interface
  - Beam must go to STS



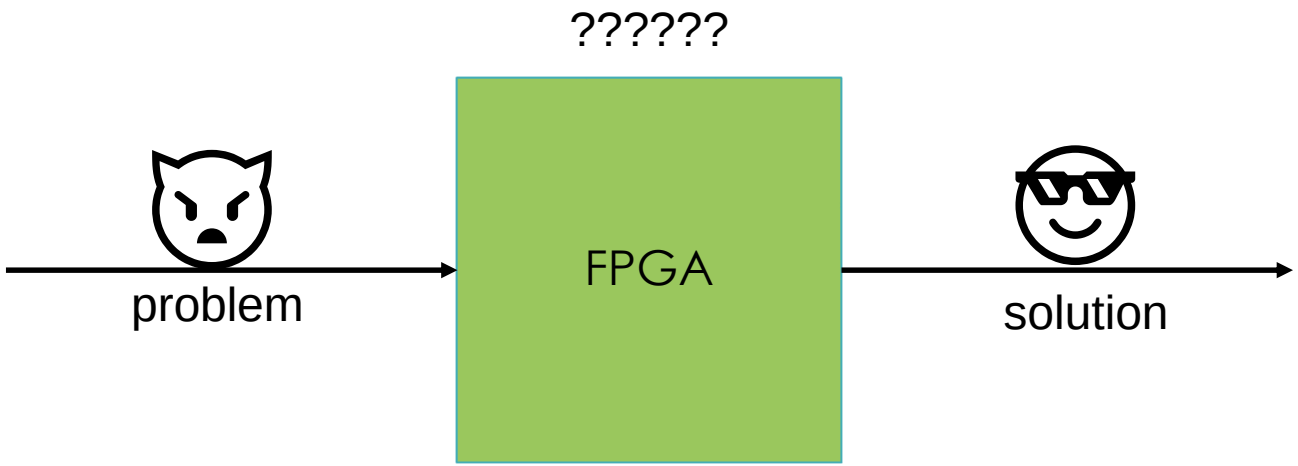
- Example: What level of effort should be spent protecting the FTS beam when a fault occurs on the STS beamline?
  - A fault occurs in the R2T2 transport line or target. It is desirable to not disrupt beam to the FTS. This requires coordination between the Timing System and MPS to ensure only STS cycles are disrupted.

Implementing interlocks

- Microcontroller design
  - PLCs “Slow Interlocks,” milliseconds
  - Software “Soft Interlocks,” seconds
- Discrete Components, microseconds
  - ICs
  - FPGAs
  - CPLDs
- Varying levels of reliability
  - Failure methods plague all types



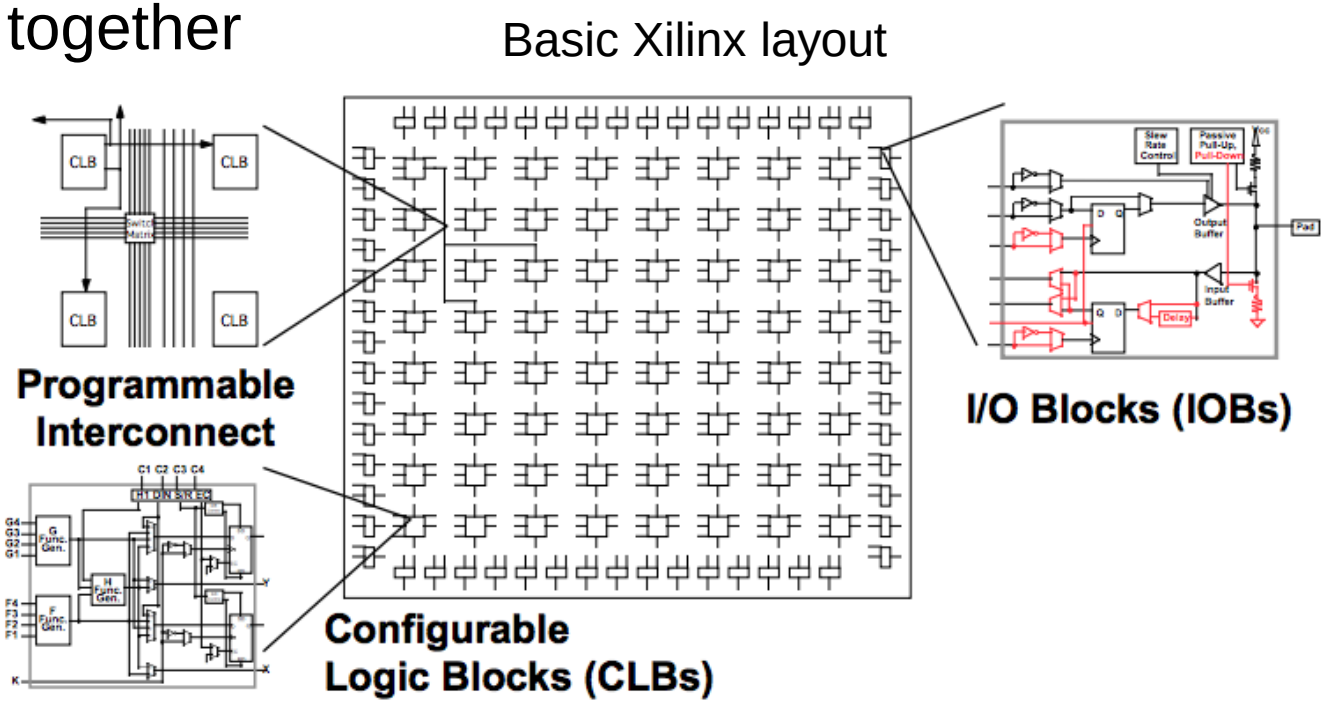
The Magic FPGA



FPGA
(Field Programmable Gate Array)

FPGA "basic" SRAM architecture

- Logic Blocks
  - 4 input LUT (look up table)
- Programmable Interconnect
  - Routing configurable resources together
- I/O pins
  - Configurable and fixed types
- Internal RAM
- External Flash
  - Device program storage
- SRAM type, most common
- Anti-fuse/Internal Flash, heavy in defense and aerospace



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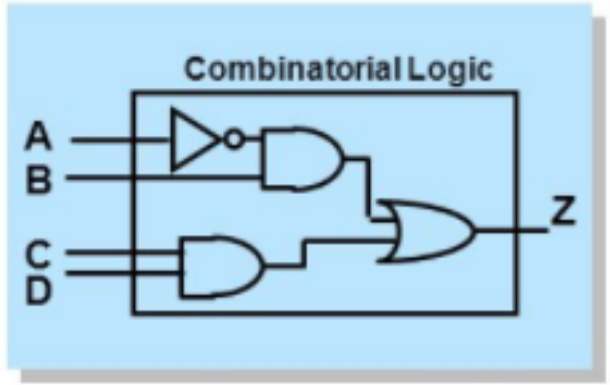
FPGA architecture

- Size metrics
  - Flip Flops (registers, bit storage)
  - LUTs
  - RAM blocks
- No logic gates internally
  - Functions are translated into Look Up Tables
- LUT (Look Up Table)
  - DFF (D-type Flip Flop)
  - Mux



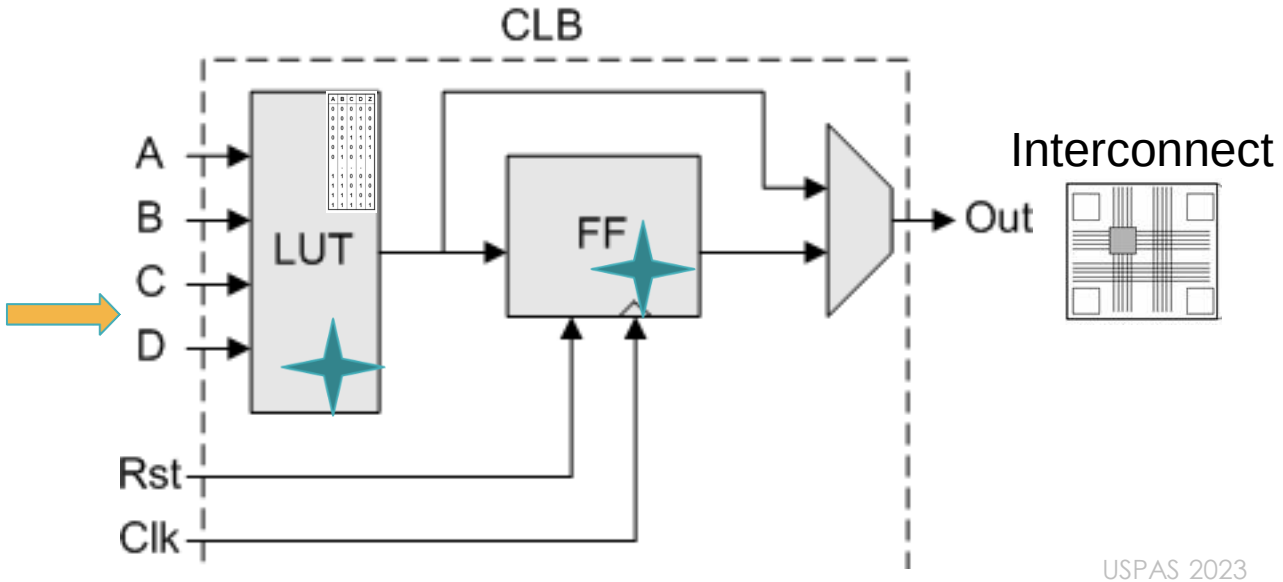
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Entire resource is consumed if any of its elements are used

**This is no longer true in modern day devices

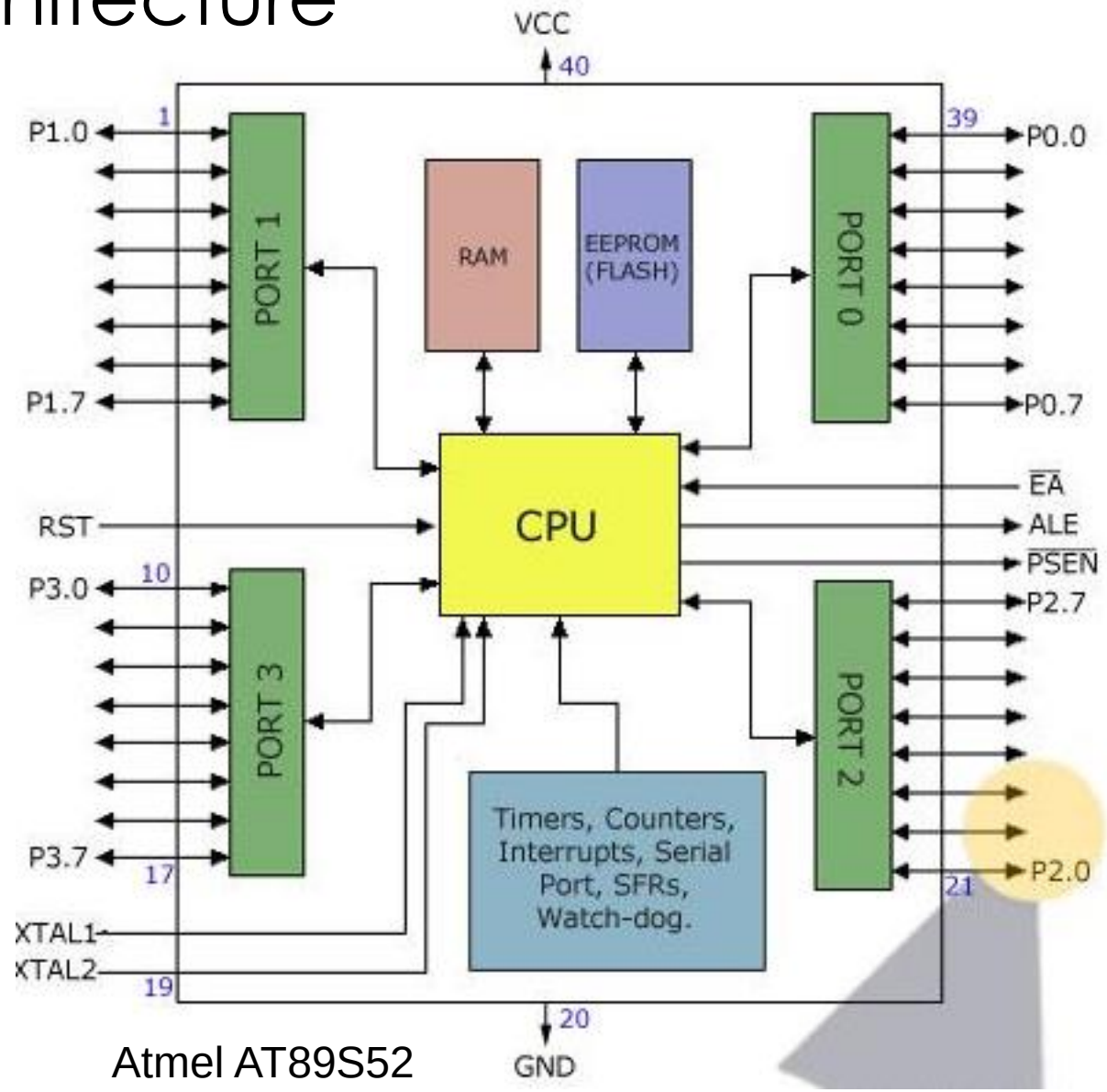
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Xilinx simplistic view of LUT configuration



Microcontroller “basic” architecture

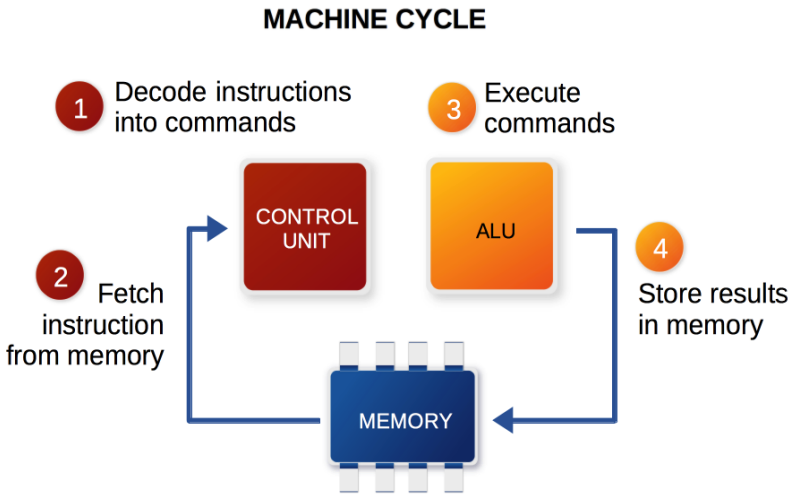
- CPU
  - Central Processing Unit
- Shared bus(es)
- RAM and Flash
  - Boot-up Instruction storage
  - Program storage
- External I/O
- Instruction/Data Cache
- Other interfaces
- Intel and PowerPC

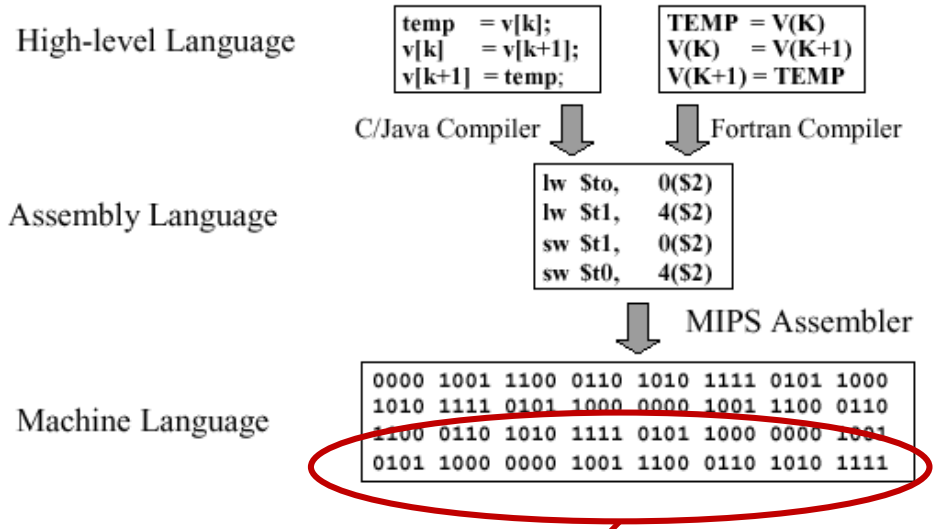


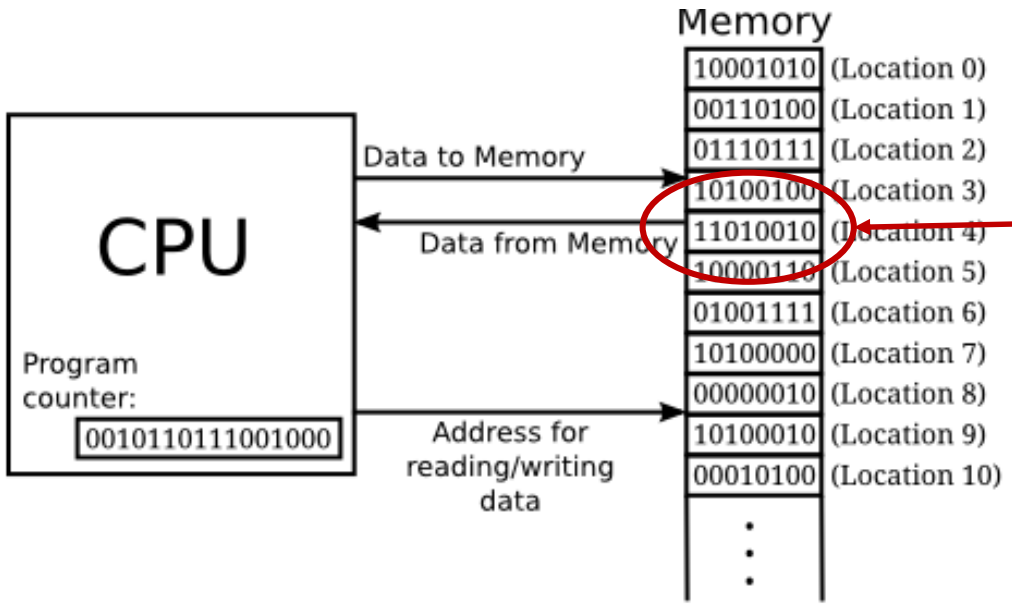
Atmel AT89S52

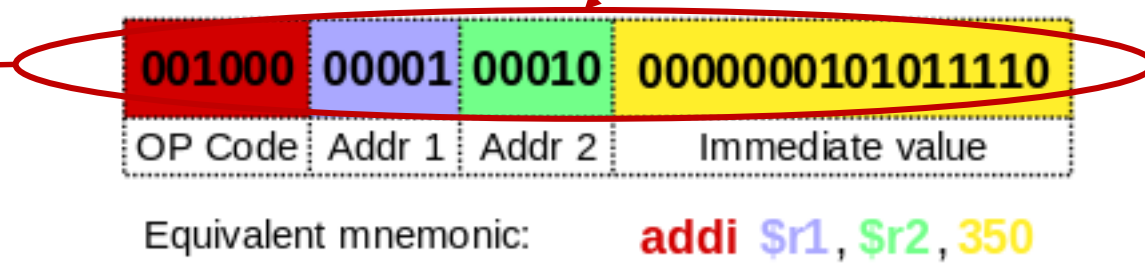
Basic CPU example

- 1GHz clock
- Perform 1 step per clock cycle
  - Intel
- “Execute commands” occur at 250 MHz!!!









Equivalent mnemonic: **addi $r1, $r2, 350**

Add the immediate value to the value stored in address location 2 and store that result in address location 1

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Basic similarities

- Flash to store programs
  - uC typically local, FPGA typically external
  - On Power up, programming functions are loaded
- Clocking resources (synchronous devices)
- User Configurable, one to many times, flash dependent not device dependent
- Susceptible to ”event upsets”
  - SEU, MEU, … several classifications depending on the failure type
- Radiation hardened devices
  - Level of ”hardening” varies significantly
- Modern day devices are highly complex architectures

Basic differences

Microcontroller

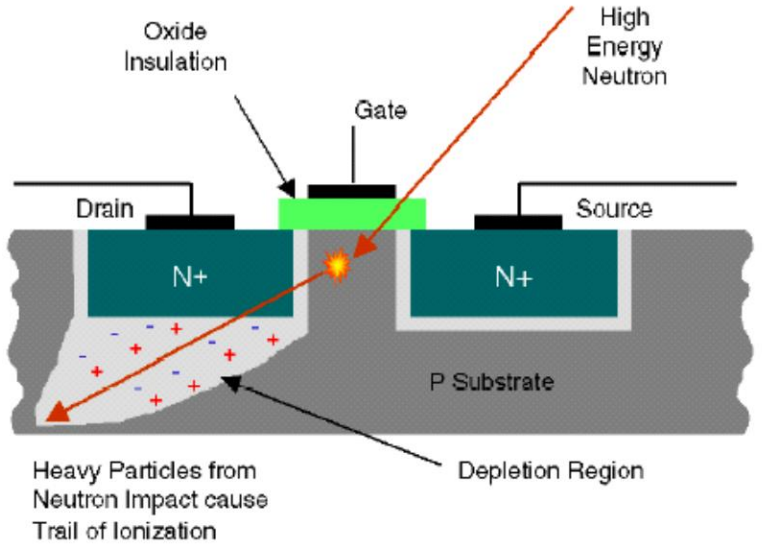
- Single process execution (time slicing)
- GHz clocking speeds
- Dynamic program configuration
- Operating Systems
- Broad user community
  - Plethora of programming languages
  - Compile and go…

FPGA

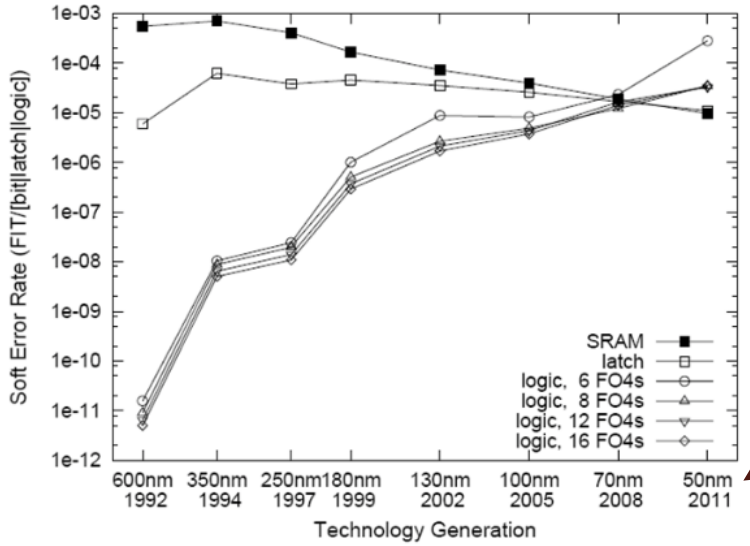
- Massive Parallel Processing
- MHz clocking speeds
- Fixed program configuration
- Direct programming
- Limited user community
  - Concurrent programming languages
  - Timing constraints, PLL configuration, …

Single Event Effects (SEE)

- SEU, MEU (Multi) Single Event Upste
- SEFI – Single Event Functional Interrupt
  - Can be repairable in real-time, depending on location and device
- SEL – Single Event Latch Up
  - Fixed by power cycling the device
- SEB – Single Event Burnout
  - Permanent damage, non-repairable

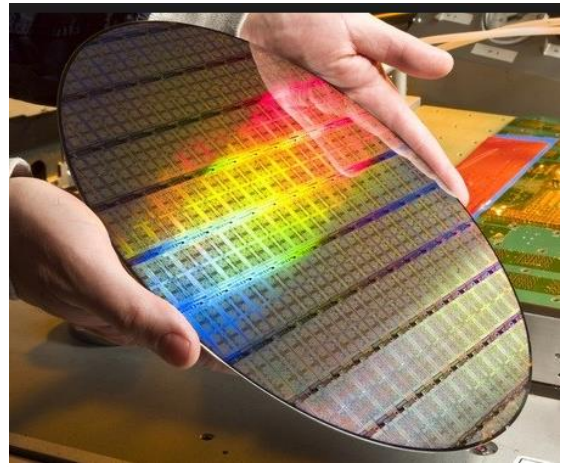


SER
Soft Error Rate



2017
14 nm

2022
7 nm



Moor's Law
transistors double per
unit area every 2 years

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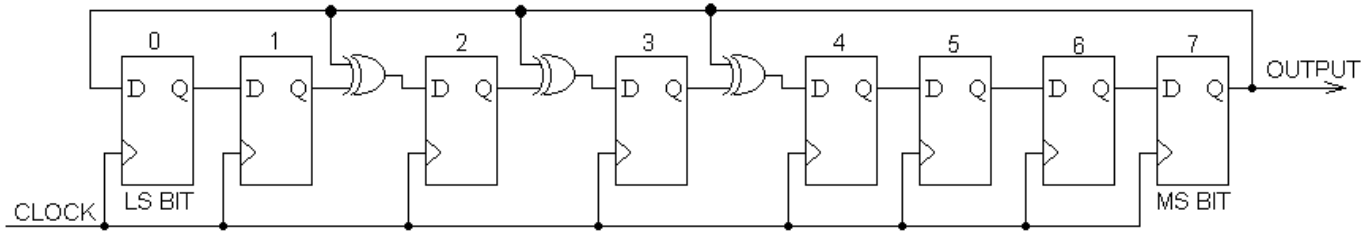
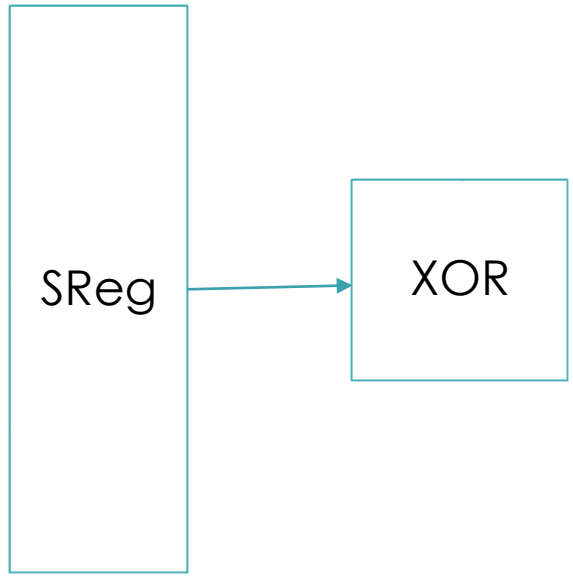
Error detection

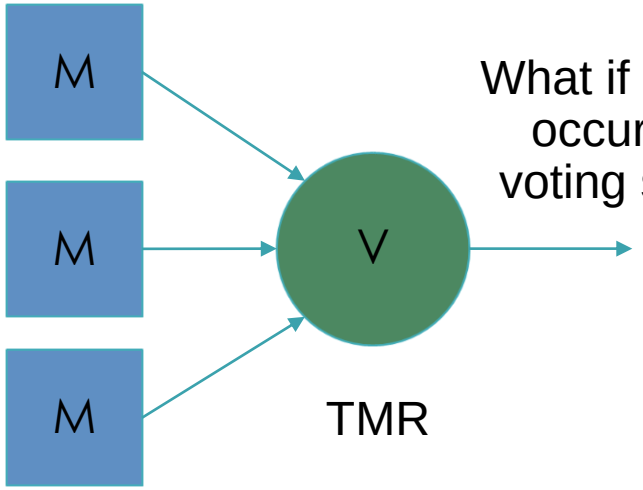
- FSM (Finite State Machine)
  - Encode “one-hot”
  - Run the State Register through an XOR gate
- CRC (Cyclic Redundancy Check)
  - CRC “Sum” is transmitted with data
- TMR (Triple Modular Redundancy)
  - Can be implemented internal to an FPGA
  - Multiple devices feeding a PLC
  - Etc…



CRC



Single bit error detection method



TMR

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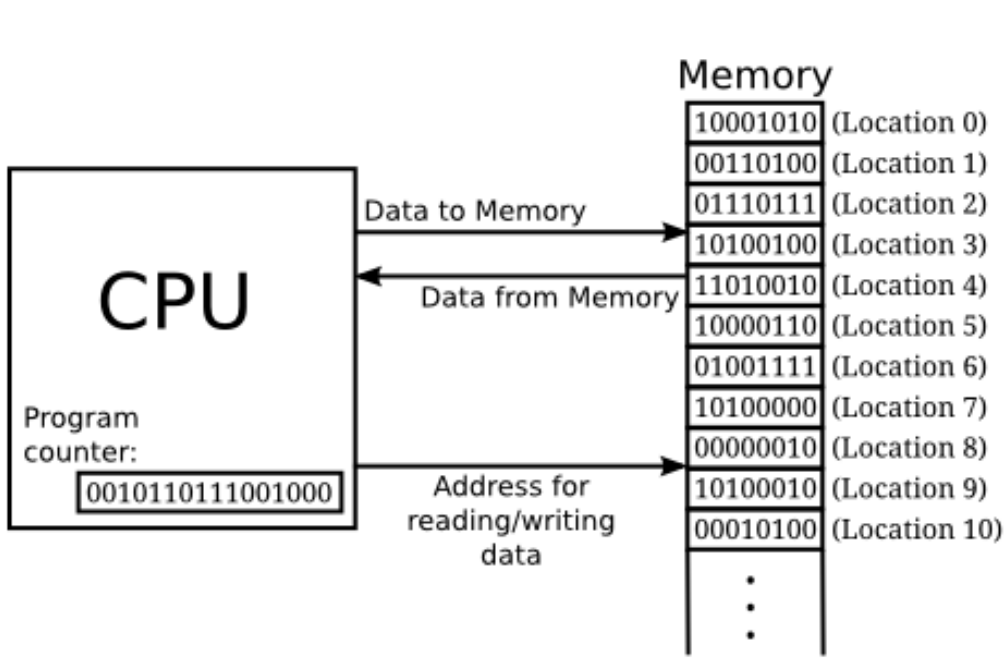
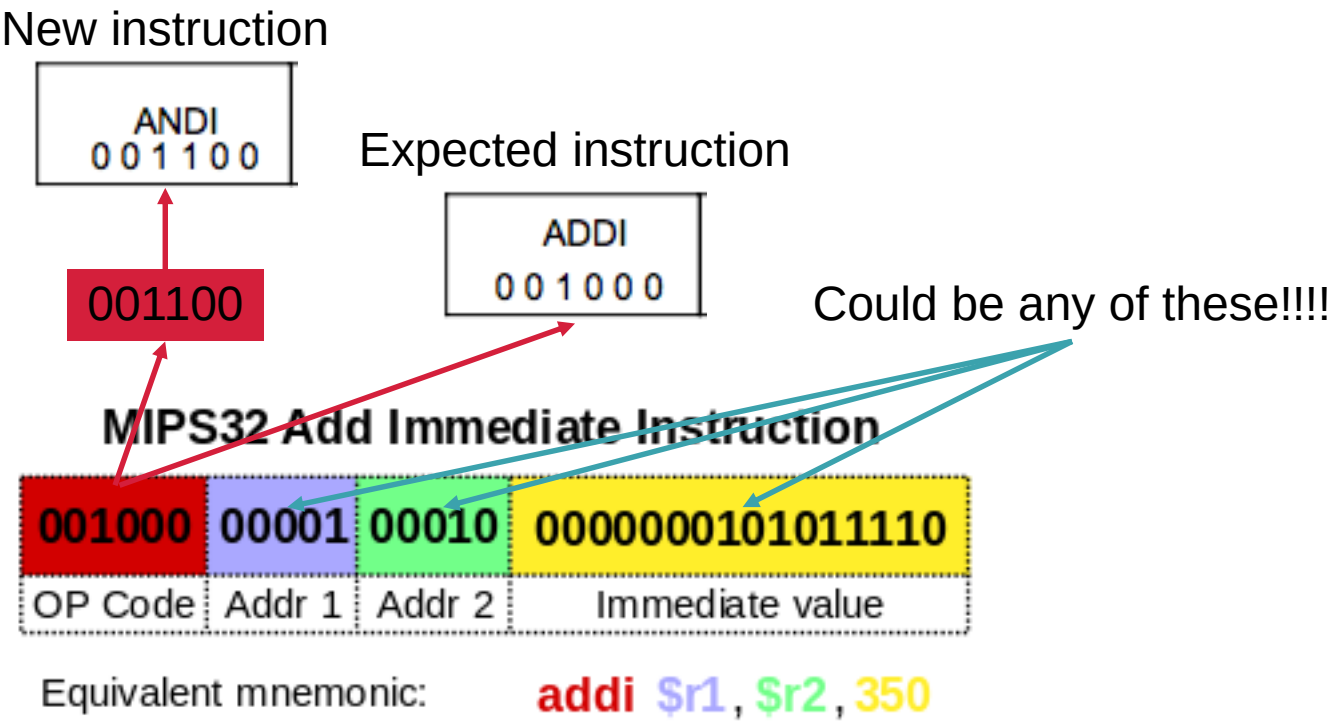
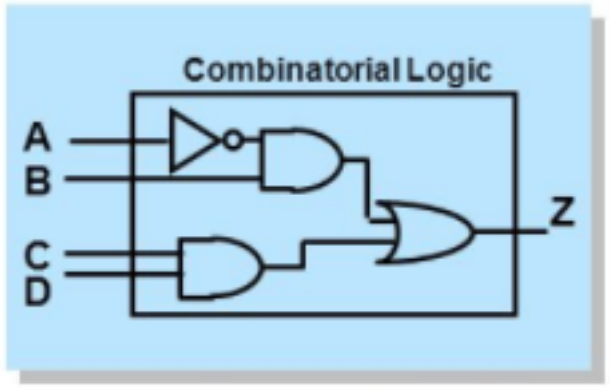
CPU SEU example

- ADDI “Add Immediate” becomes ANDI ”logical AND Immediate”
- This example applies to address or value registers as well
- What if this was a branch or jump command?





FPGA SEU example

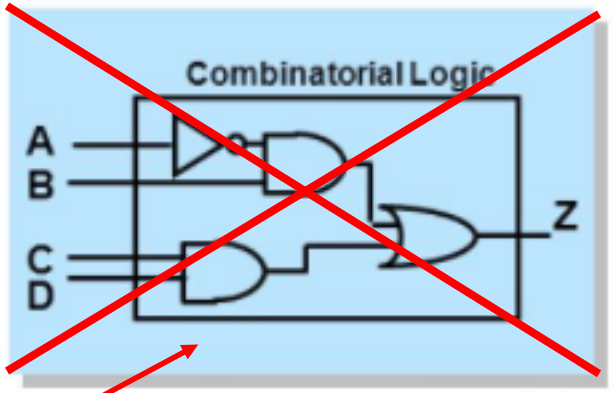


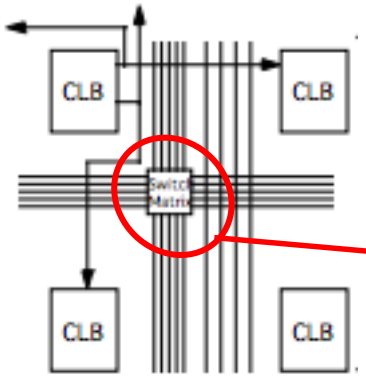
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

X

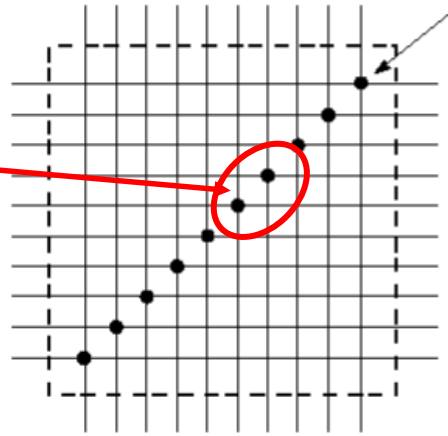
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
0	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

X





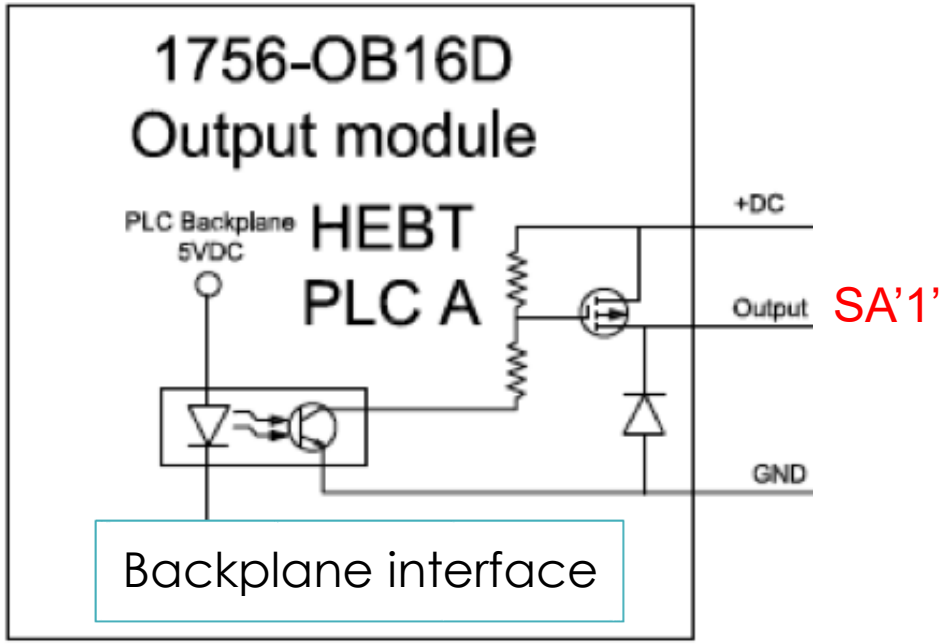
Programmable switch matrix



- Utilize CRC capabilities of programmable devices
- Usually requires partial to full reconfiguration of the device
  - This can be an automated process
  - For Interlocks, it will likely be better to notify and take no immediate action

Other failure modes

- Stuck at ‘1’/‘0’ (high/low)
  - Doubled Digital I/O as SNS for PLC interfaces (SA1) ”MPS Good”
    - SNS Vacuum Interface
    - Electrical overload during maintenance created permanent damage to the output gate
  - Gated Clock “MPS Good”
    - SNS MPS Hardware failure
    - Firmware doesn’t match final design requirements
      - Does your organization consider firmware software or hardware?
      - Are firmware changes subject to DCN (Design Change Notification) process?
        - What if it’s part of an interlock system???

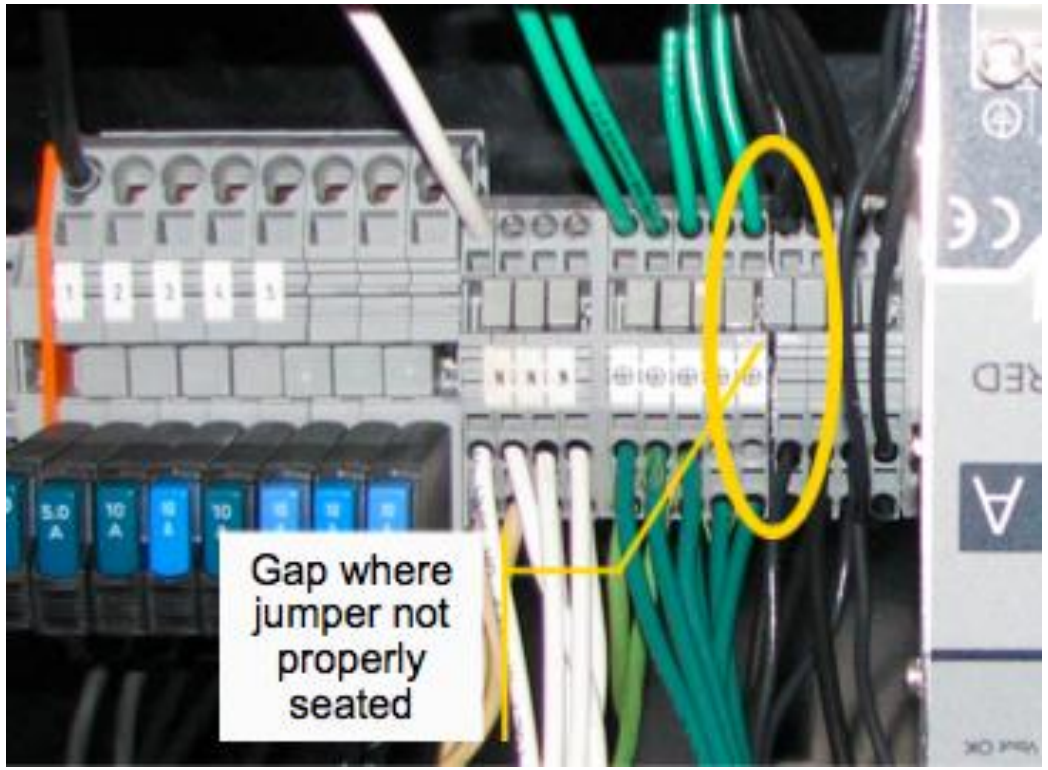


Protection system grounding error

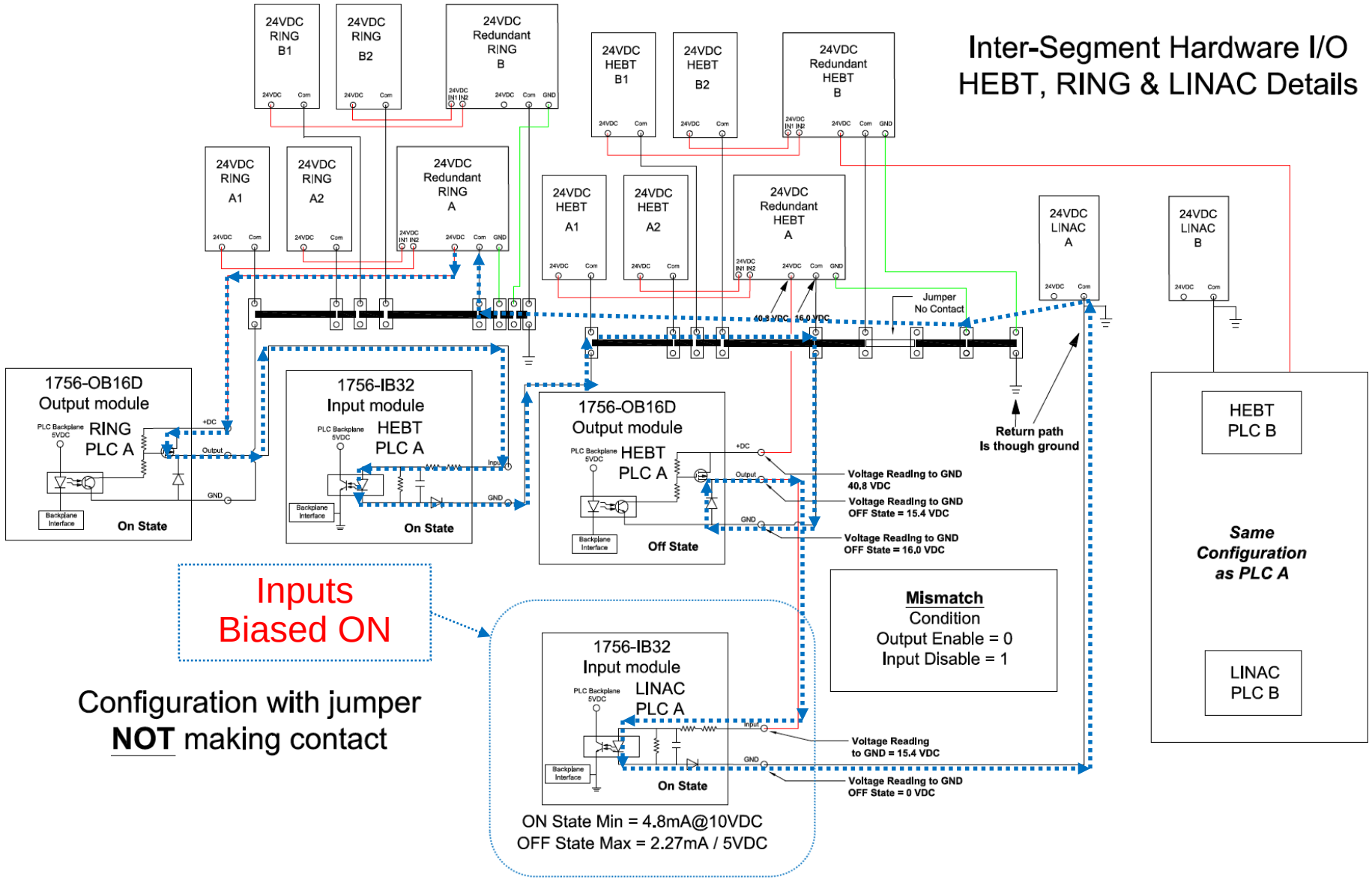
- April 2013 - Modification to add redundant power supplies to increase availability
  - Inter-segment handshaking not tested as part of installation QA or post modification tests
- Error found July 31, 2013 during annual certification testing
  - Under certain conditions, PPS would not have shut off the front end for a downstream fault
  - Common mode error affected both of the redundant chains
  - Unintended result of modification to PPS systems to add redundant power supplies
  - Beam Operations halted until mitigating measures in place
    - It took 9 days before receiving a letter of resumption from DOE
  - Failure mode identified and replicated on bench
    - Very complicated failure mode

Accelerator PPS grounding error

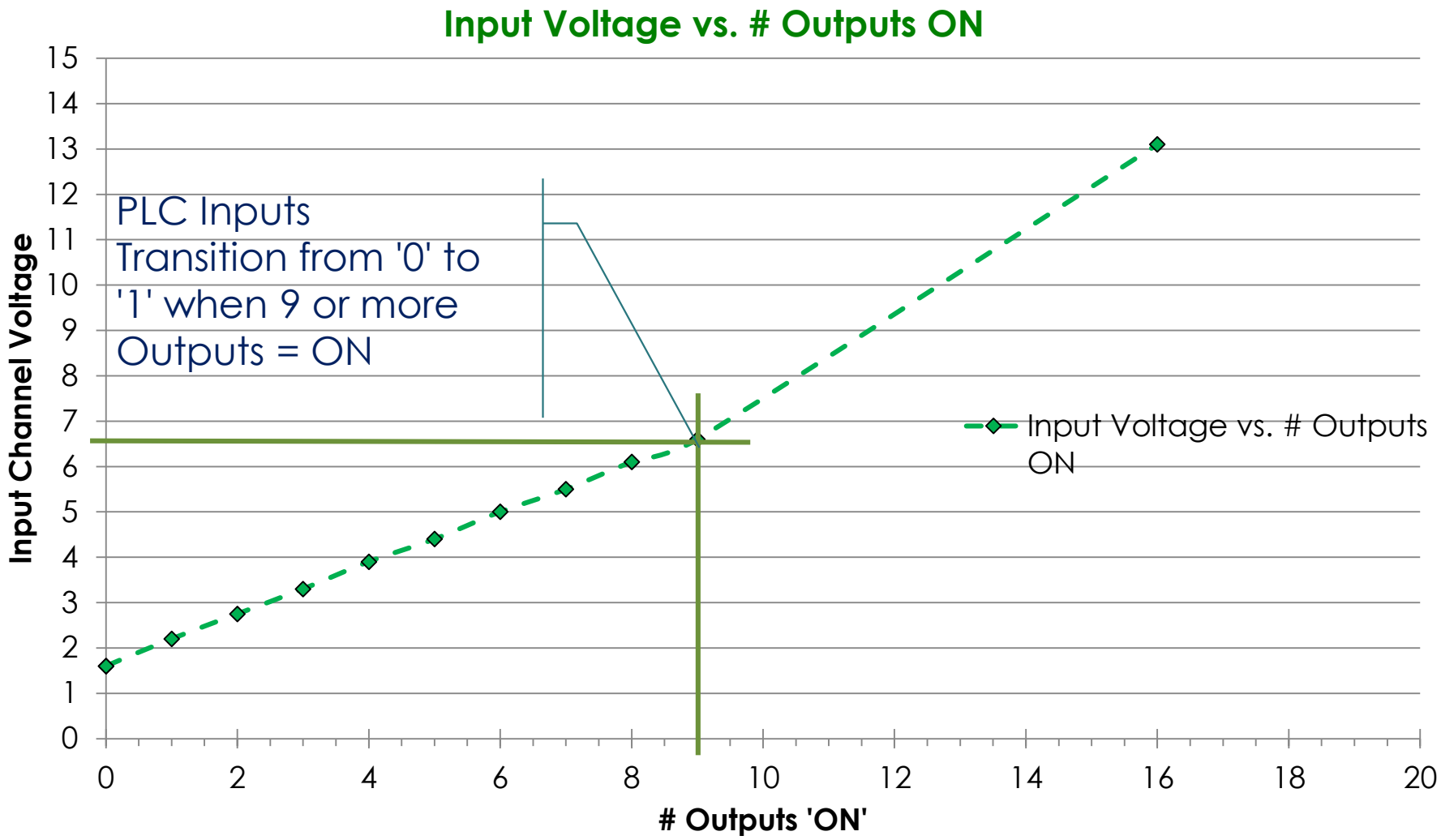
- Power supply modification required a common ground between A and B divisions
- Improperly installed jumper "floated" linac PPS ground, creating a sneak circuit
- Sneak circuit defeated segment to segment handshaking if enough PLC outputs were ON



Biased input “good condition”



Sneak circuit – outputs bias inputs



Questions