UNIVERSITÉ
DE GENÈVE
FACULTÉ DES SCIENCES
Département de physique
nucléaire et corpusculaire

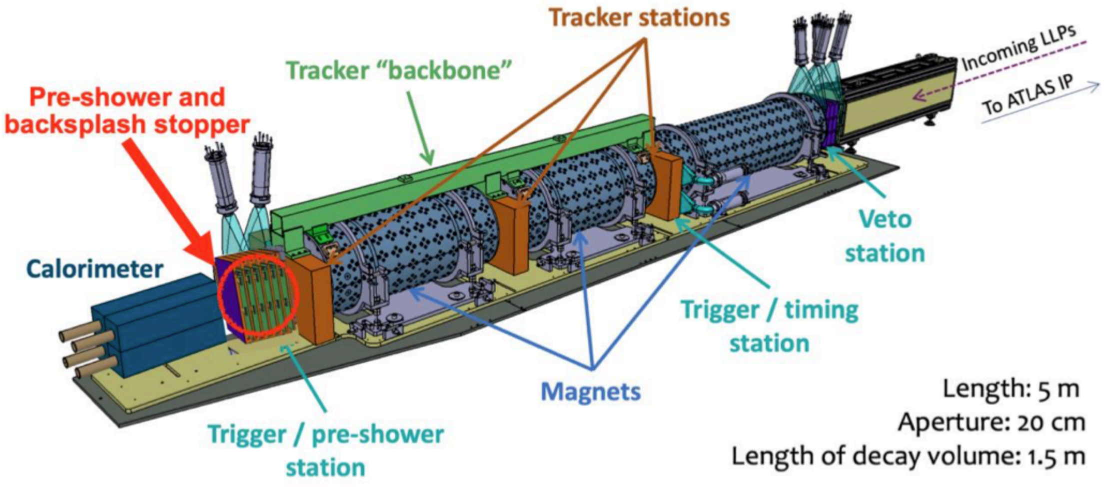
The Monolithic ASIC for the High Precision Preshower Detector of the FASER Experiment at the LHC

CHIARA MAGLIOCCA

on behalf of the FASER Preshower Upgrade Team

Joint SPS and ÖPG Annual Meeting 2023, Basel

The FASER Experiment at LHC



Length: 5 m
Aperture: 20 cm
Length of decay volume: 1.5 m

- **F**orw**A**rd **S**earch **E**xpe**R**iment
- Designed to search for **light and weakly-interacting particles** + study the **interactions of high-energy neutrinos** (FaserNu)

- Fluxes of high-energy SM particles are supressed
- Muons and neutrinos only exception
- FASER can probe **Axion-Like-Particles** (ALPs) model

Zero degrees angle → huge LLPs flux

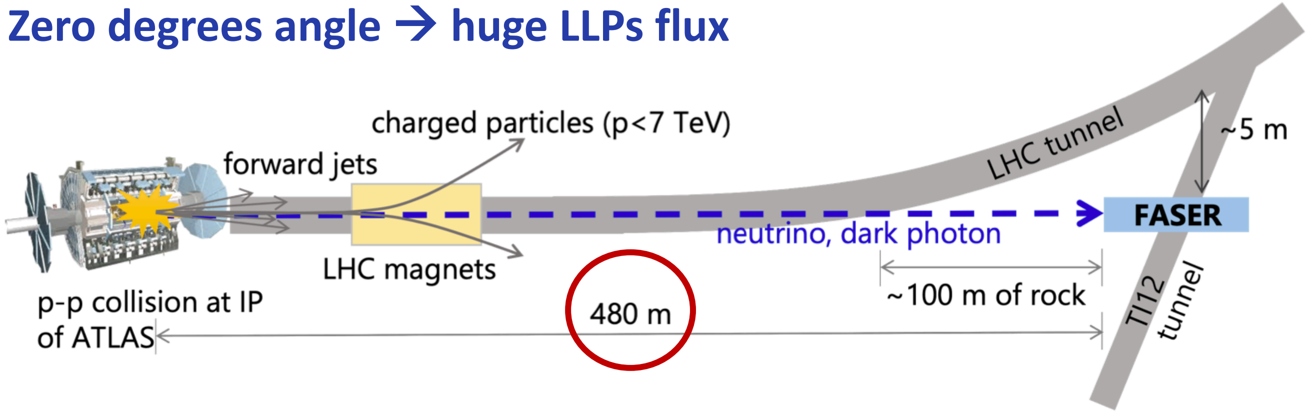
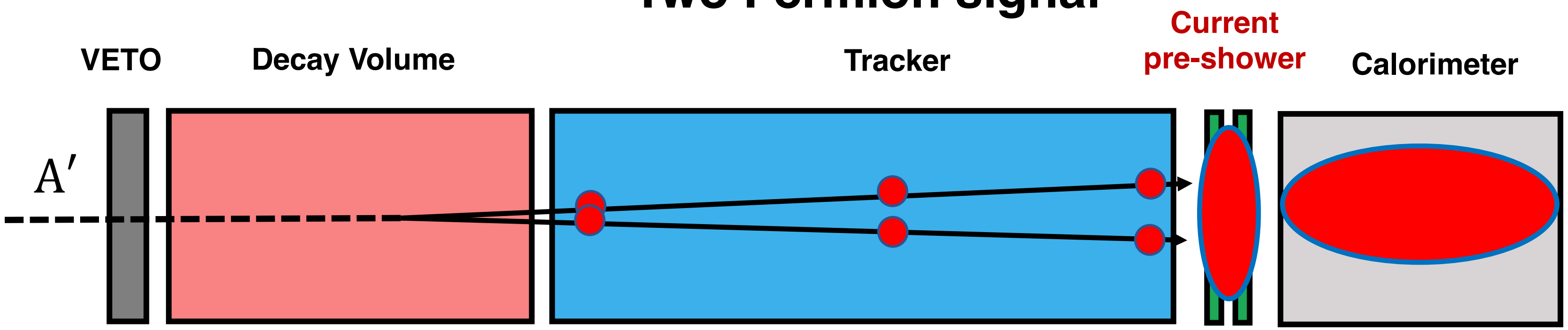


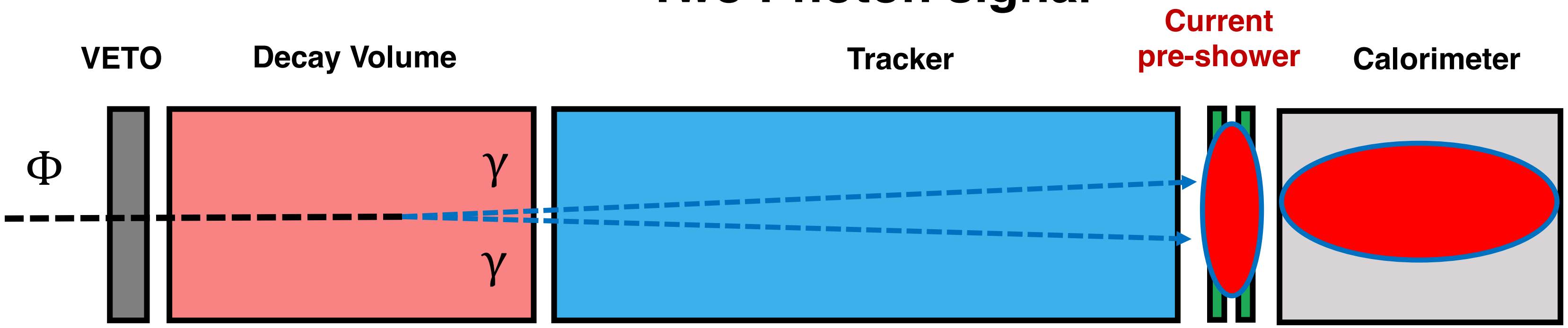
Figure: Location of FASER in the tunnel - schema is not in scale.

What Are We Able to Detect Well: Two Fermion Signal

Two Fermion signal



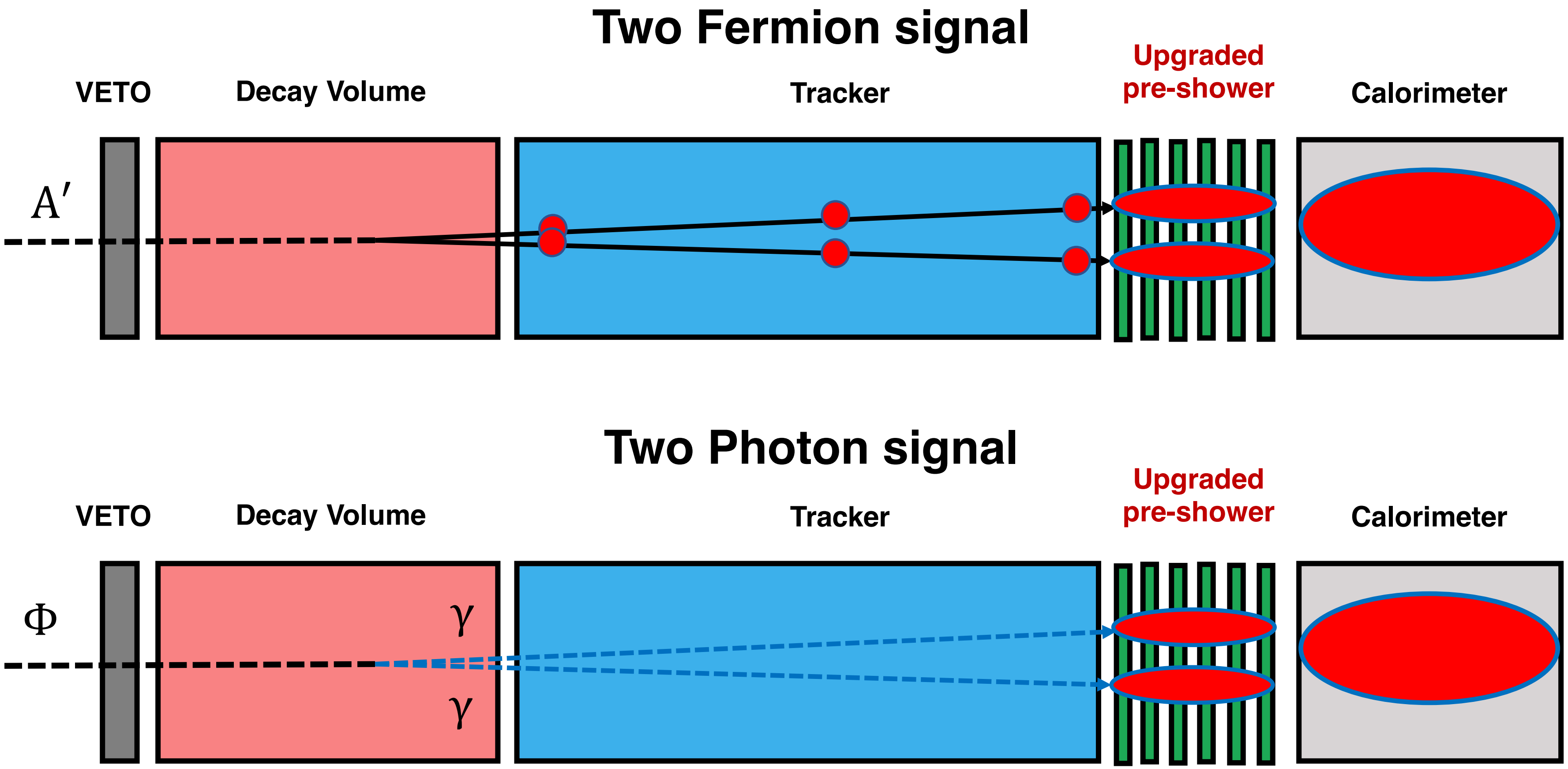
Two Photon signal



NO XY GRANULARITY

unable to resolve diphoton events!

What Are We Willing to Detect: Two Photon Signal



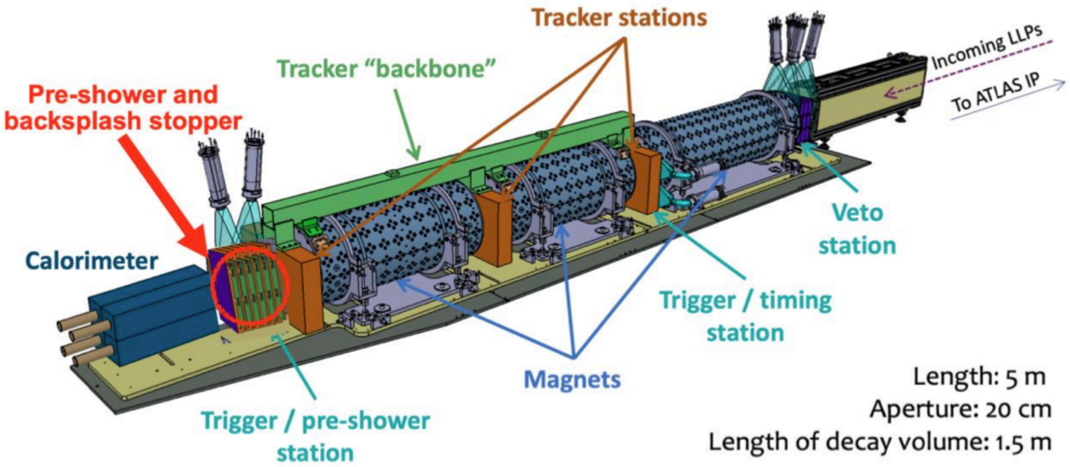
HIGH XY GRANULARITY

The FASER Pre-shower Detector Upgrade

Main Challenge:
Independent measurement of two very collimated high energy photons

Current preshower:

2 layers of tungsten (1X0) + scintillating detectors
⇨ no XY granularity



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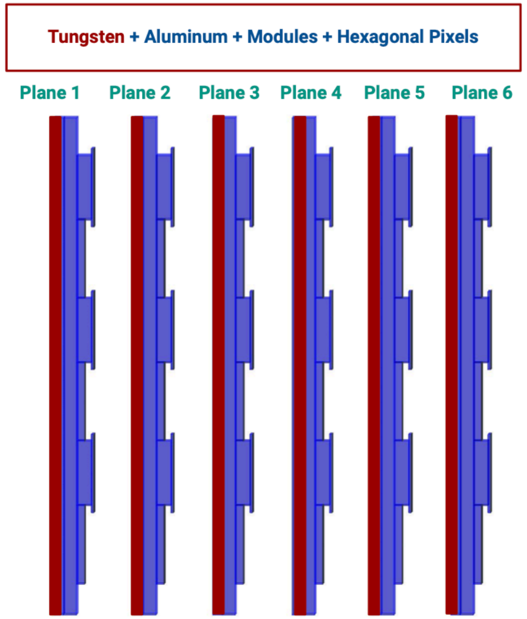
Length of decay volume: 1.5 m

The upgrade:

- **High granularity/high dynamic range** pre-shower based on monolithic silicon pixels sensors
- Discriminate **TeV scale electromagnetic showers**
- Targeting data-taking during last year of LHC Run 3 and HL-LHC

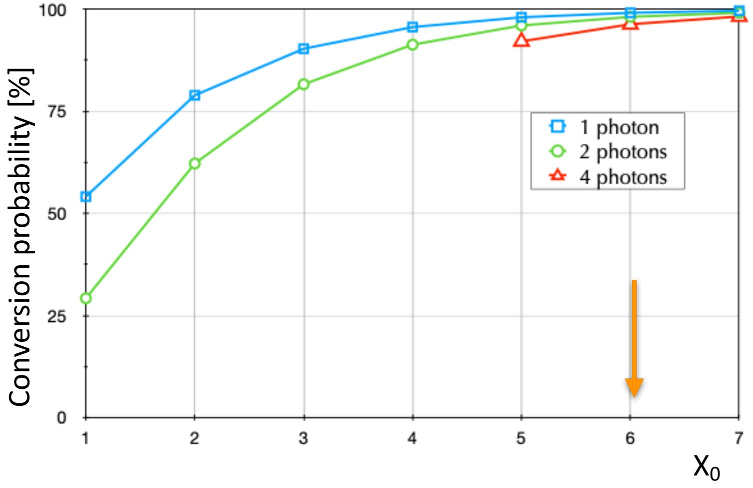
Pre-shower Upgrade Design

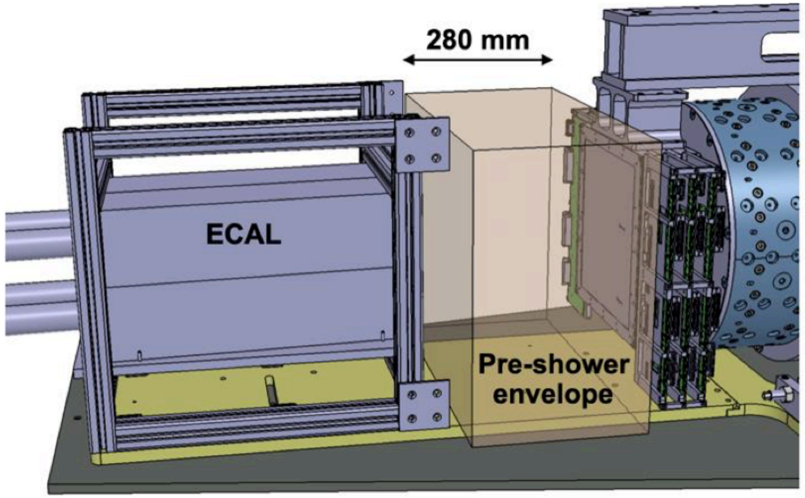
- 6 detector planes
- **6X_0 of tungsten in total**
- One plane of **monolithic Si-pixel sensors** after each tungsten layer

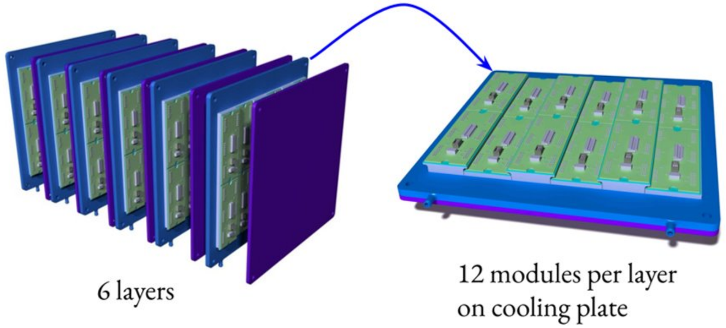


2*(1.70 X_0 of W + Si plane) + 4*(0.65 X_0 of W + Si plane)

More tungsten in the first two layers to force early photon conversion

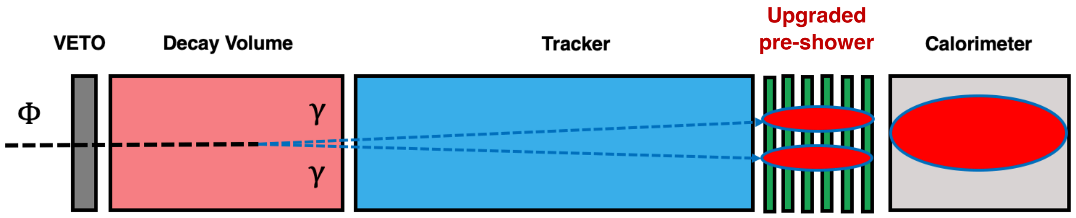




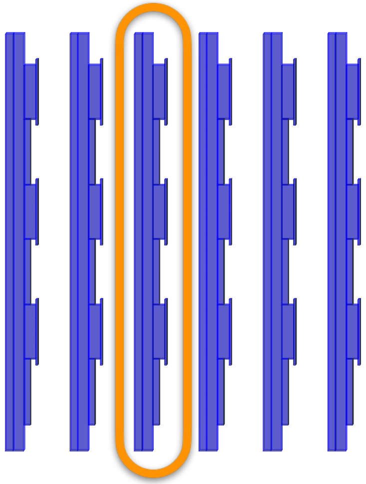


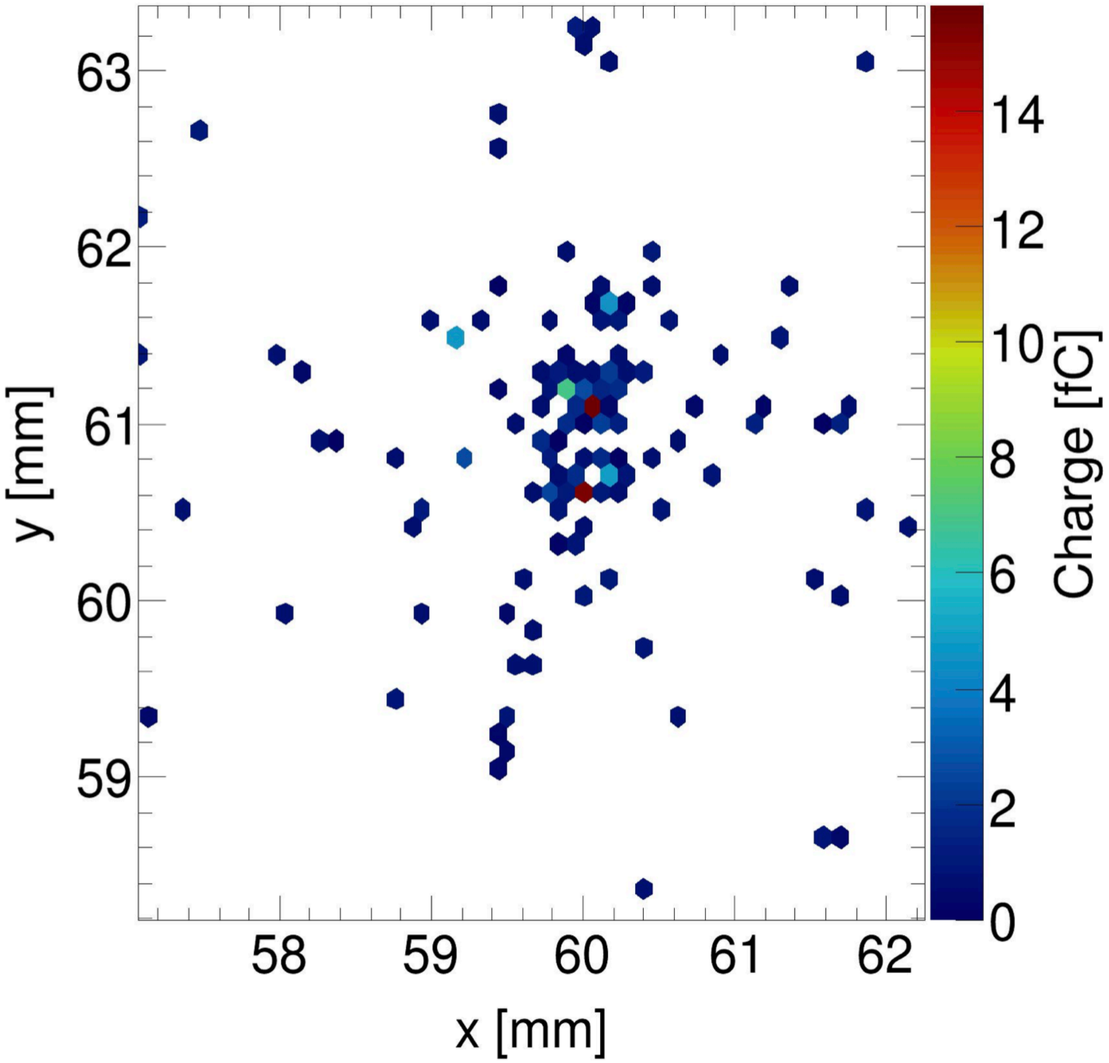
Pre-shower Simulation: Diphoton Signature

Why 6 planes?
Why pixelated sensors?



E1= 1 TeV
E2= 1 TeV
d=500um





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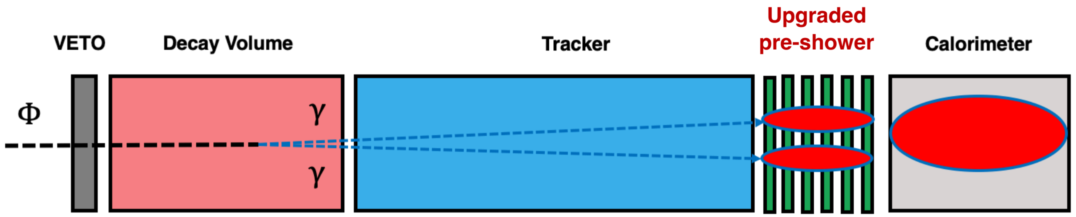

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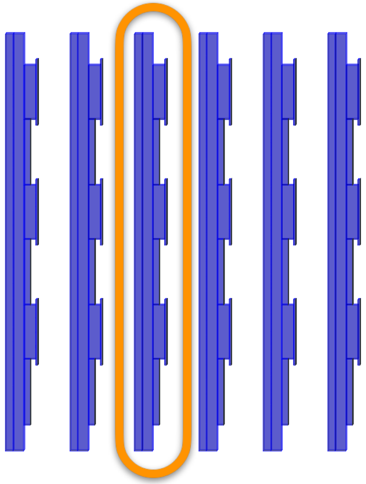

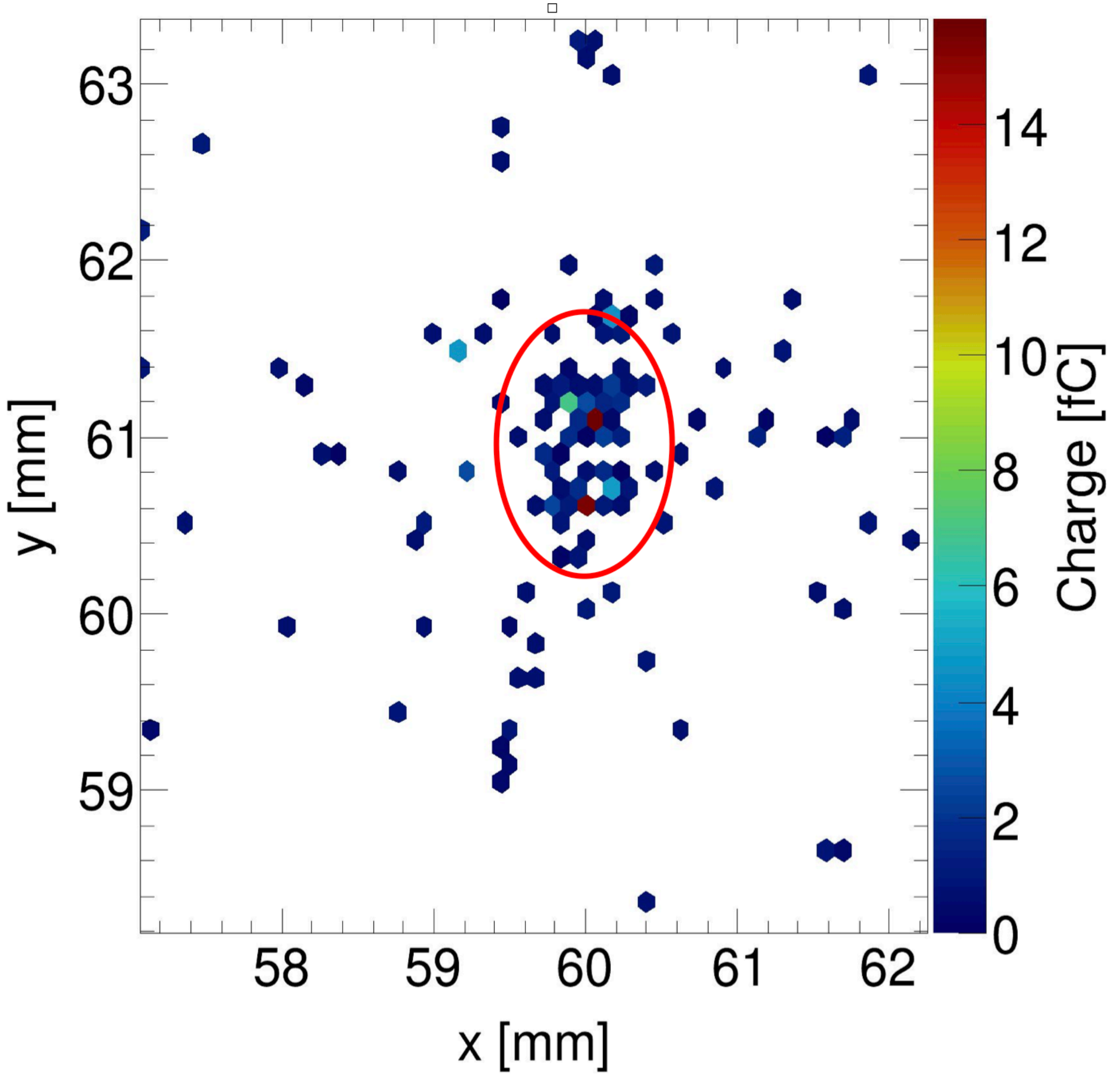

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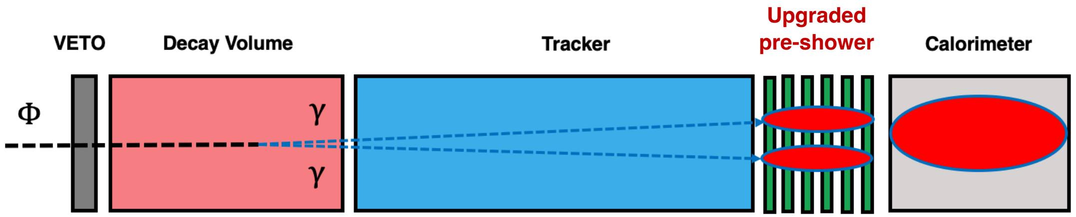

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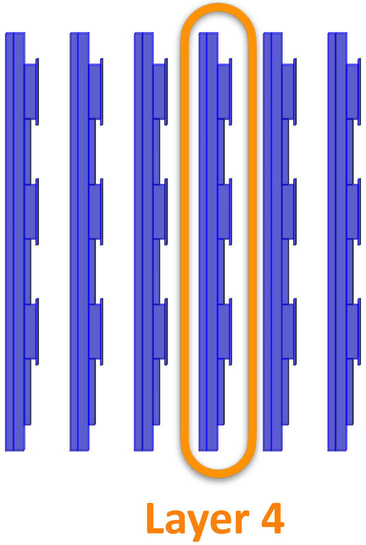

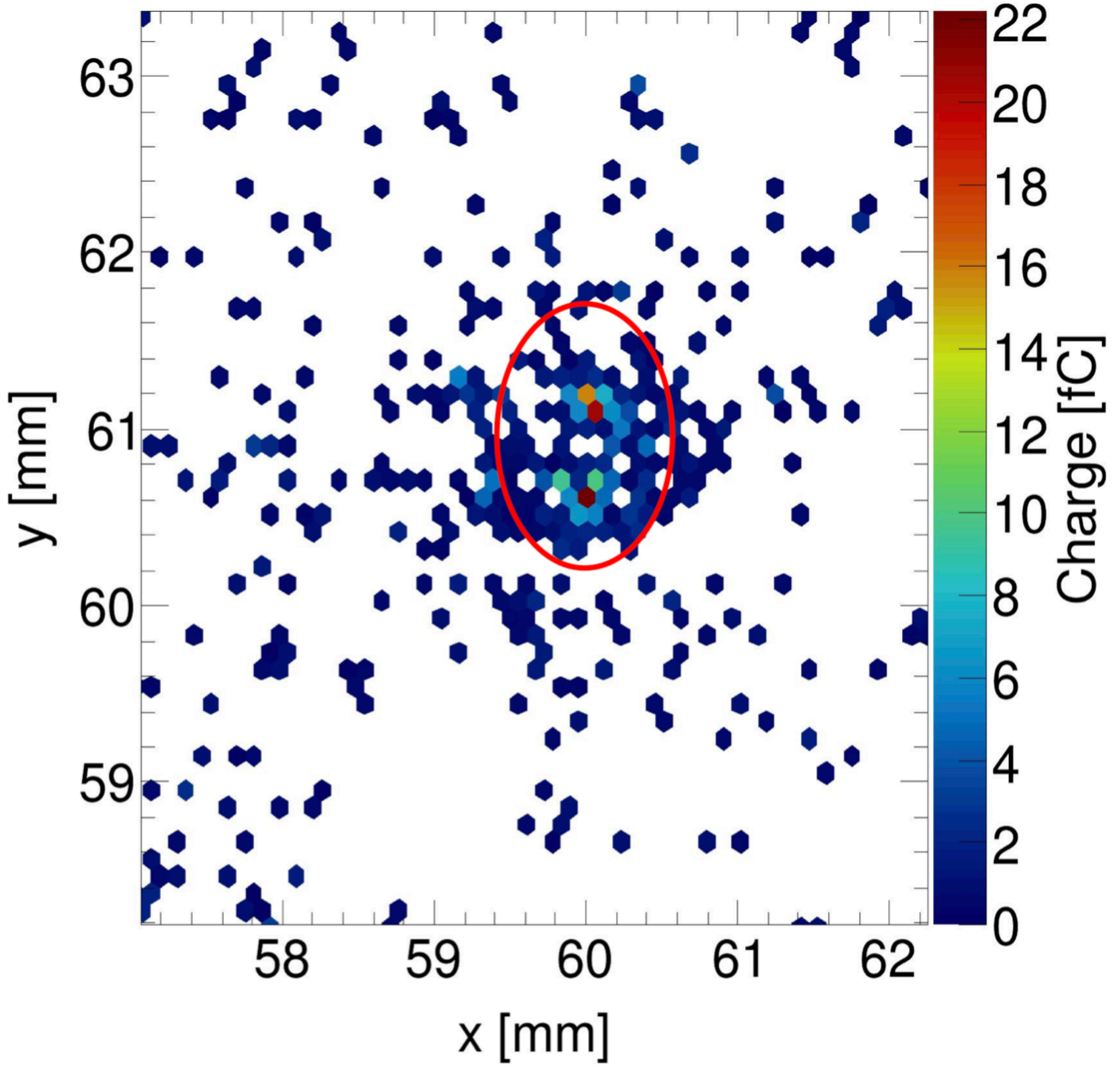

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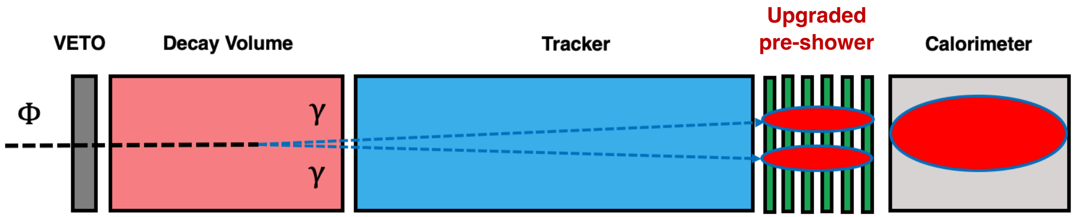

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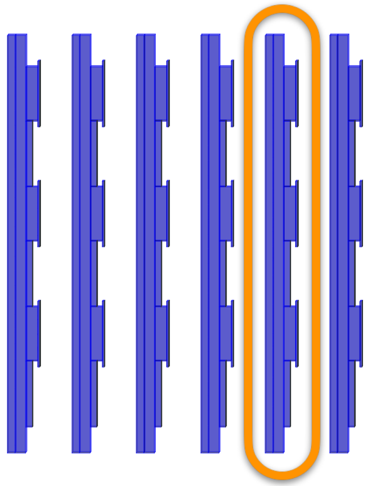
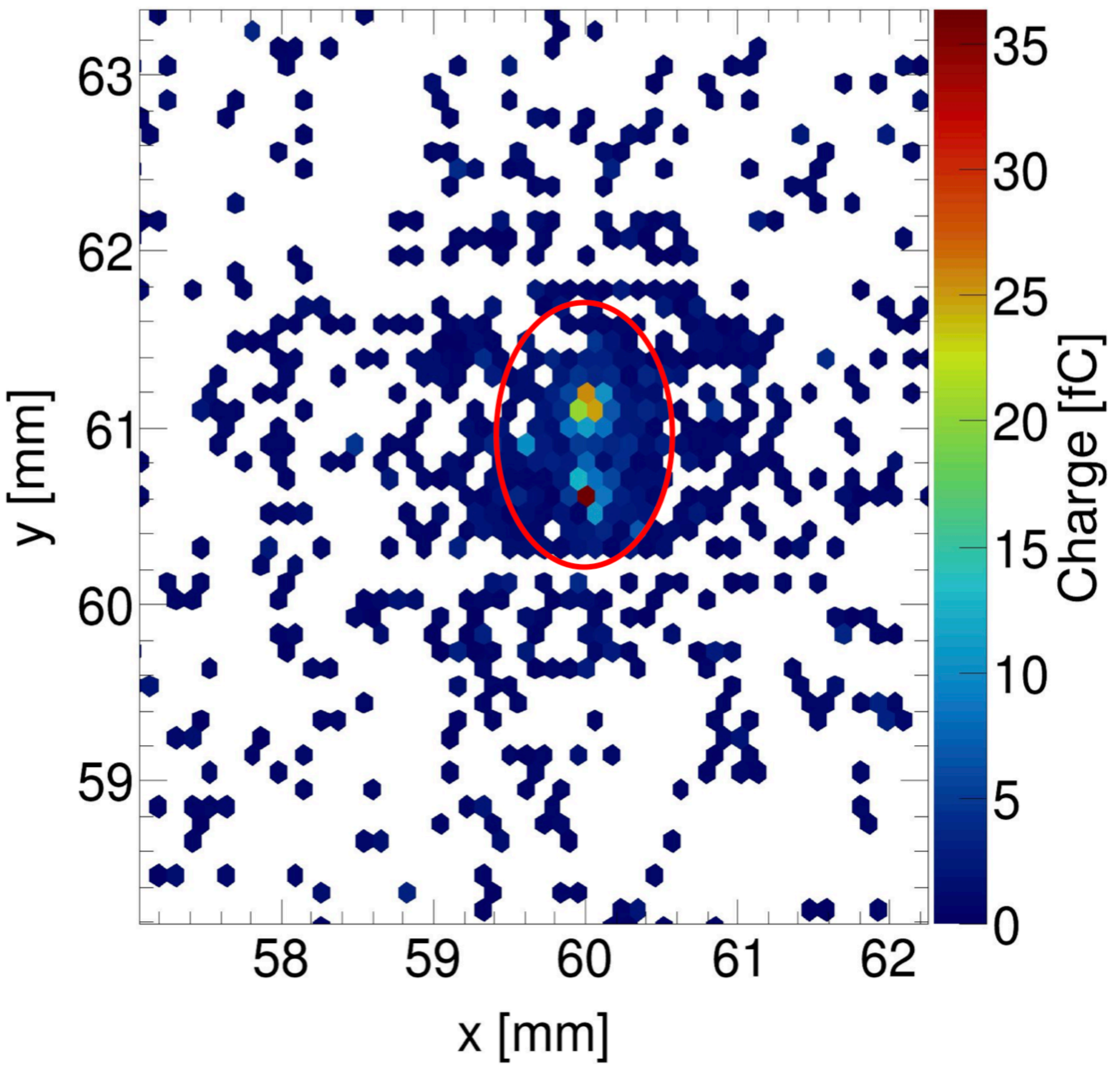

Layer 5



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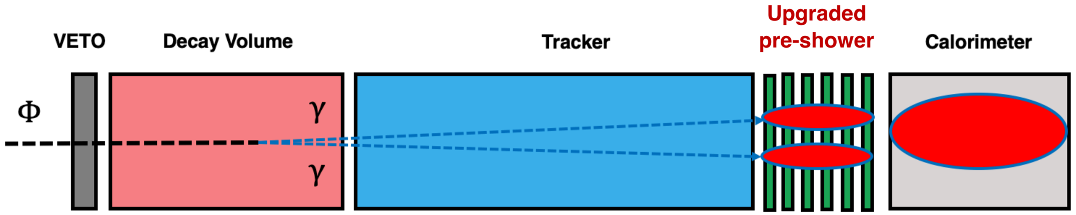

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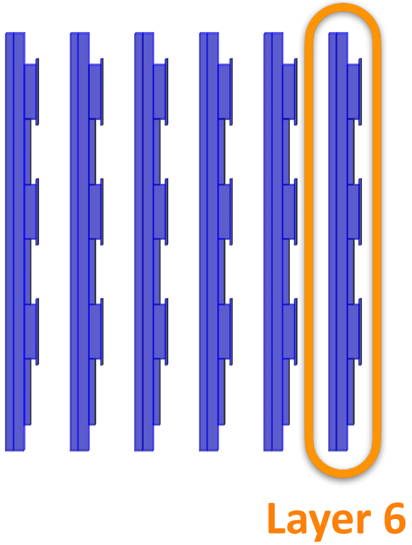

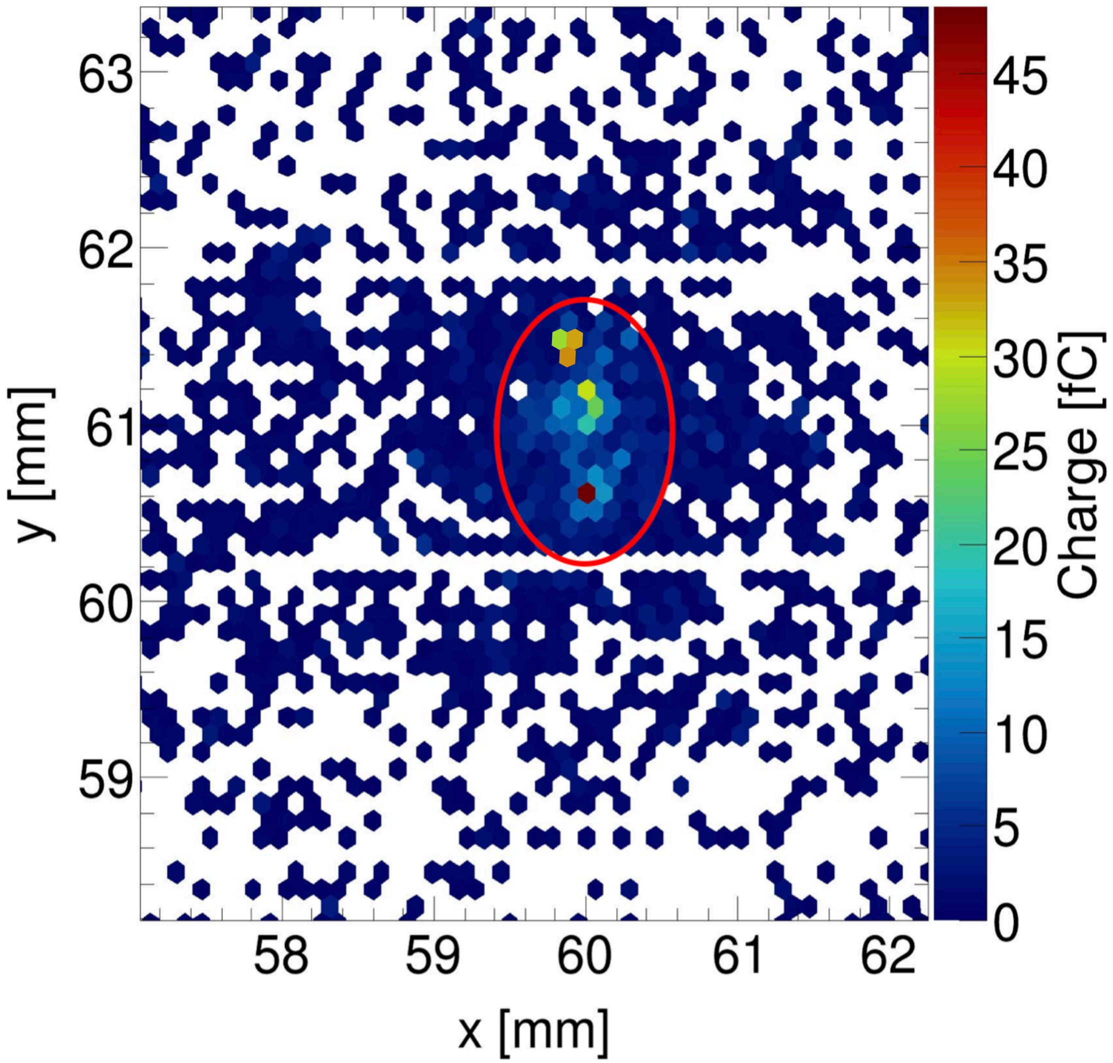

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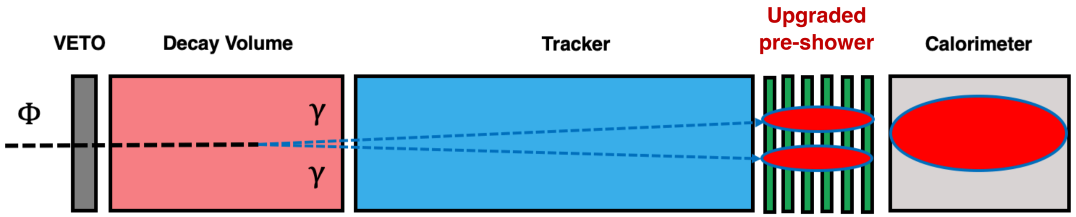

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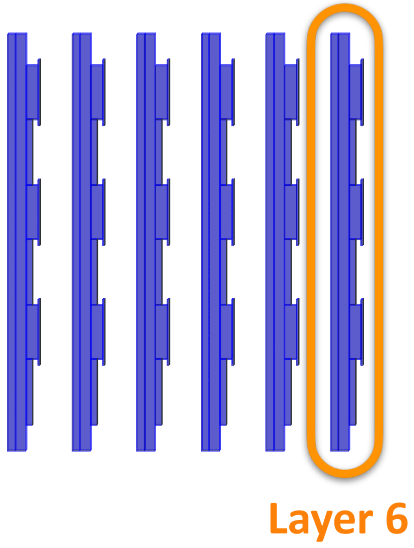
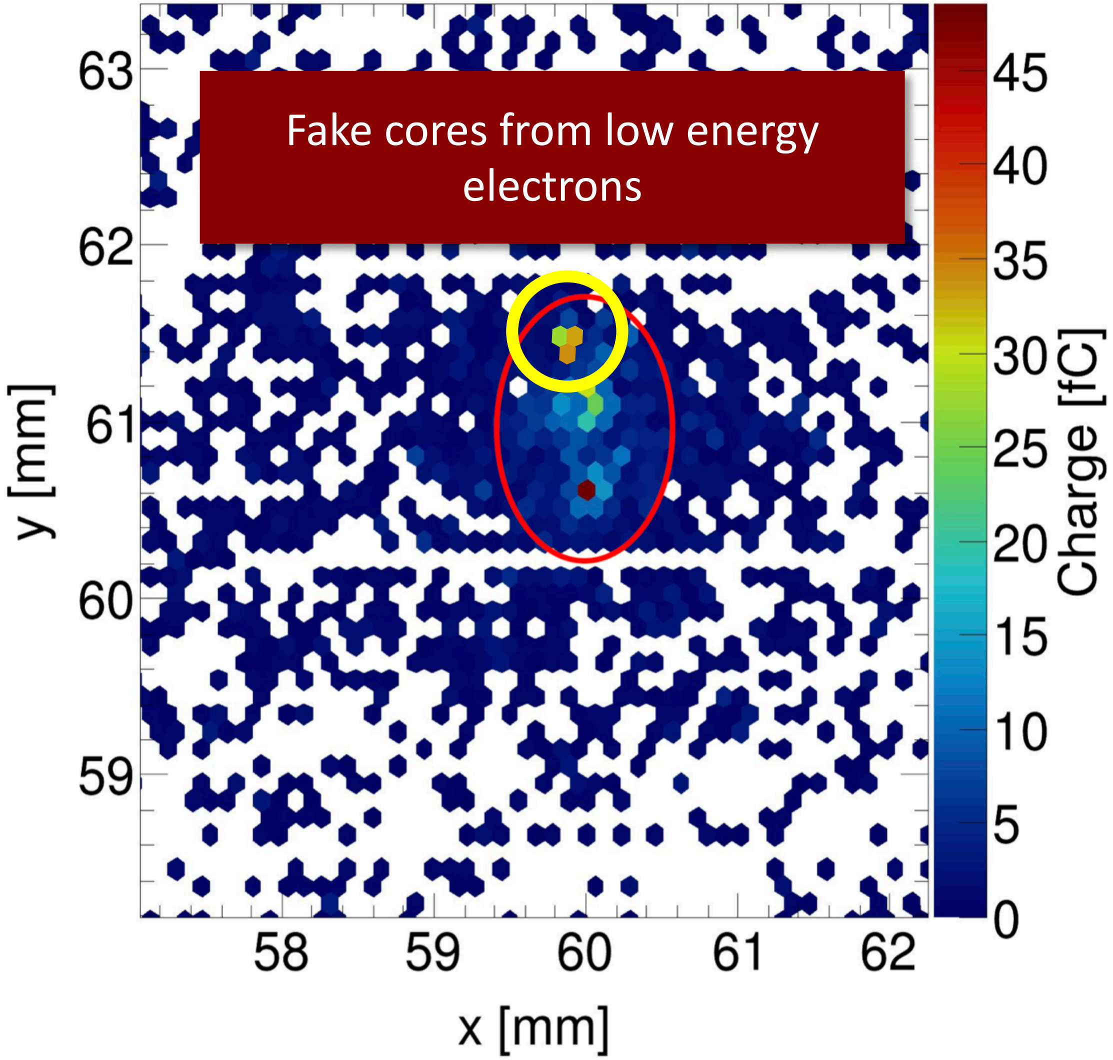


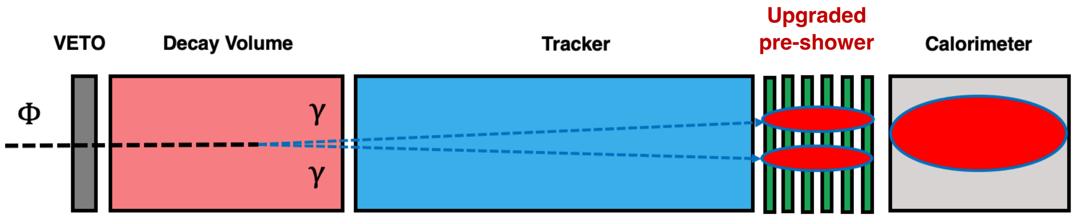


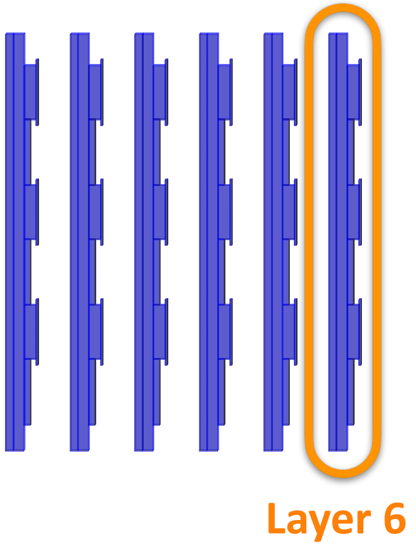
Fake cores from low energy electrons

Pre-shower Simulation: Diphoton Signature

Very large occupancy

High dynamic range for charge measurements





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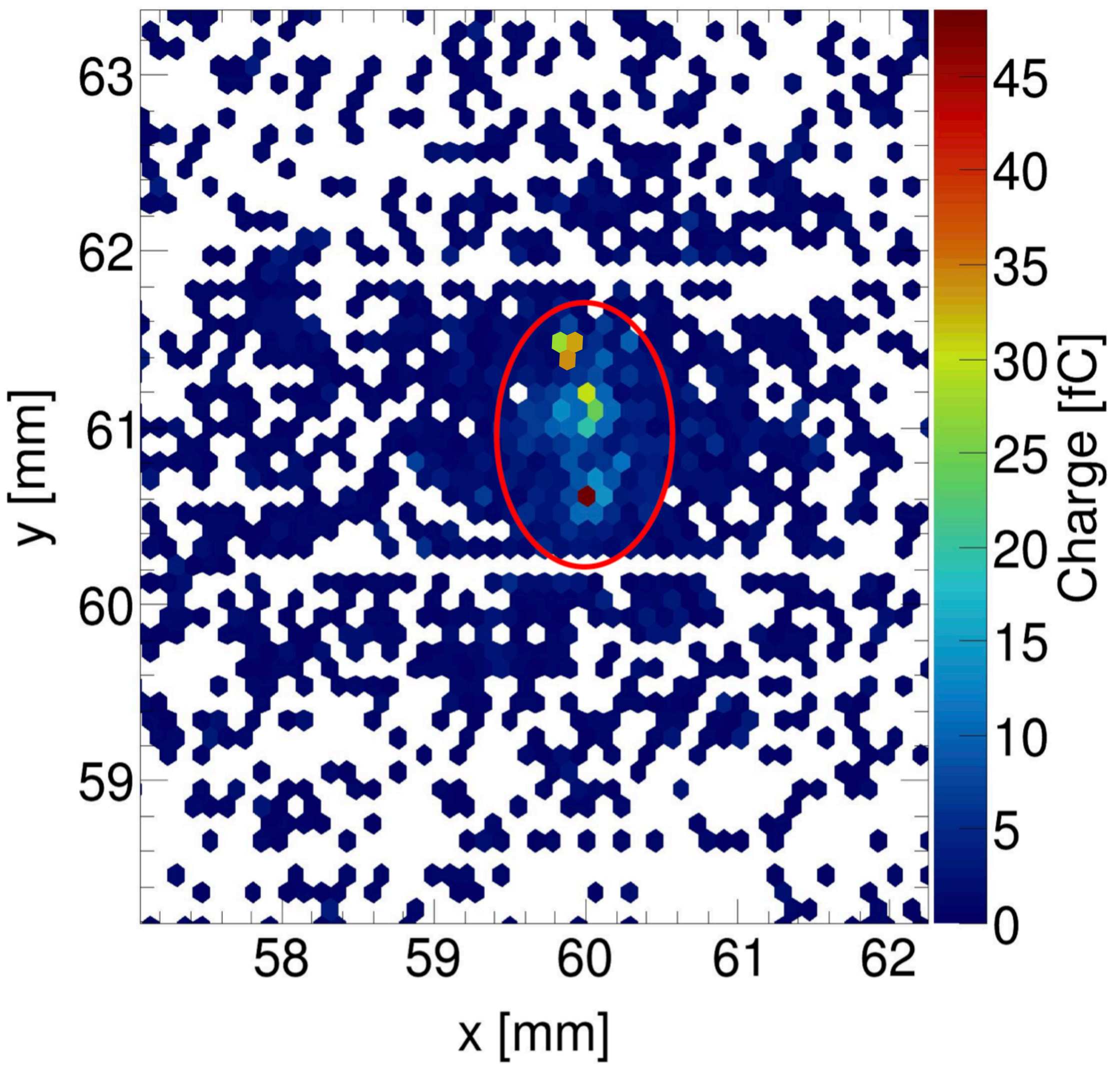
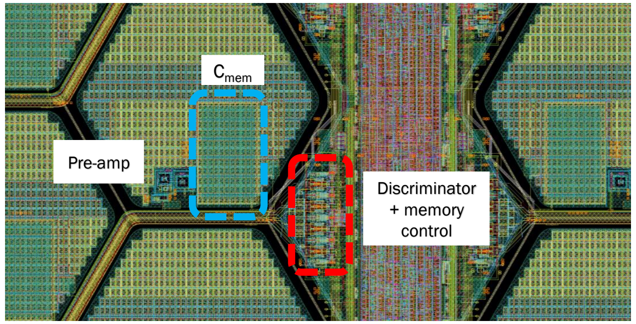
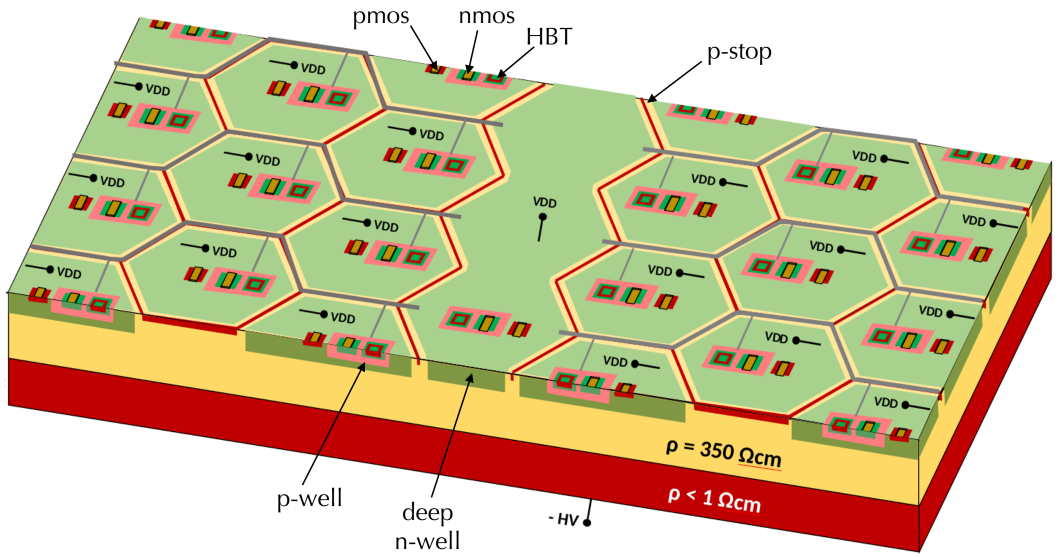


Monolithic Pixel ASIC: the Sensor



Monolithic active pixel sensor
130 nm SiGe BiCMOS technology (SG13G2 by IHP microelectronics)

- High-resistivity (220 Ωcm) substrate, about 130 µm thickness
- Hexagonal 65 µm side pixels integrated as triple well; 80fF pixel capacitance
- **High dynamic range** for charge measurement (0.5 ÷ 65 fC)
- **Ultra fast readout** with no digital memory on-chip (to minimize dead area)
- **Local analog memories** to store the charge

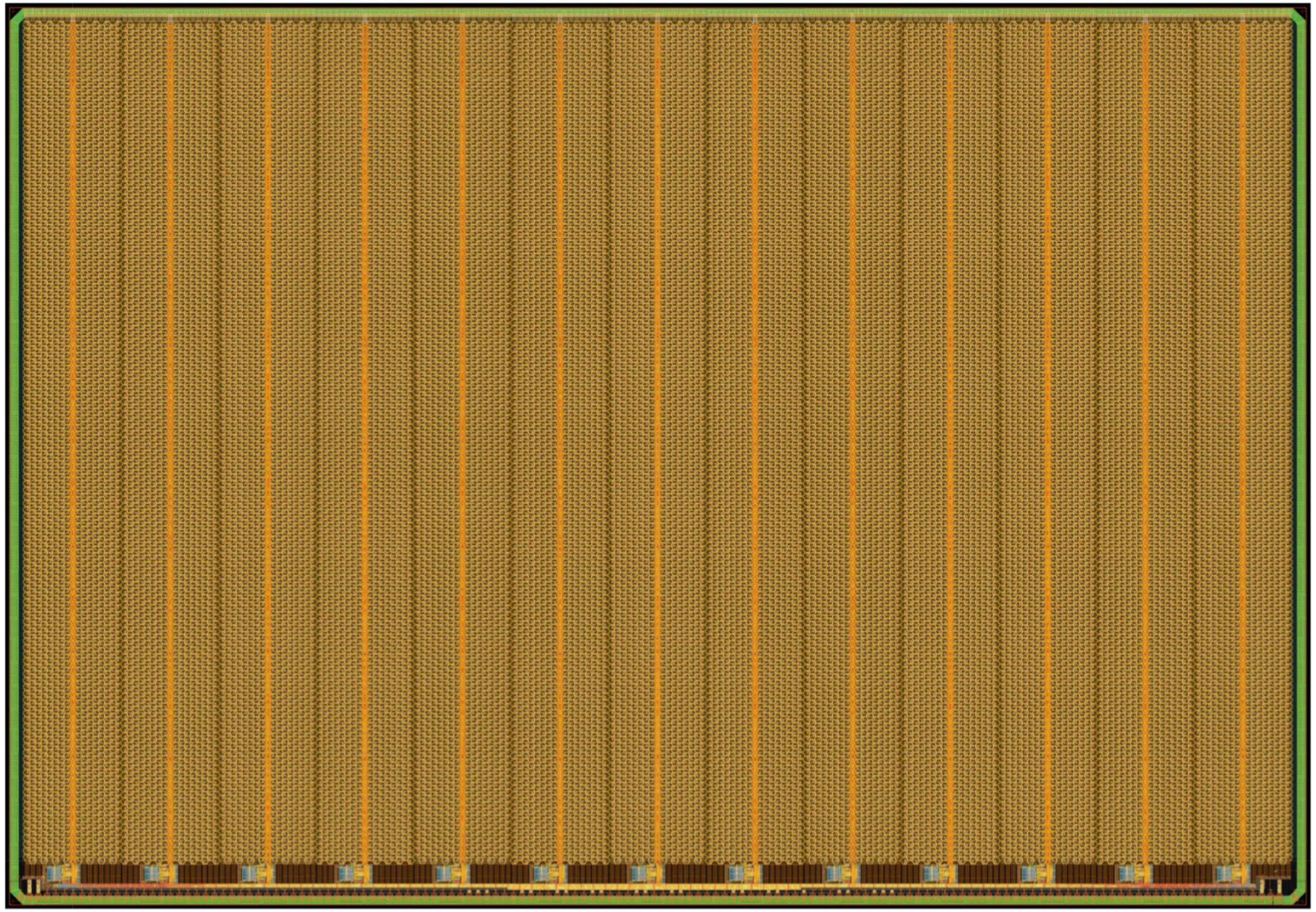


Main specifications	
Pixel Size	65 µm side (hexagonal)
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 µs
Power consuption	< 150 mW/cm^2
Time resolution	< 300 ps

Final Production Chip submitted in May 2023

Monolithic ASIC Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)



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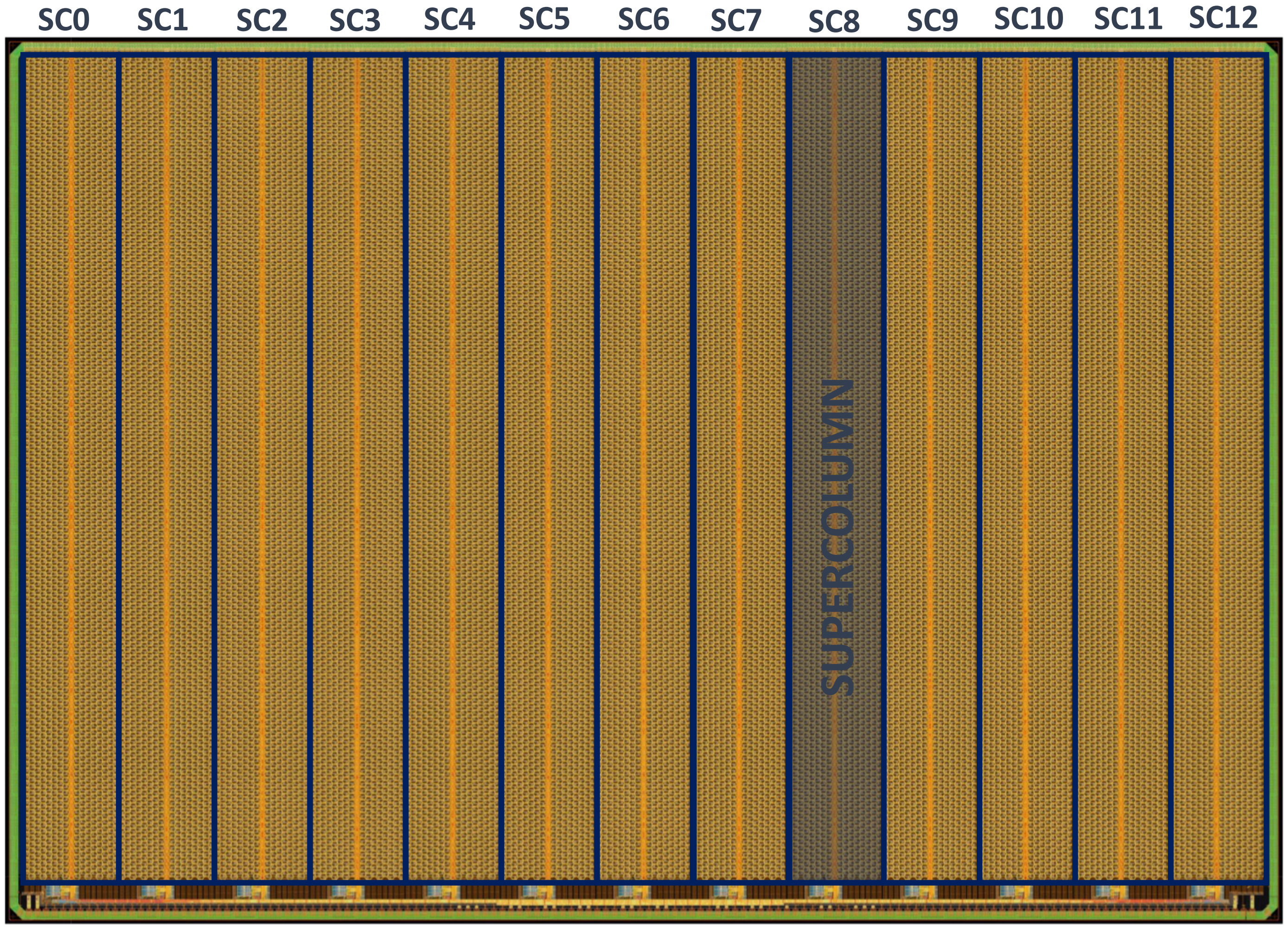
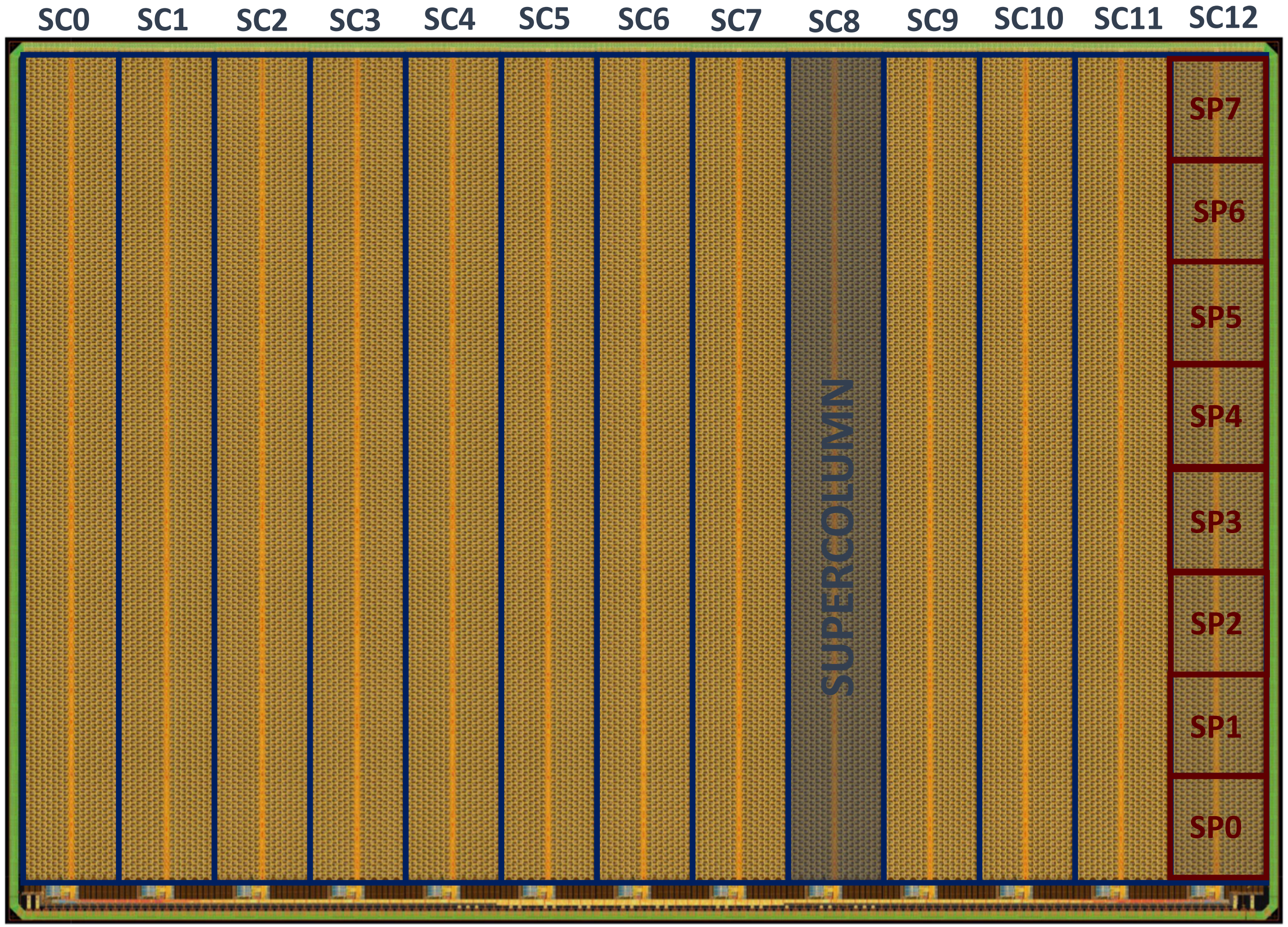
Monolithic ASIC Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)
- 13 **Supercolumns** (SC)



Monolithic ASIC Modular Architecture

- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26'624 pixels in total**)
- 13 **Supercolumns** (SC)
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)



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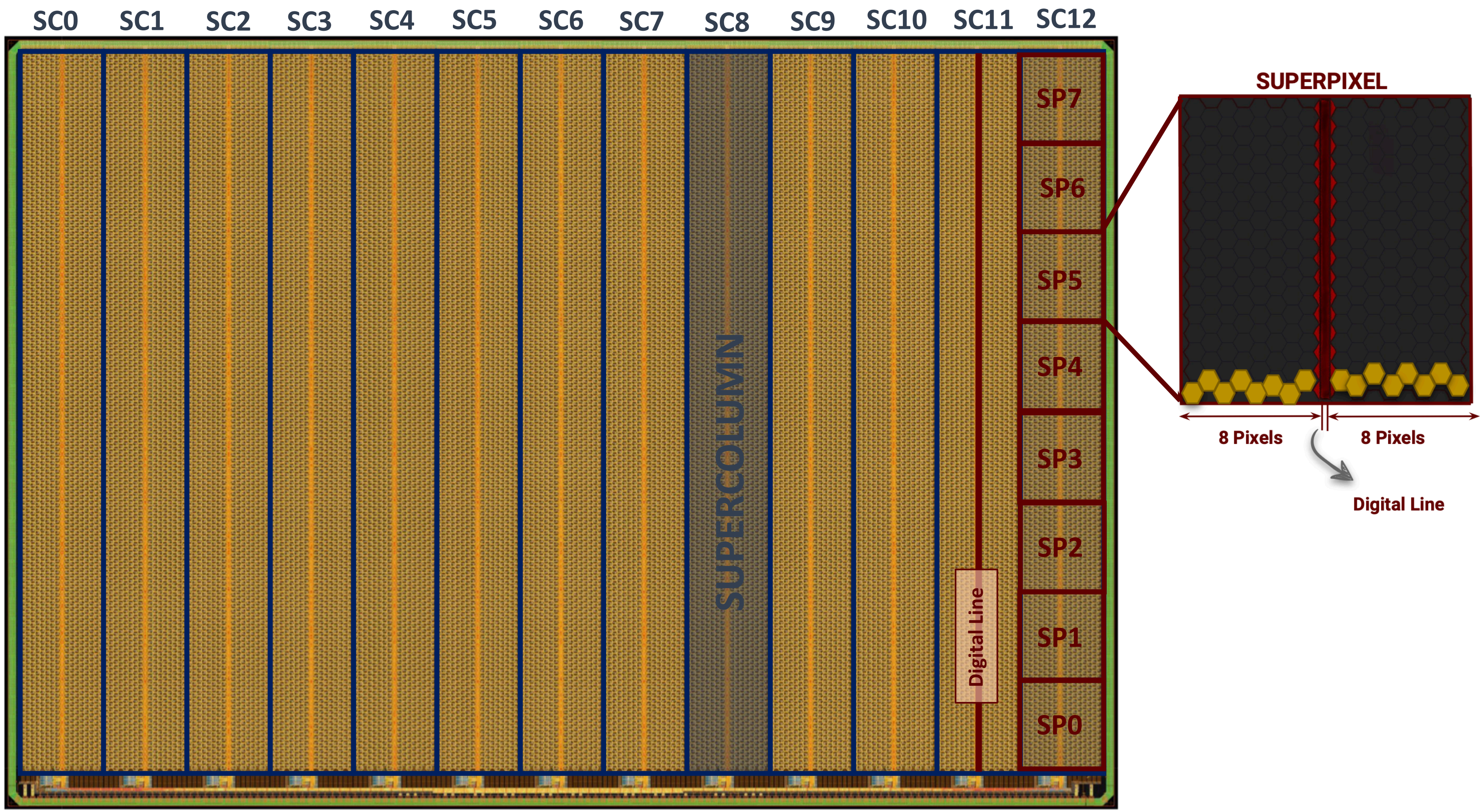
- and 1 **Digital Line** (40 µm)



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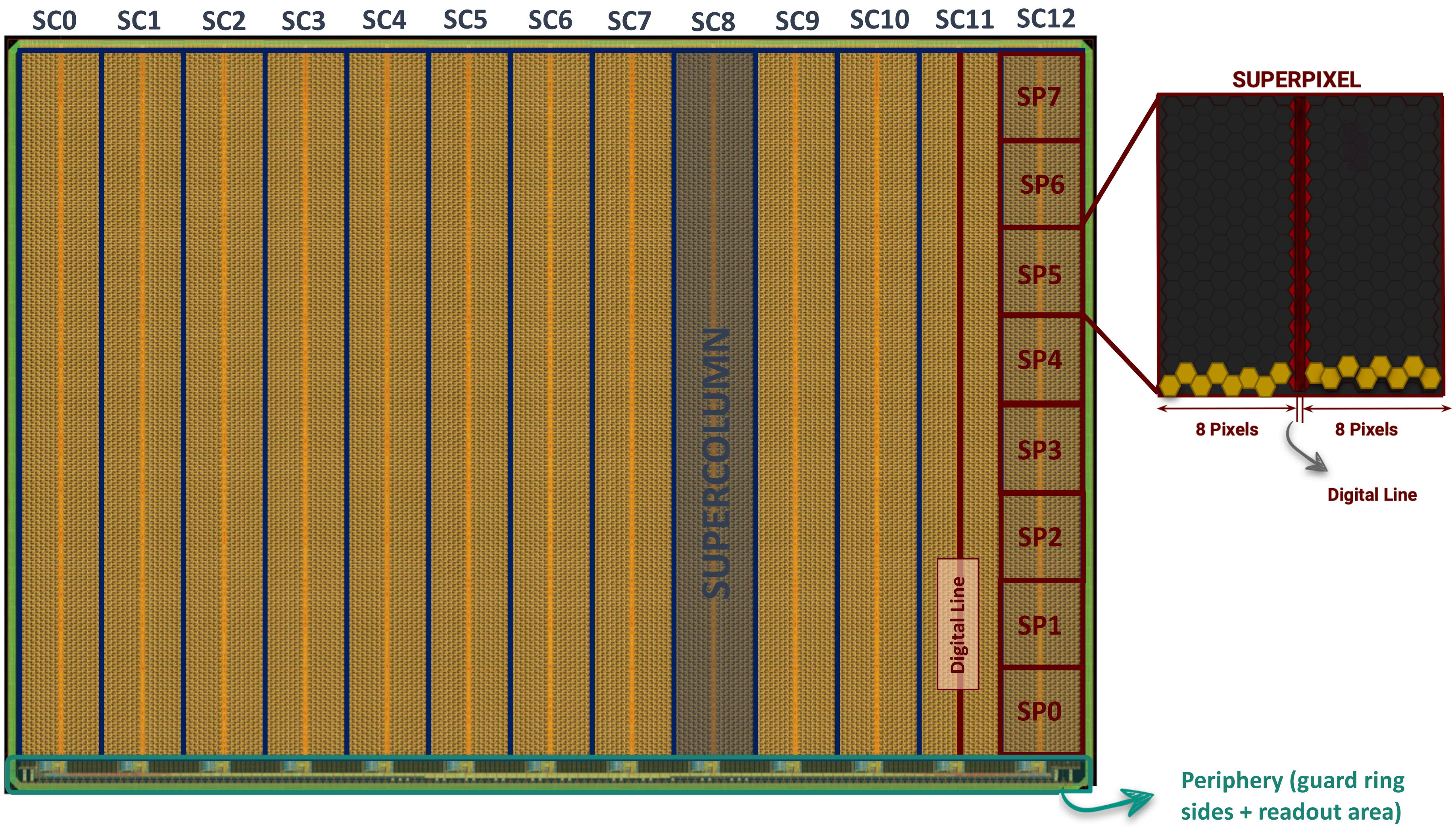
- Chip size: 2.2 x 1.5 cm^2 with matrix of 208x128 pixels (**26’624 pixels in total**)
- 13 **Supercolumns** (SC)
- Each Supercolumn has 8 **Superpixels** (SP) (16x16 pixels)
- and 1 **Digital Line** (40 µm)
- **Periphery** (I/O and arbitrary logic) with dead area
  - 720 µm on the readout side
  - 270 µm for the guard ring



Periphery (guard ring sides + readout area)

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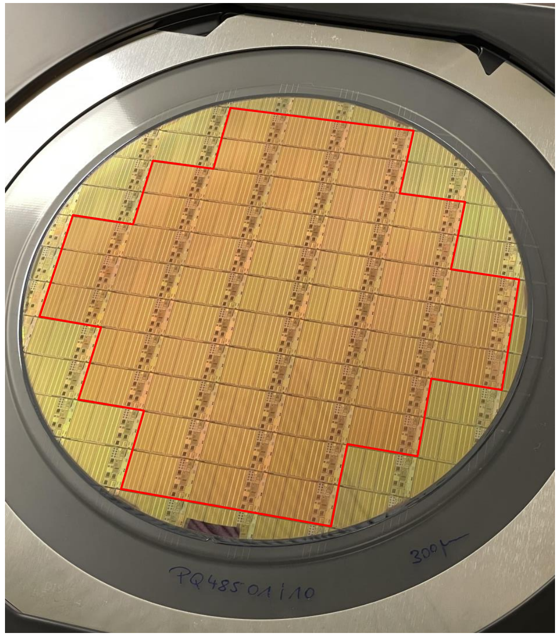
The Pre-production ASIC

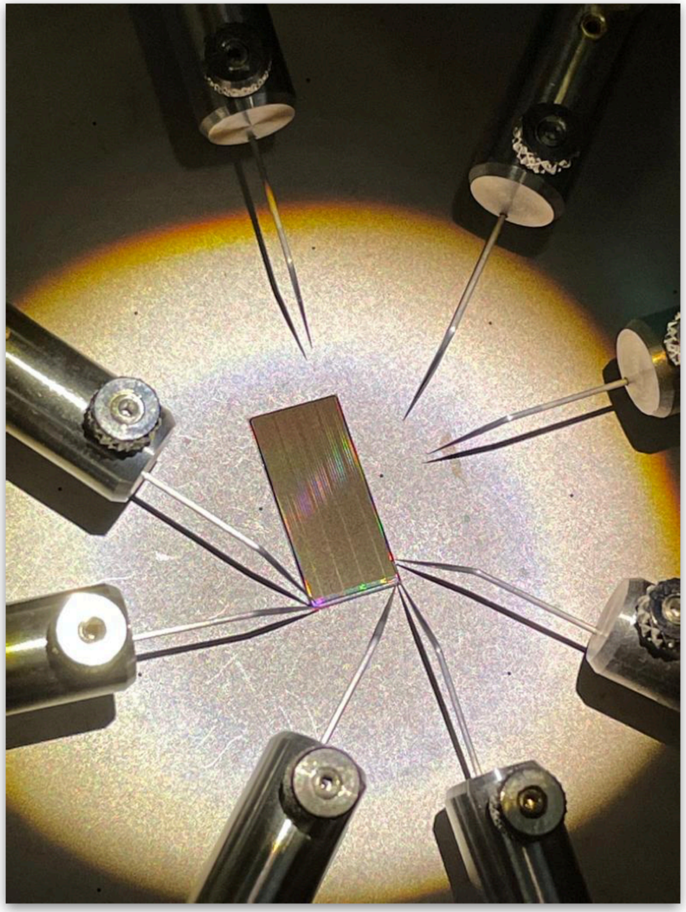
Reticle: 2.4 x 1.5 cm^2

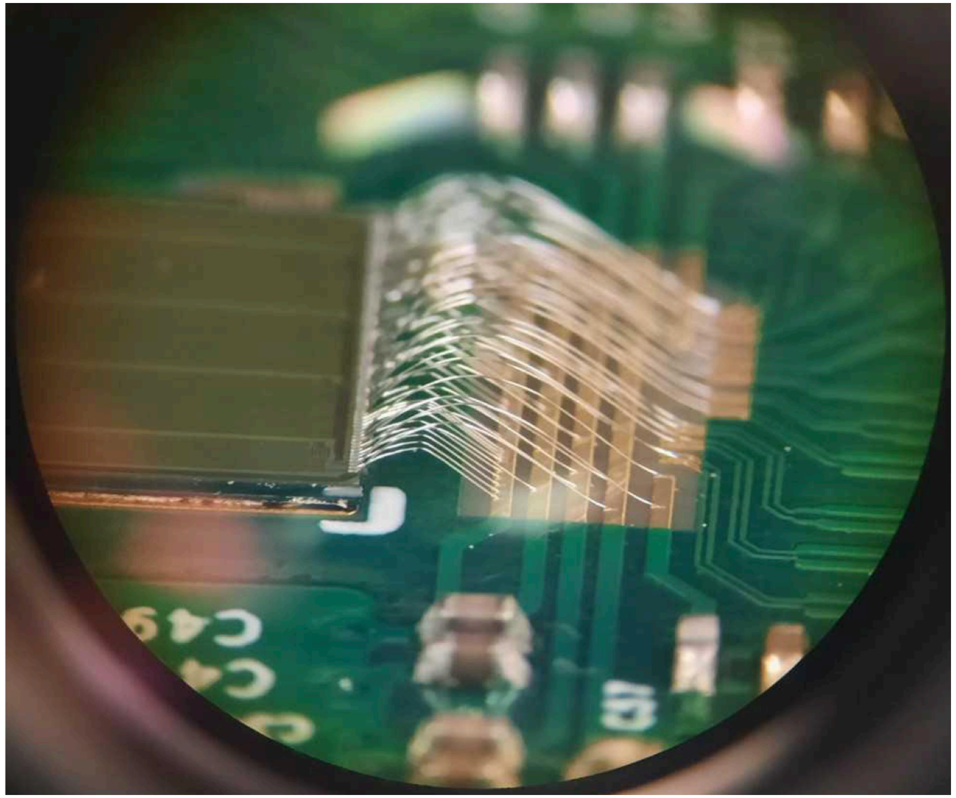
53 reticles per wafer

Thickness 300 µm



CHIP @ probe station

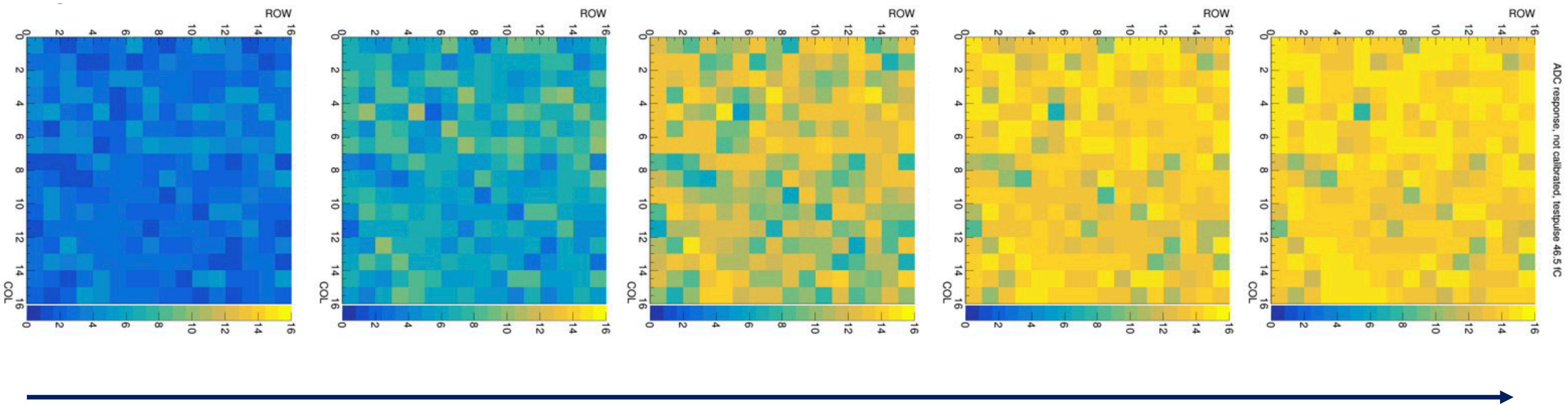




Test on pre-production ASIC: ADC Response

Study of the chip response for different value of injected charge

(here one Superpixel)



Injected charge

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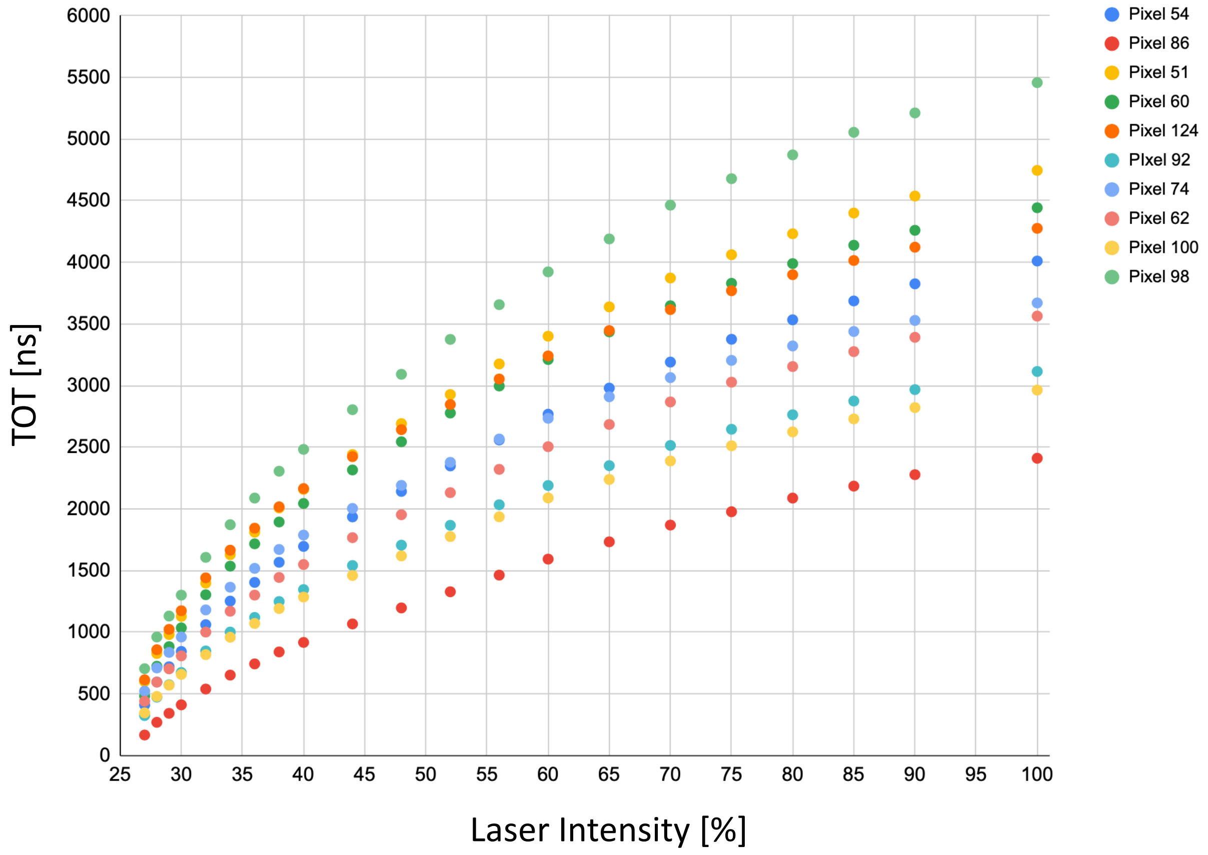
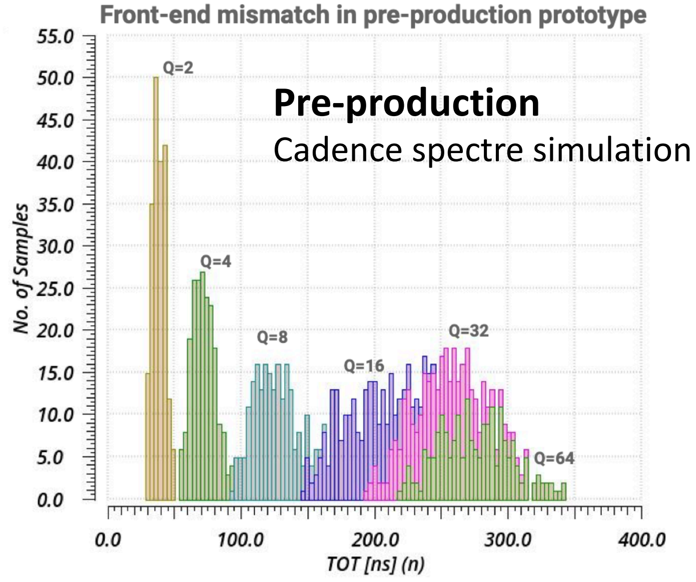
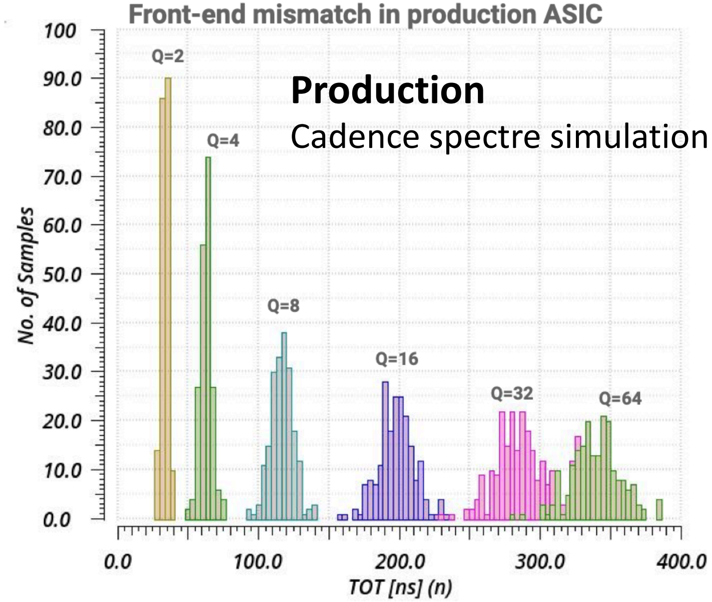
Test on pre-production ASIC Front-end Mismatch



Large mismatch on the pre-production chip from amplifier response

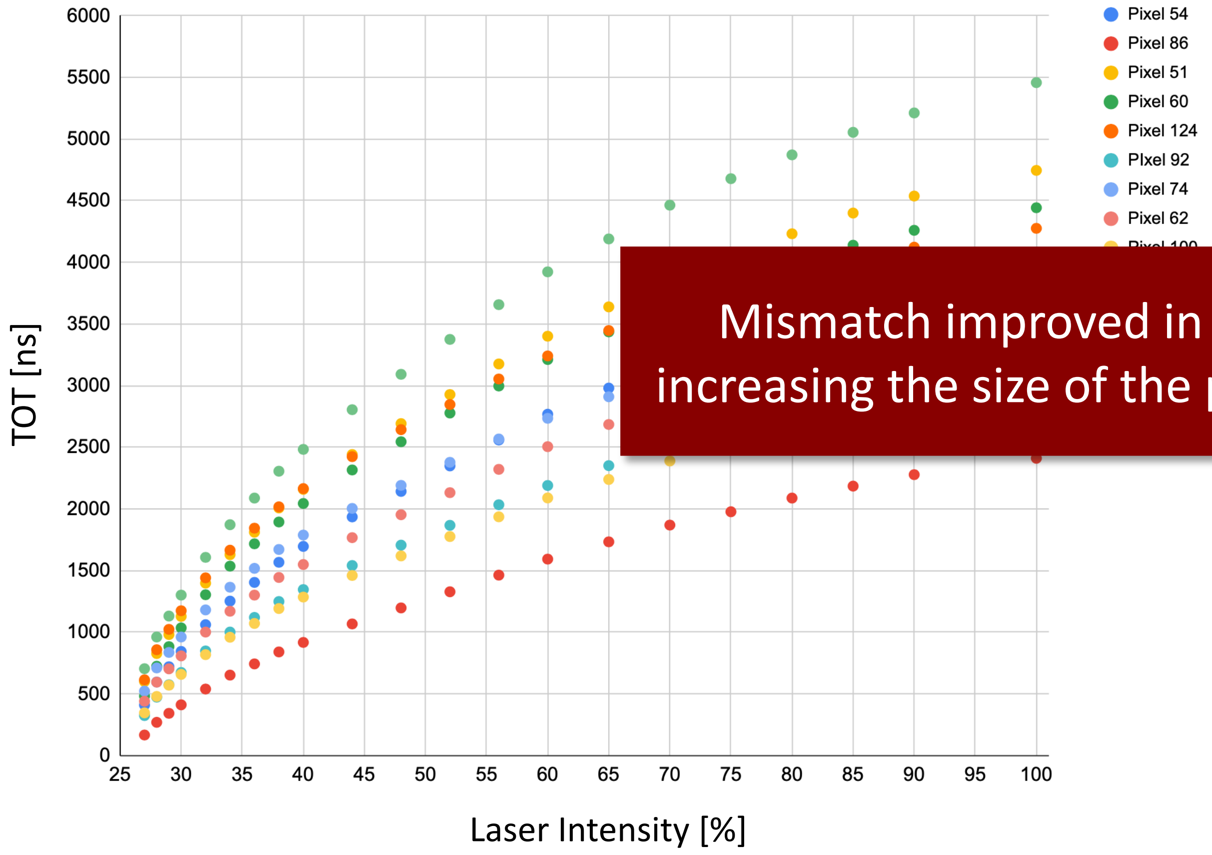


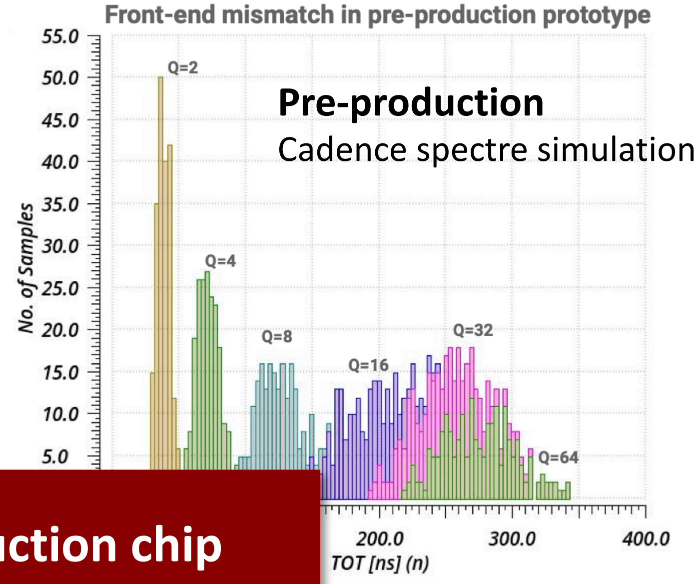
Pre-production
Cadence spectre simulation



Production
Cadence spectre simulation

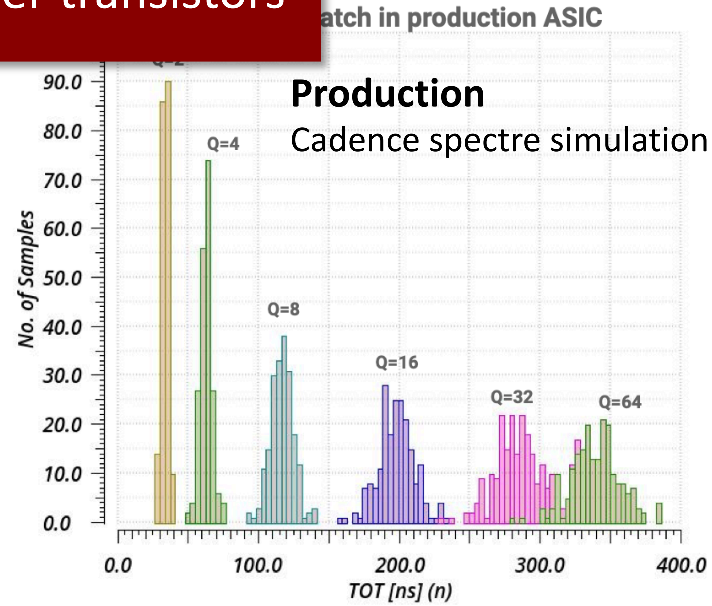
Test on pre-production ASIC: Front-end Mismatch





Pre-production
Cadence spectre simulation

Mismatch improved in the **production chip** increasing the size of the preamplifier transistors



Production
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Large mismatch on the pre-production chip from amplifier response

Summary and Conclusions

- A **new preshower detector** is being developed for the **FASER experiment** at the LHC
    - Enabling the discrimination of ultra-collimated TeV diphoton events from LLP decays
    - 130 nm SiGe BiCMOS Technology MAPS designed and developed at the University of Geneva, with support from KIT and CERN
    - Targeting installation in 2024 and data-taking during last year of LHC Run 3 and HL-LHC

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  - Everything is working fine and we are finalizing the characterization in the Lab
  - Minor bugs have been identified and corrections have been implemented in the production chip
  - First assembled modules currently ongoing
  - A paper on the characterization of the pre-production chip will be published soon

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- **Final production chip submitted in May 2023**
    - Expected delivery: December 2023
    - Test beam at SPS (CERN) planned for August 2024

The FASER Collaboration

CERN
UNIVERSITÉ DE GENÈVE
KYUSHU UNIVERSITY
UC IRVINE
UNIVERSITÄT BERN
Technion Israel Institute of Technology
NAGOYA UNIVERSITY
UNIVERSITY of WASHINGTON
JOHANNES GUTENBERG UNIVERSITÄT MAINZ JG|U
מכון ויצמן למדע WEIZMANN INSTITUTE OF SCIENCE
KEK
UNIVERSITY OF OREGON
UNIVERSITÄT BONN
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MANCHESTER 1824 The University of Manchester
ROYAL HOLLOWAY UNIVERSITY OF LONDON
UNIVERSITY OF LIVERPOOL
CHIBA UNIVERSITY
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International laboratory covered by a cooperation agreement with CERN
UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

FASER Collaboration Members

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The development and construction of the W-Si pre-shower of the FASER experiment was funded by the **Swiss National Science Foundation (SNSF)** under the **FLARE grant 20FL21-201474** at the University of Geneva. Additional financial contributions from **KEK**, **Kyushu University**, **Mainz University**, **Tsinghua University** and the **Heising-Simons Foundation** are also acknowledged

UNIVERSITÉ
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FACULTÉ DES SCIENCES
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FASER

Thank you !

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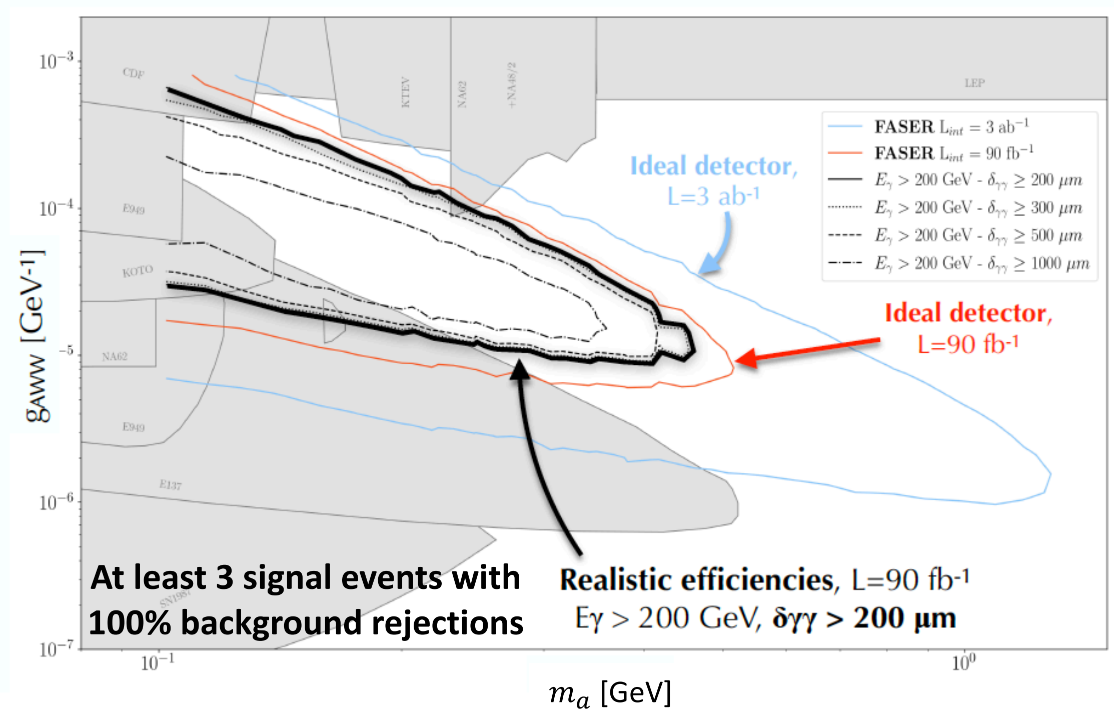
List of publications on the Preshower Upgrade:

- The FASER Detector
  arXiv: 2207.11427: Accepted for publication in JINST
- The FASER W-Si High Precision Preshower Technical Proposal
  CERN-LHCC-2022-006
- Measurements and analysis of different front-end configurations for monolithic SiGe BiCMOS pixel detectors for HEP applications
  F. Martinelli *et al* 2021 *JINST* **16** P12038

Discovery potential for ALP



Ideal detector, L=3 ab^{-1}

Ideal detector, L=90 fb^{-1}

At least 3 signal events with 100% background rejections

Realistic efficiencies, L=90 fb^{-1}
Eγ > 200 GeV, **δγγ > 200 μm**

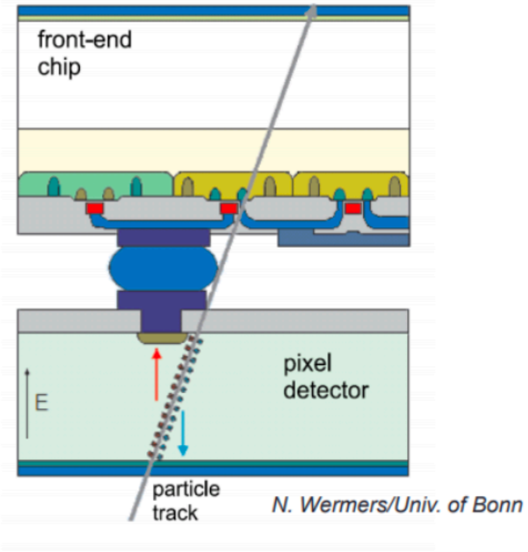
BACKUP SLIDES

Hybrid VS Monolithic Pixel Detectors

ATLAS

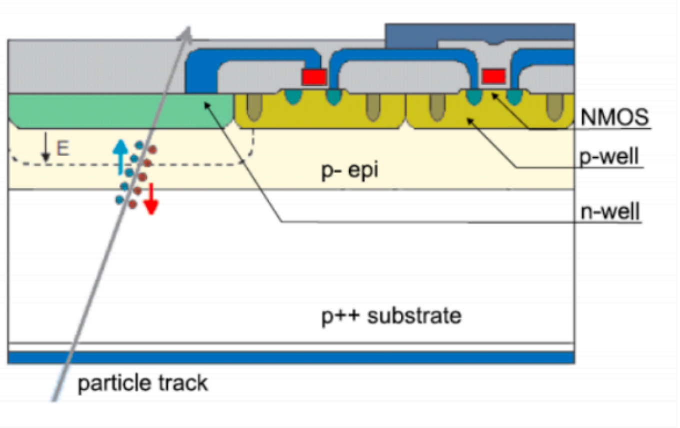
FASER

Hybrid Pixel Detector



N. Wermers/Univ. of Bonn

Monolithic Pixel Detector (example)



cost ratio

Readout chip : sensor chip : bump bonding ≅ 1:2:7

PROS: better optimization of sensors and electronics

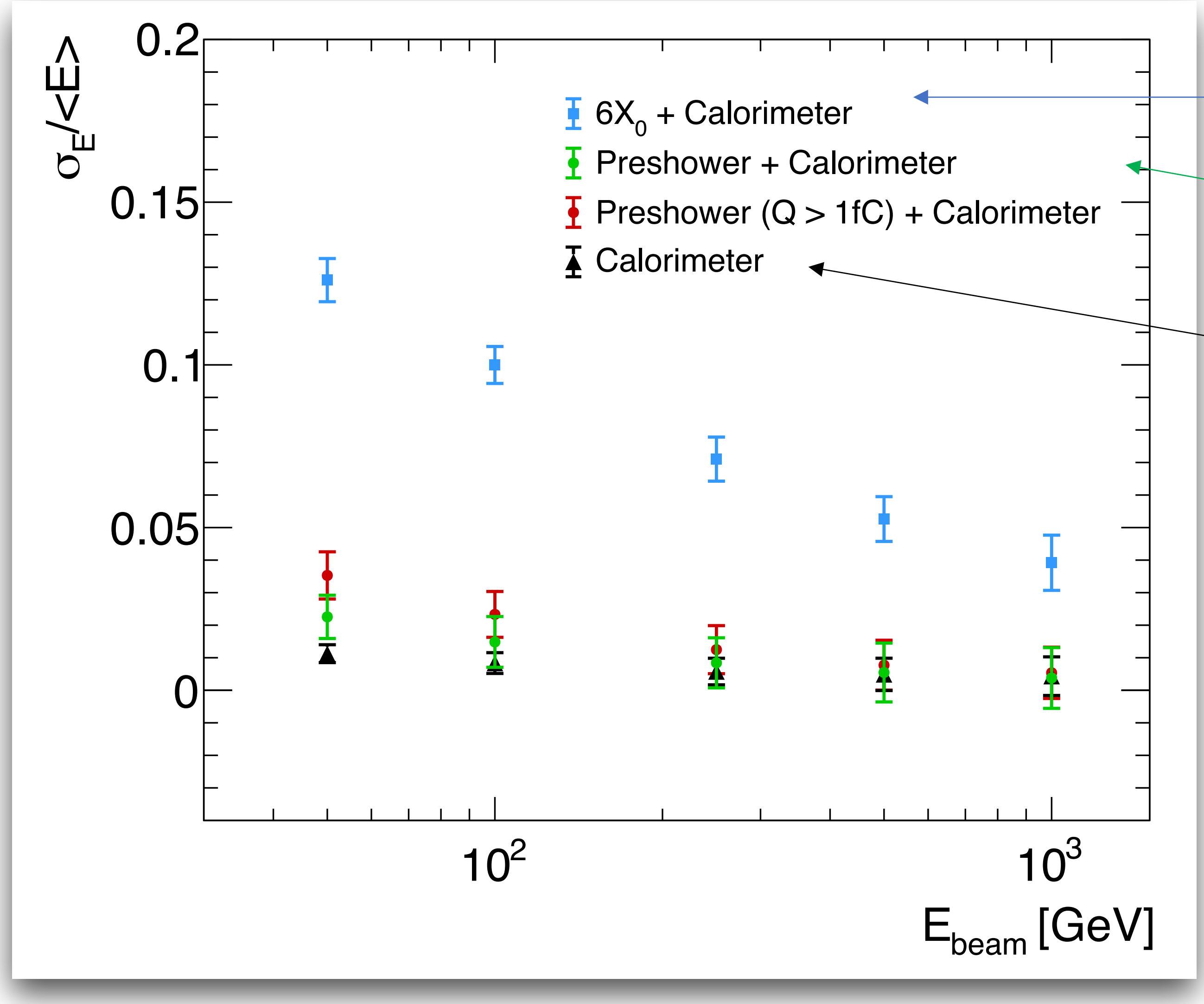
CONS: generally high production costs

Sensor integrated in the readout, **only CMOS processing**

PROS: lower production costs

CONS: more difficult design

Energy resolution



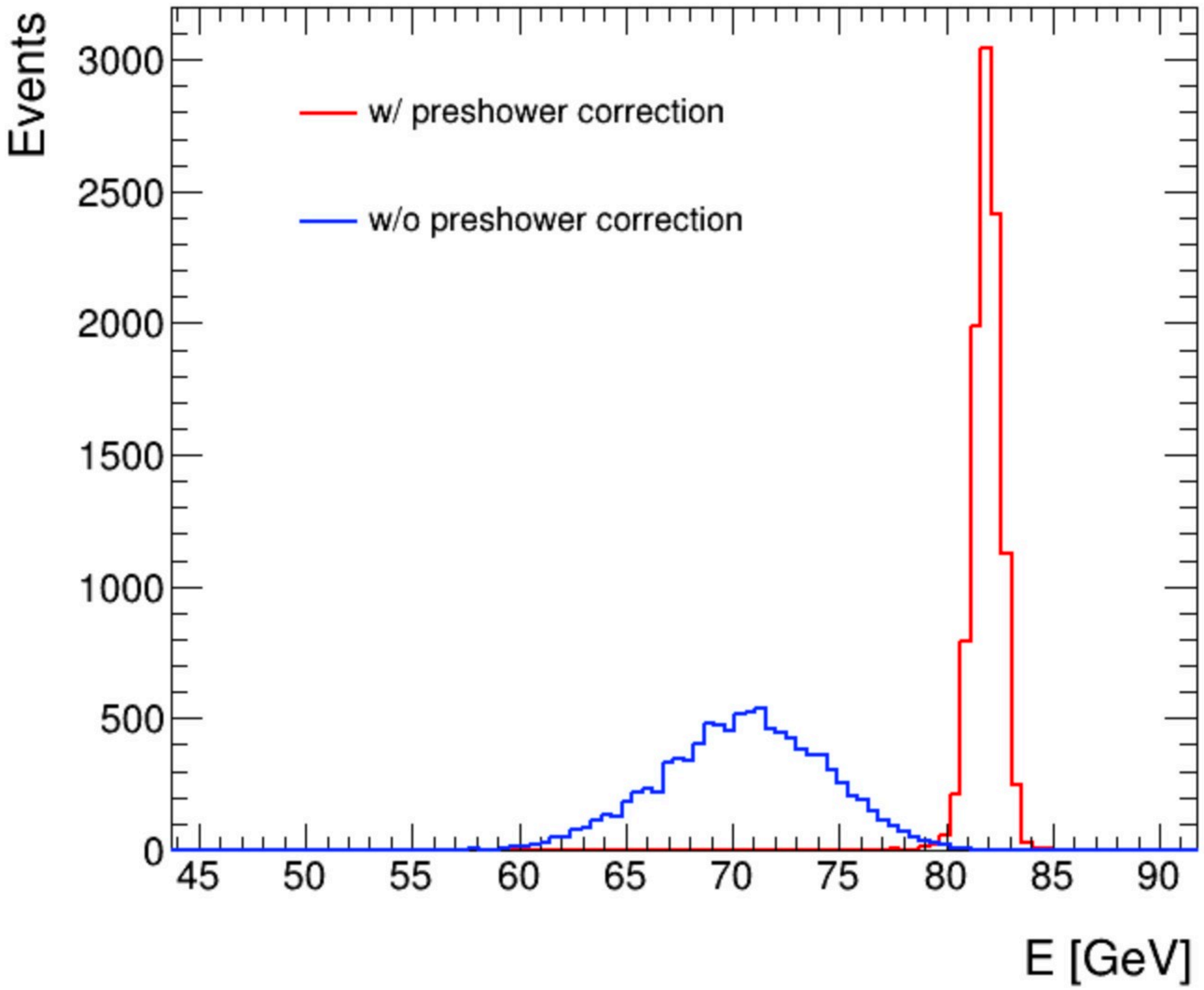
Only looking at the calorimeter
(not using the preshower information)

Correcting with the Preshower measurement

Calorimeter only

Energy resolution

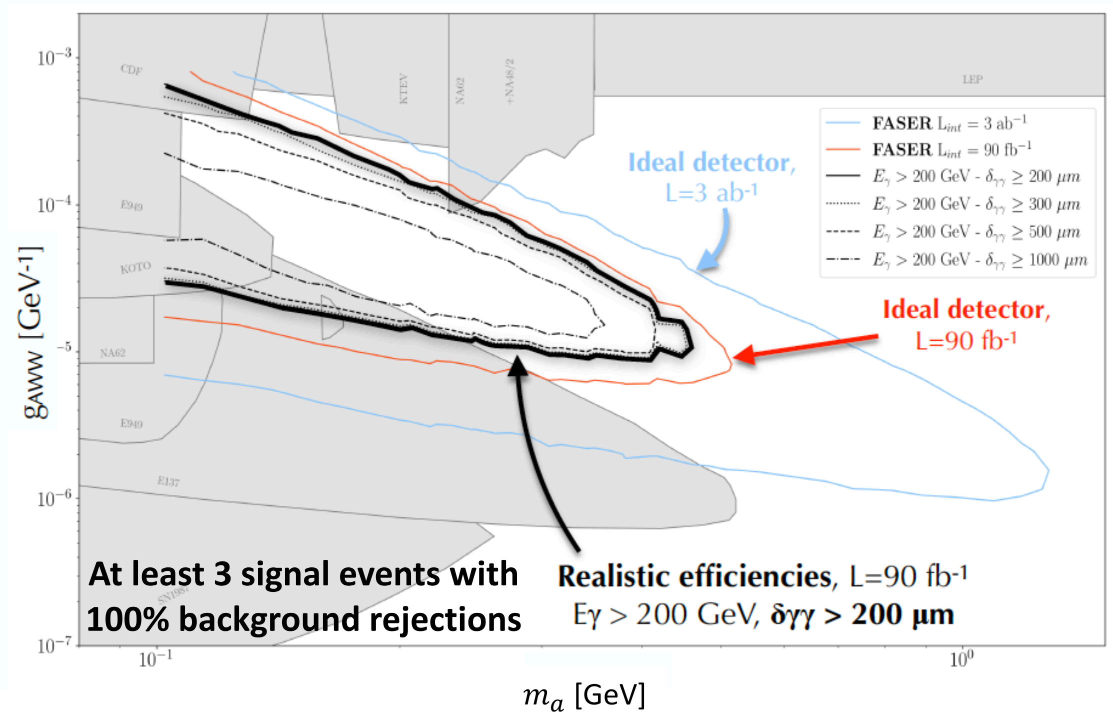
For 500 GeV photons



H. Abreu et al. "The FASER W-Si High Precision Preshower Technical Proposal"
CERN-LHCC-2022-006 ; LHCC-P-023
https://cds.cern.ch/record/2803084

Motivations for a new pre-shower detector

Discovery potential for ALP



Ideal detector,
L=3 ab-1

Ideal detector,
L=90 fb-1

At least 3 signal events with 100% background rejections

Realistic efficiencies, L=90 fb-1
Eγ > 200 GeV, **δγγ > 200 μm**

- **Enables measurements:**
  - Axion-Like-Particles (ALP) produced via aWW coupling
  - LLP with neutral pions in the final state
  - Neutrino background suppression

- **Reinforces measurement:**
  - Dark photon and other LLPs decaying into charged fermions
  - LLP with charge and neutral pions in the final state

Detector requirement:
Discriminate photons down to **200 μm separation** to exploit the full potential of the experiment

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

The FASER Small Prototype Chip (2021)

Purpose

study **different level of INTEGRATION OF THE FRONT-END** electronics inside the sensitive area of the pixels

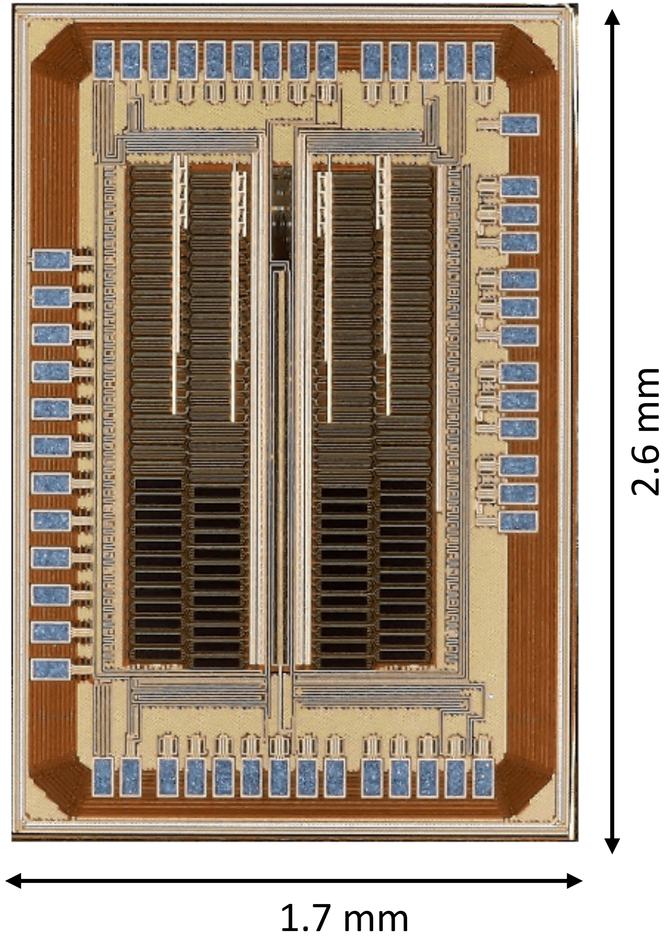
Final aim

identify the BEST FRONT-END CONFIGURATION for the pre-production chip of the FASER Pre-shower (submitted in June 2021)

200 µm x 50 µm PIXELS
shape to reduce the electric field at the edge of the sensitive areas

Tested in 2021

2 superpixels
16x4 pixels each

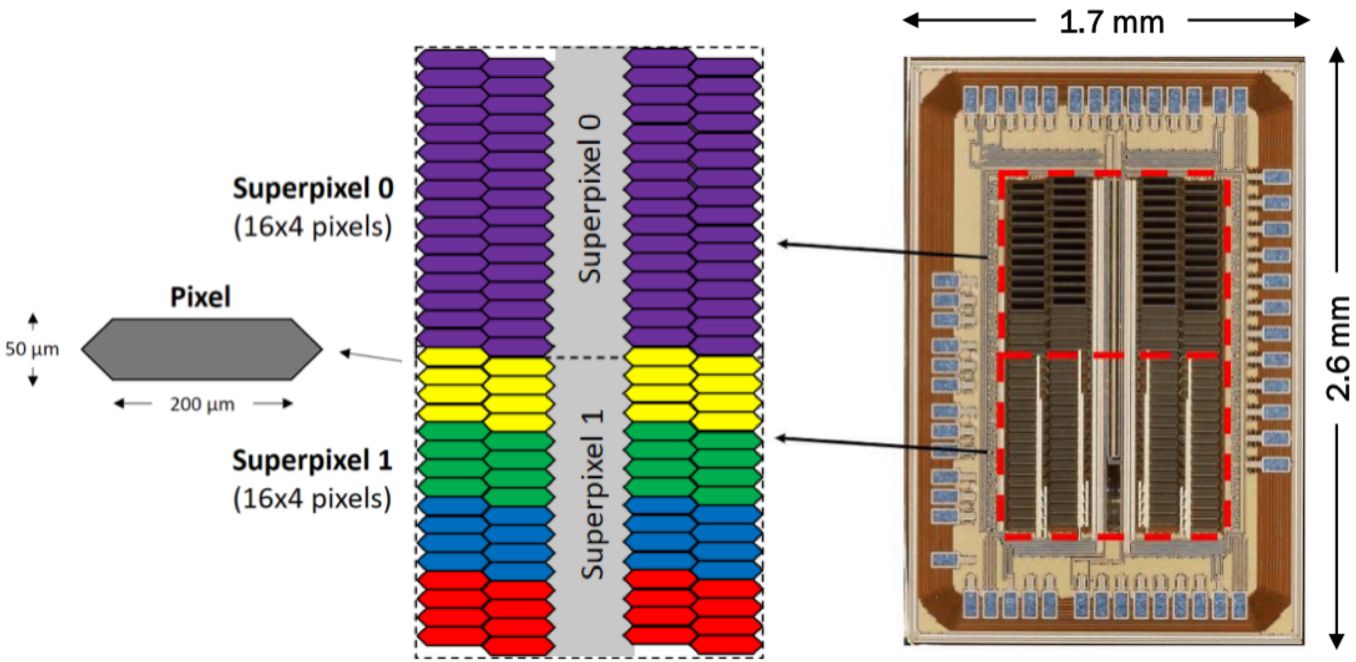


Small Prototype: Front-end Configurations

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

First chip prototype tested in 2021

- designed to study different levels of integration of the front-end electronics
- simultaneous goals: minimize dead area and routing capacitance, maximize stability



From all electronics in pixel

Best expected performance

- 🟥 All front-end system in Pixel
- 🟦 Driver in Pixel, discriminator outside
- 🟩 Everything in Pixel, featuring an inverting stage
- 🟨 Only pre-amplifier in Pixel
- 🟪 All front-end system outside

Backup options for further studies

To all electronics outside pixel

Small Prototype: Results and Comments

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

- 🟥 All front-end system in Pixel
- 🟦 Driver in Pixel, discriminator outside
- 🟩 Everything in Pixel, featuring an inverting stage.
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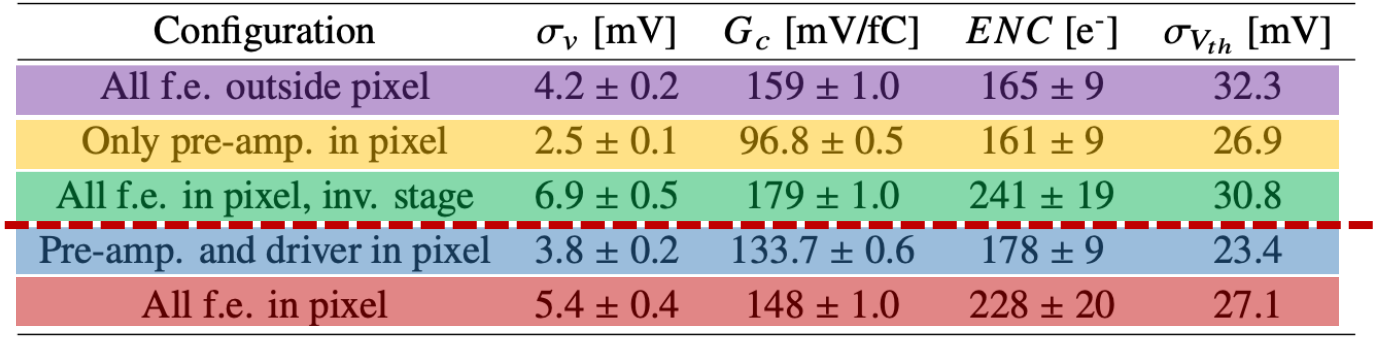
- 🟪 All front-end system outside



Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e$^-$]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1

Last two configurations represent a good compromise between *comptacness* and *performance*: adopted for the pre-production prototype

Pre-production Chip (2022)

Engineering run (IHP Microelectronics)
In each reticle three pixel matrices

FASER_v1 (baseline)

- 4 supercolumns
- in-pixel preamplifier and driver
- discriminator outside

FASER_v2

- 128 x 48 pixels
- 3 supercolumns
- all in-pixel (preamplifier, driver and discriminator)

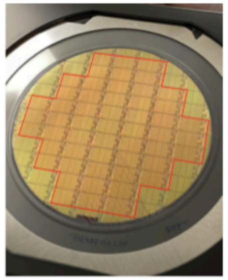
FASER_ALT

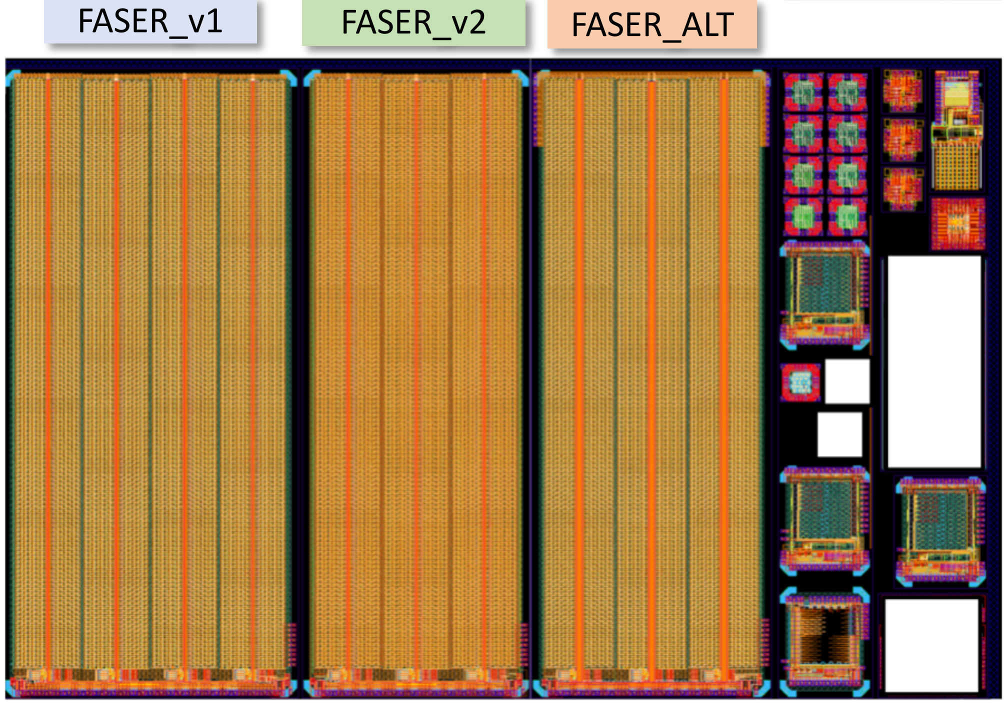
- 128 x 48 pixels
- 3 supercolumns
- no analog memories
- counter for charge measurement

Reticle: 2.4 x 1.5 cm^2

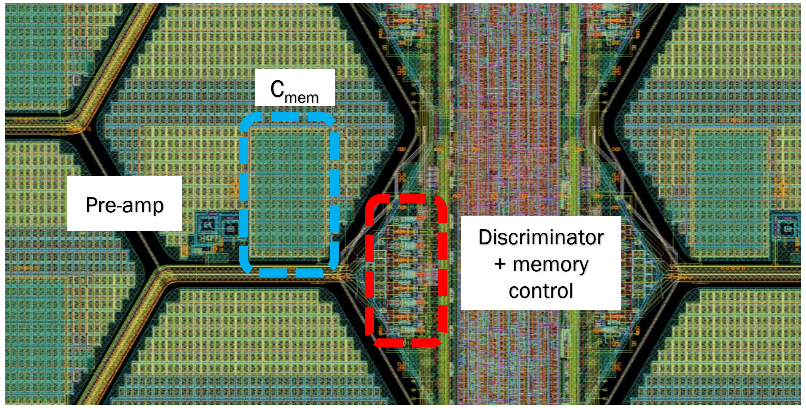
53 reticles per wafer

Thickness 300 µm





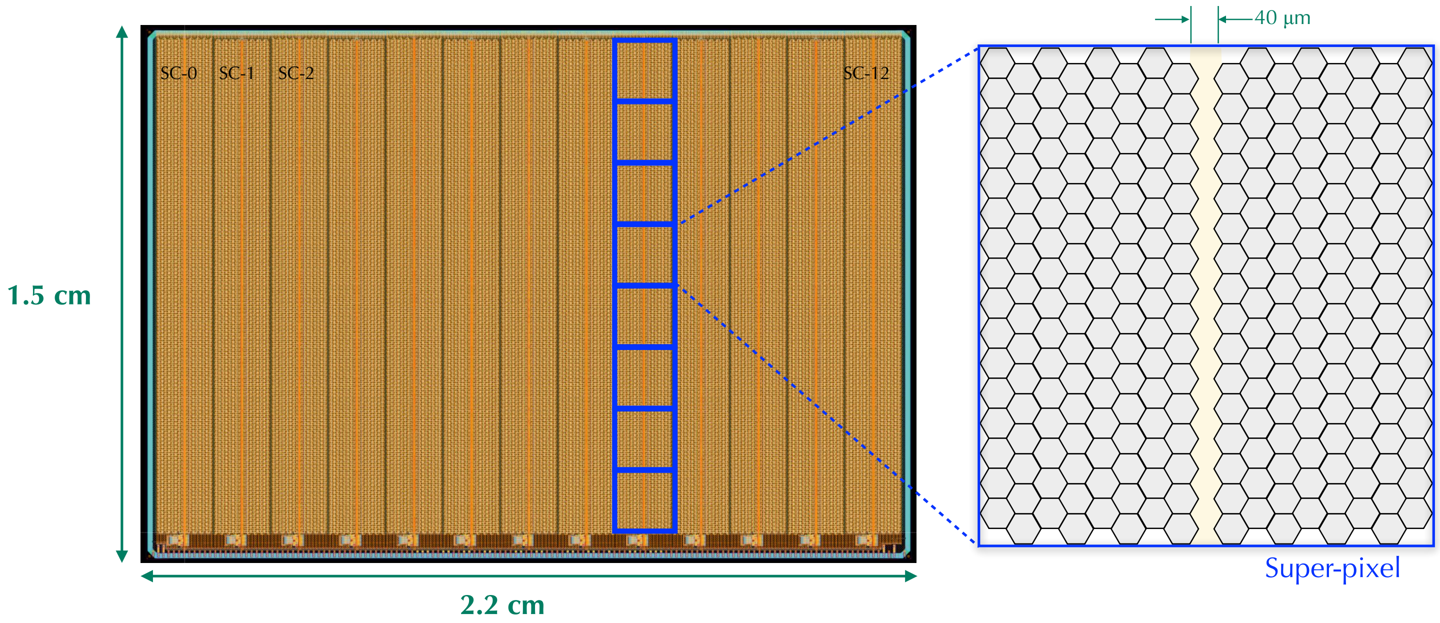
Pre-production Chip (2022)



Chip organized in 13 Supercolumns, each with

- Active region, subdivided into **8 Superpixels** of 16x16 pixels each
- Digital column (40 µm) in the middle: sharing of digital electronics

Digital periphery on the bottom, and multiple guard-ring structures

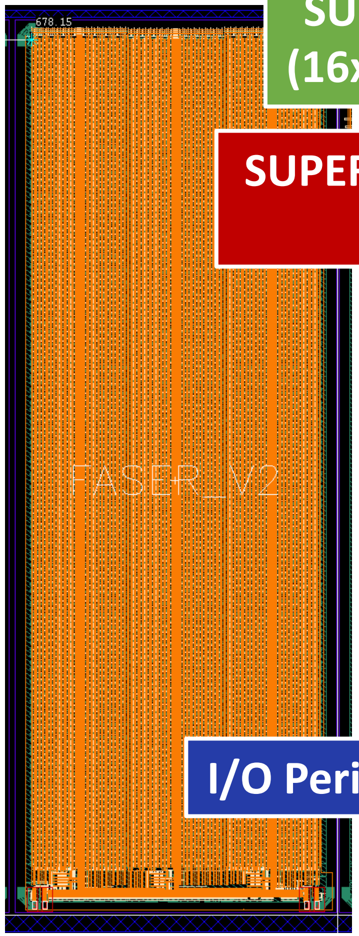


Superpixel:

- 16 rows of 8+8 pixels
- Analog multiplexer
- 4-bit flash ADC
- 3 FAST-OR lines
- Local bias circuit
- Programming logic to mask pixels

Dead area <5%

The Chip Architecture

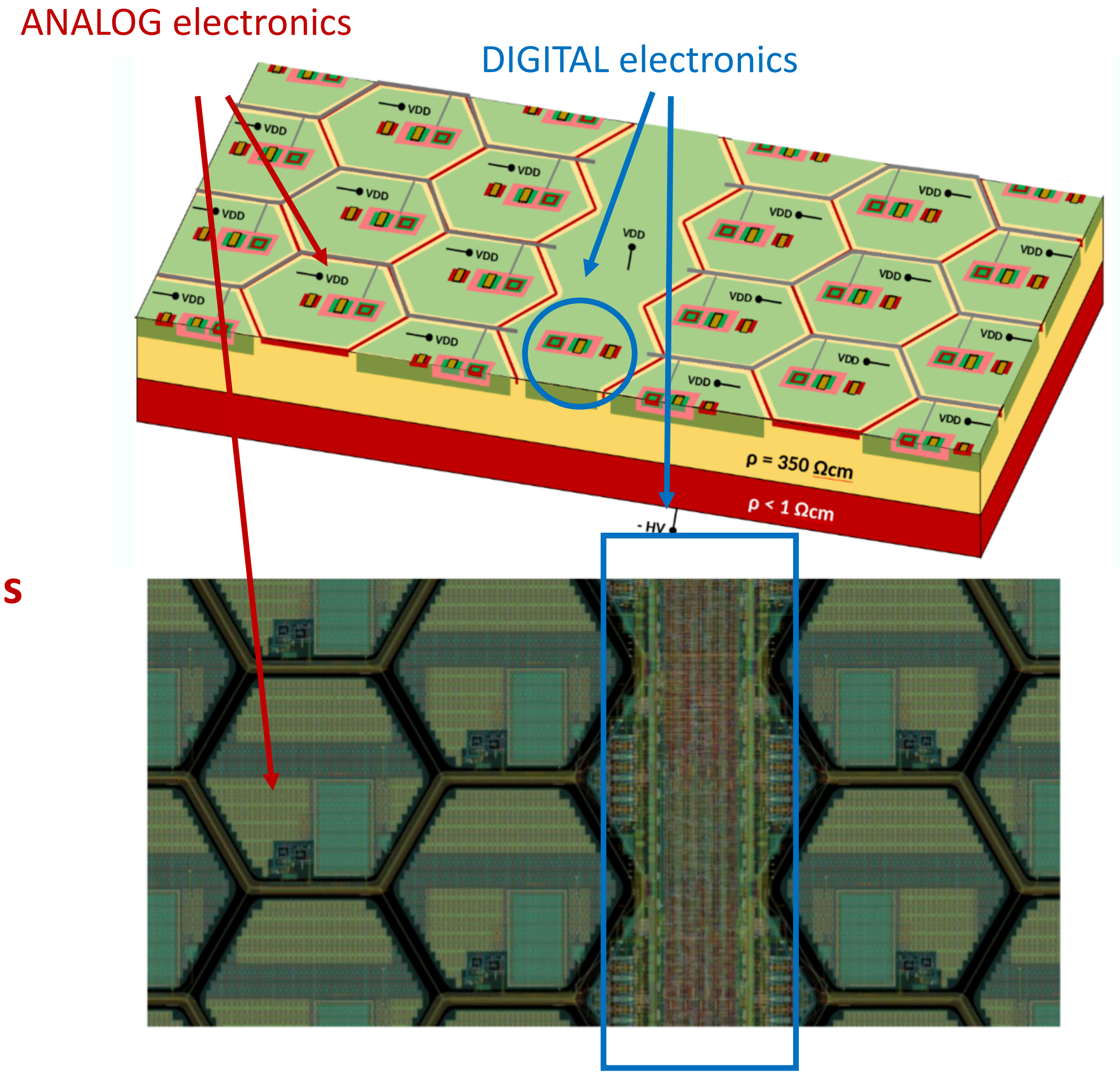


SUPERPIXEL (16x16 pixels)

SUPERCOLUM with READOUT (8 Superpixels)

I/O Periphery

MODULAR ARCHITECTURE
Matrices divided in **super-pixels**
and **super-columns**

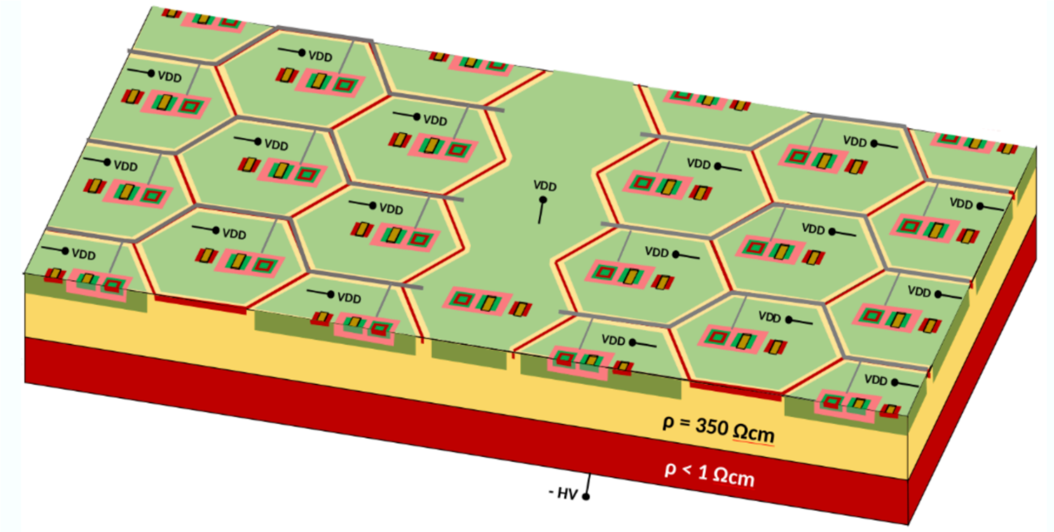


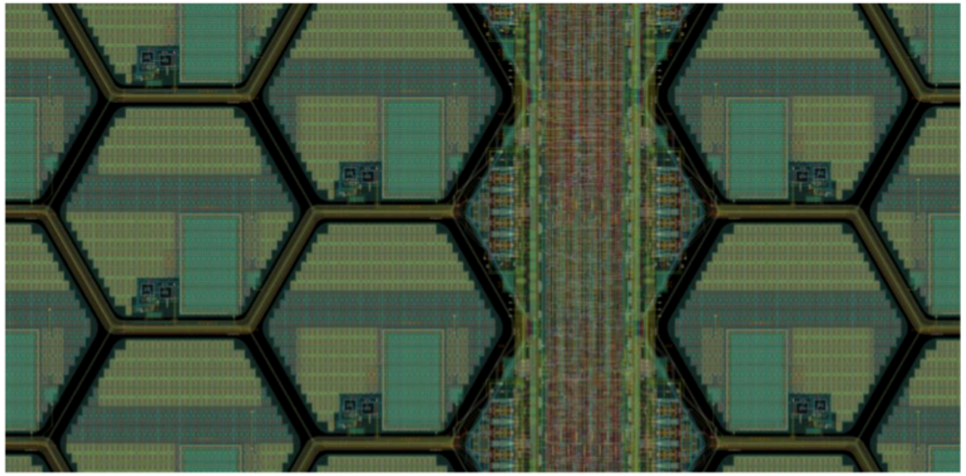
Sensor Cross Section

- Low resistivity heavily p-doped substrate as a support
- Negative high voltage applied to the substrate

- High resistivity 50 µm epitaxial layer
- Triple – well design
- **Analog electronics inside the pixel**
- **Digital electronics outside the pixel**
- Electronics inside the guard ring isolated from substrate using a deep n-well
- Digital electronics in a separate well
- Positive low voltage applied to pixels and electronics deep n-wells

- ≈ 6% dead area in the pixel matrix

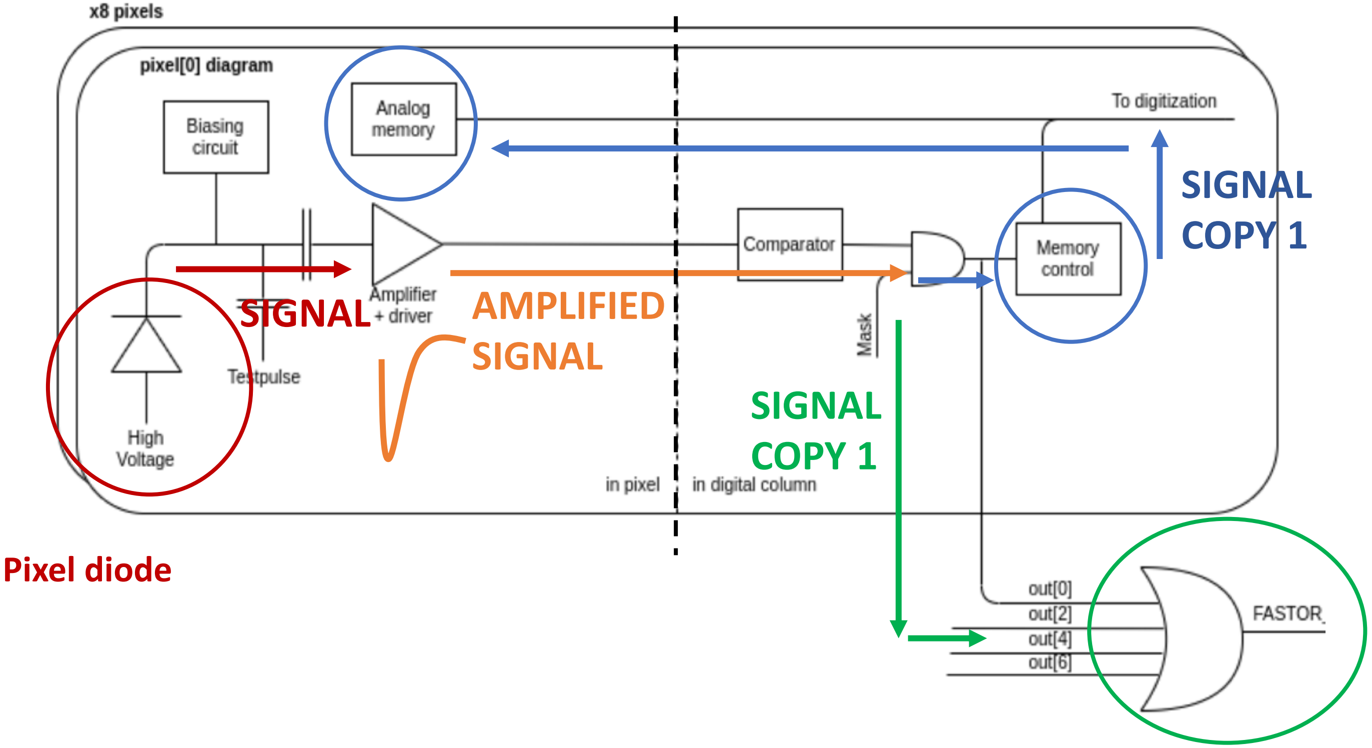




Monolithic Pixel ASIC: Pixel Circuitry

- When an hit arrives a signal is produced
- The signal gets amplified by the PRE-AMPLIFIER
- The signal is sent ouside the pixel to the COMPARATOR
- The output of the comparator is copied:
  - **COPY 1** goes to the MEMORY CONTROL
  - **COPY 2** goes to the FAST-OR that will give the signal to start the Readout
- **Memory Control** loads the analog memory inside the pixel if the charge is over threshold
- After some delay, readout starts supercolumn after supercolumn

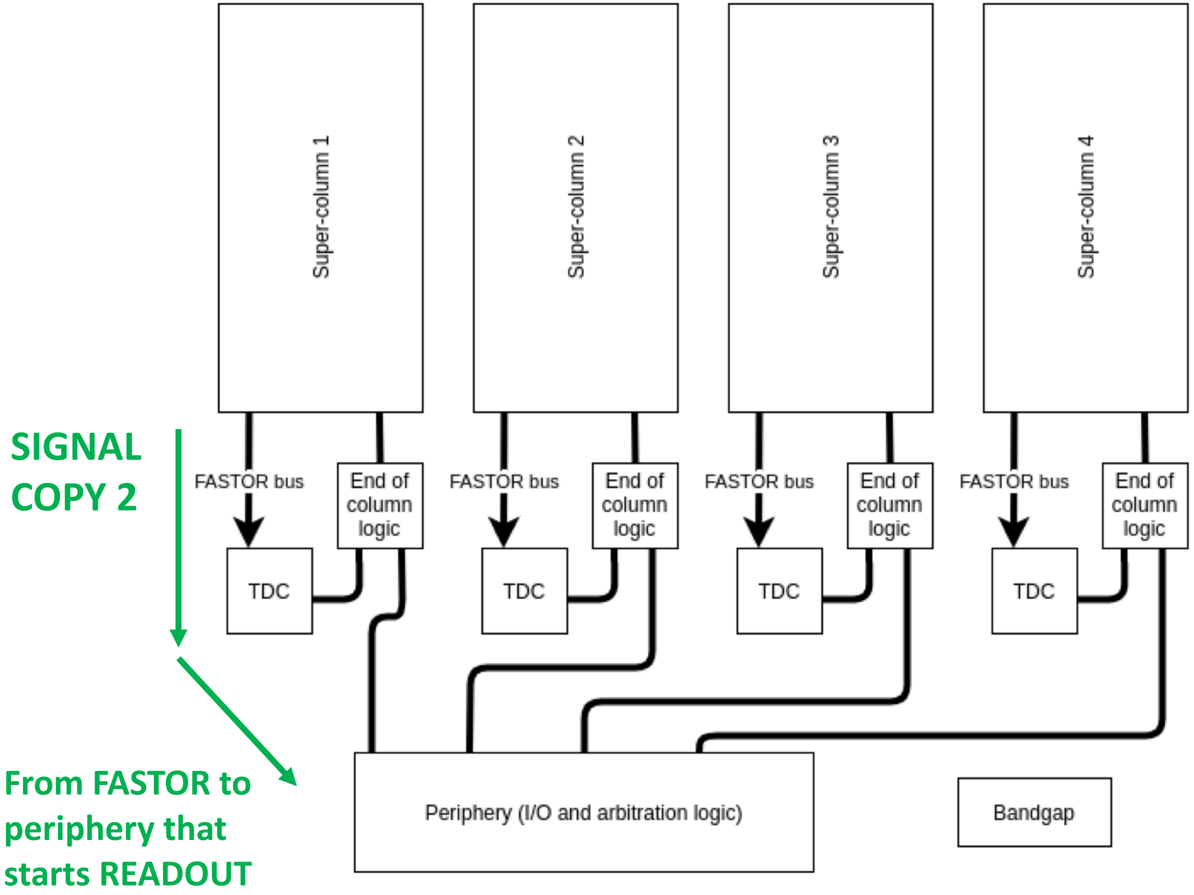
Analog memory INSIDE THE PIXEL where the info of the charge is stored



Pixel diode

FASTOR exit the super-pixel

ASIC Structure and Readout



SIGNAL COPY 2

From FASTOR to periphery that starts READOUT

- A copy of the signal exit **IMMEDIATELY** the pixel through the FASTOR
- Each FASTOR send a signal to the perifery to start the READOUT
- To be sure we collected the charge entirely, the **perifery waits a bit before starting the READOUT**
- **Readout time max 200 µs**
- If in a super-pixel **zero FASTOR** are **active, zero bit are sent to the periphery (optimization)**

Pre-production ASIC Prototype: First Tests

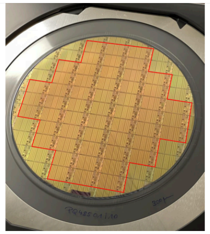
Wafers received in June 2022, tested in the laboratory

- I-V characteristics measured at probe station
- Charge response scrutinised with ^{109}Cd and IR laser
- Stress-tests for digital electronics and readout

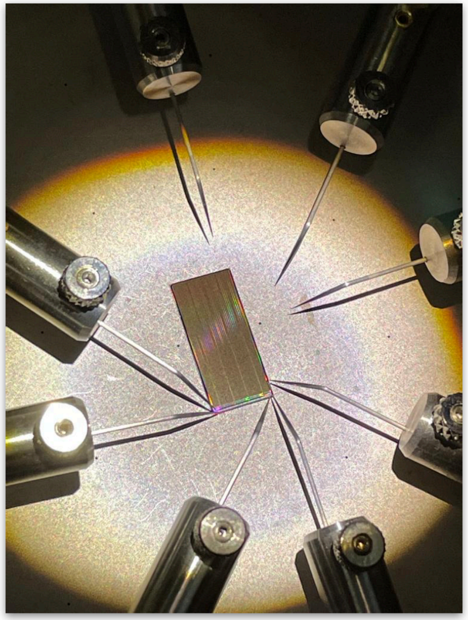
Reticle: 2.4 x 1.5 cm^2

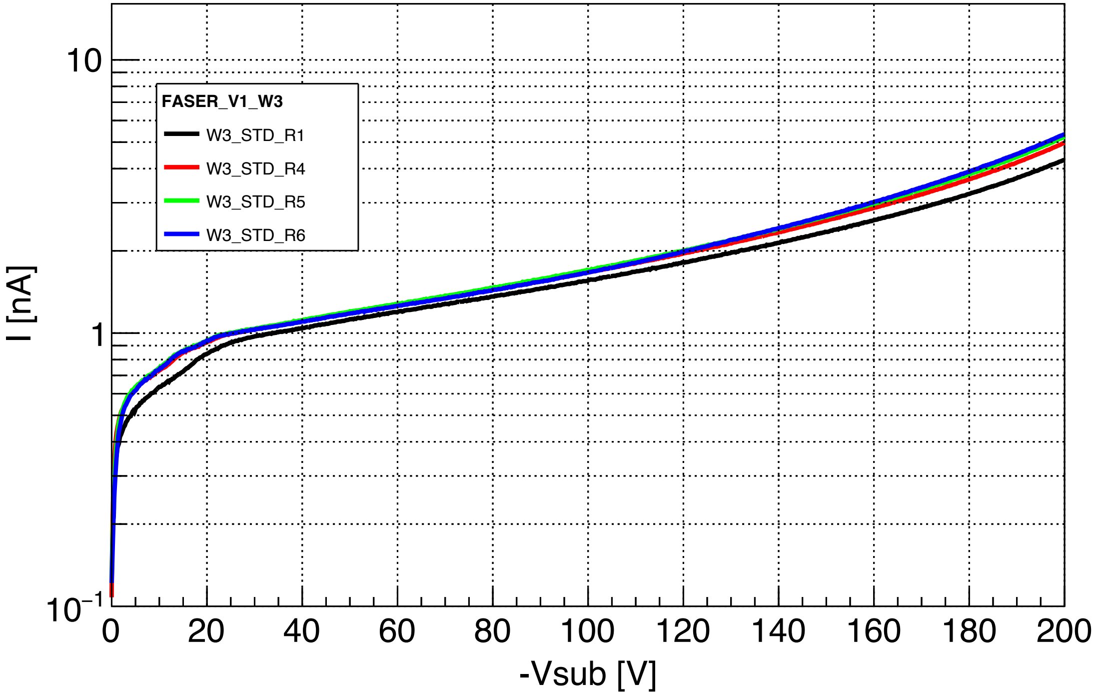
53 reticles per wafer

Thickness 300 µm



CHIP @ probe station





The chip can operate up to -200 V

The LHC Forward Physics

- Most LHC detectors sensitive to transverse particles coming from head-on pp collisions
- **Large forward cross section currently wasted and not probed**

- Forward particles are **highly collimated**: only ~ 1cm spread for 100 m longitudinal travel
- **A small detector far away could potentially see a large flux of Long-Lived Particles (LLPs) with very small background**

- ForwArd Search ExpeRiment
- Proposal submitted in 2018 and approved by Cern in March 2019

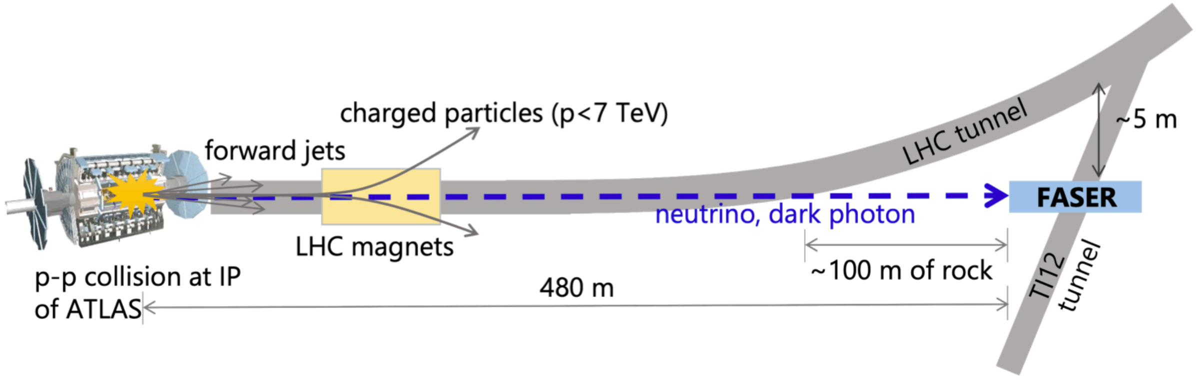
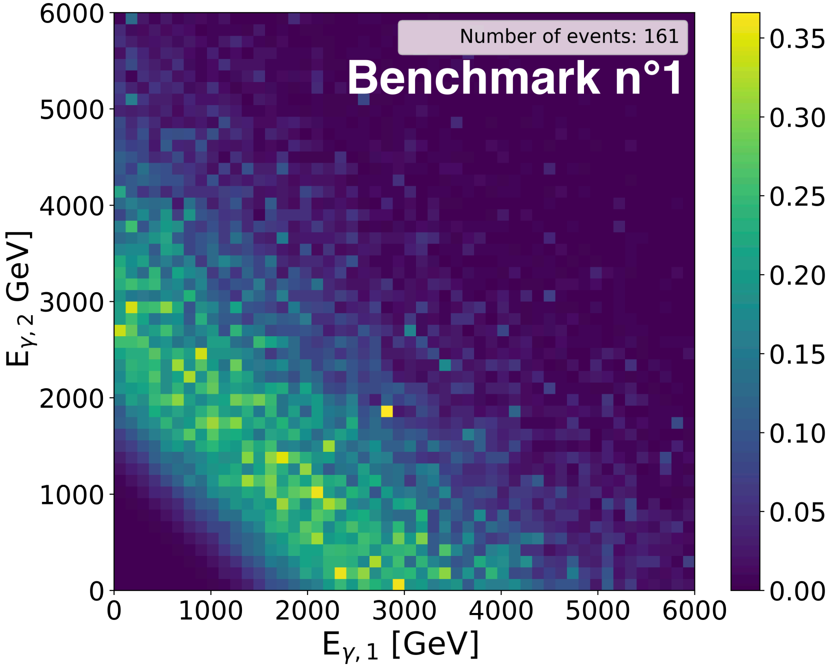
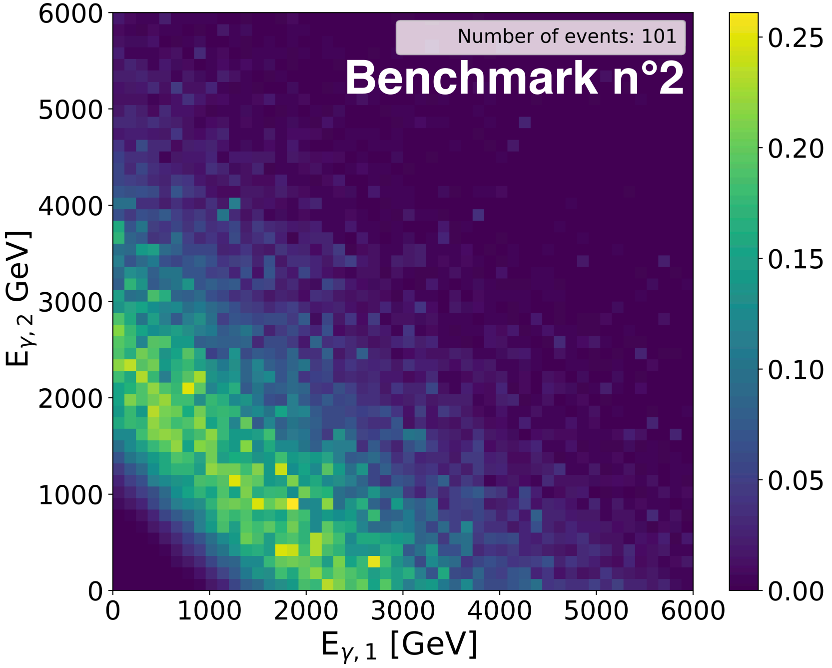
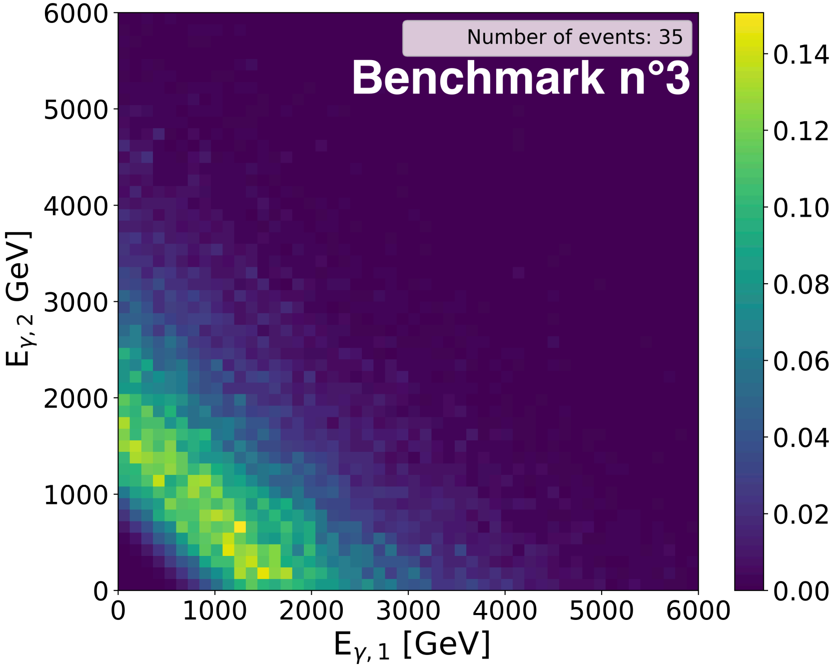


Figure: Location of FASER in the tunnel - schema is not in scale.

Di-photon Signal Energy Distributions

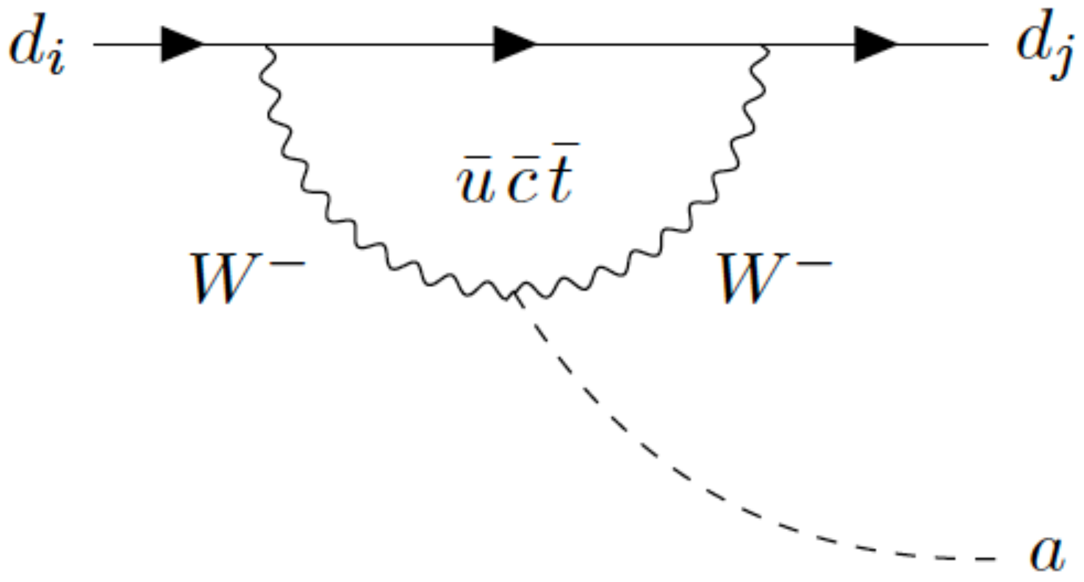






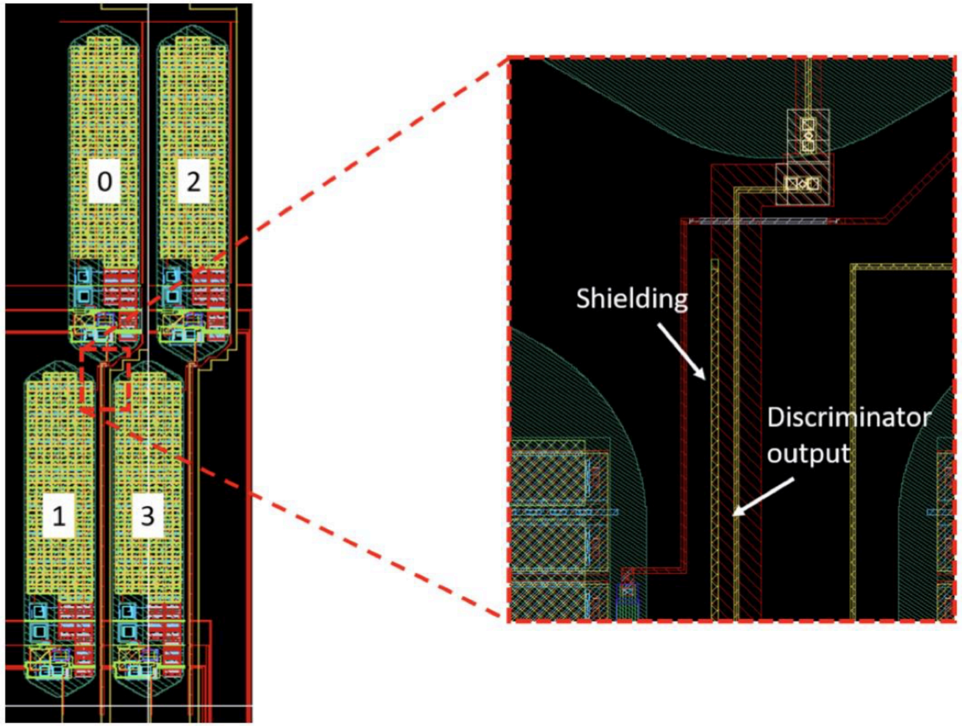
ALPs Production: FCNC

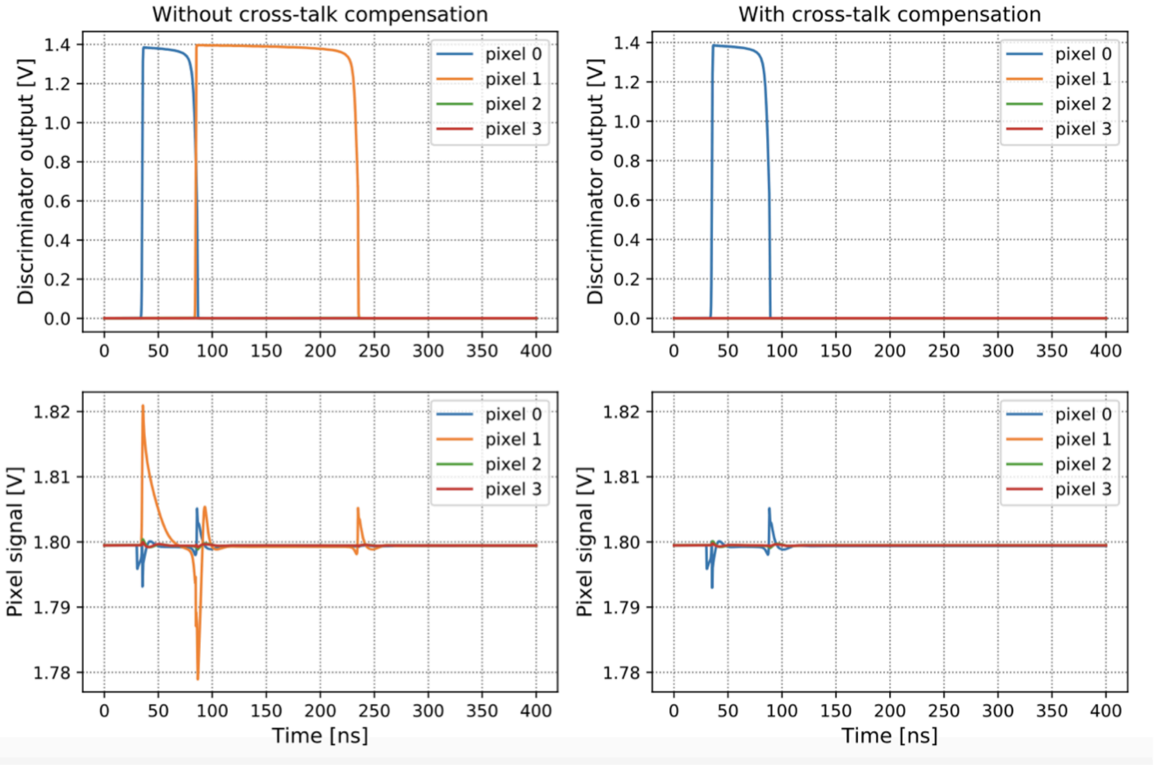
- Down type quark becomes an up type quark
- Emits a charged boson which will itself radiate an ALP
- It then interacts with the up type quark which changes flavor again to become a down type quark



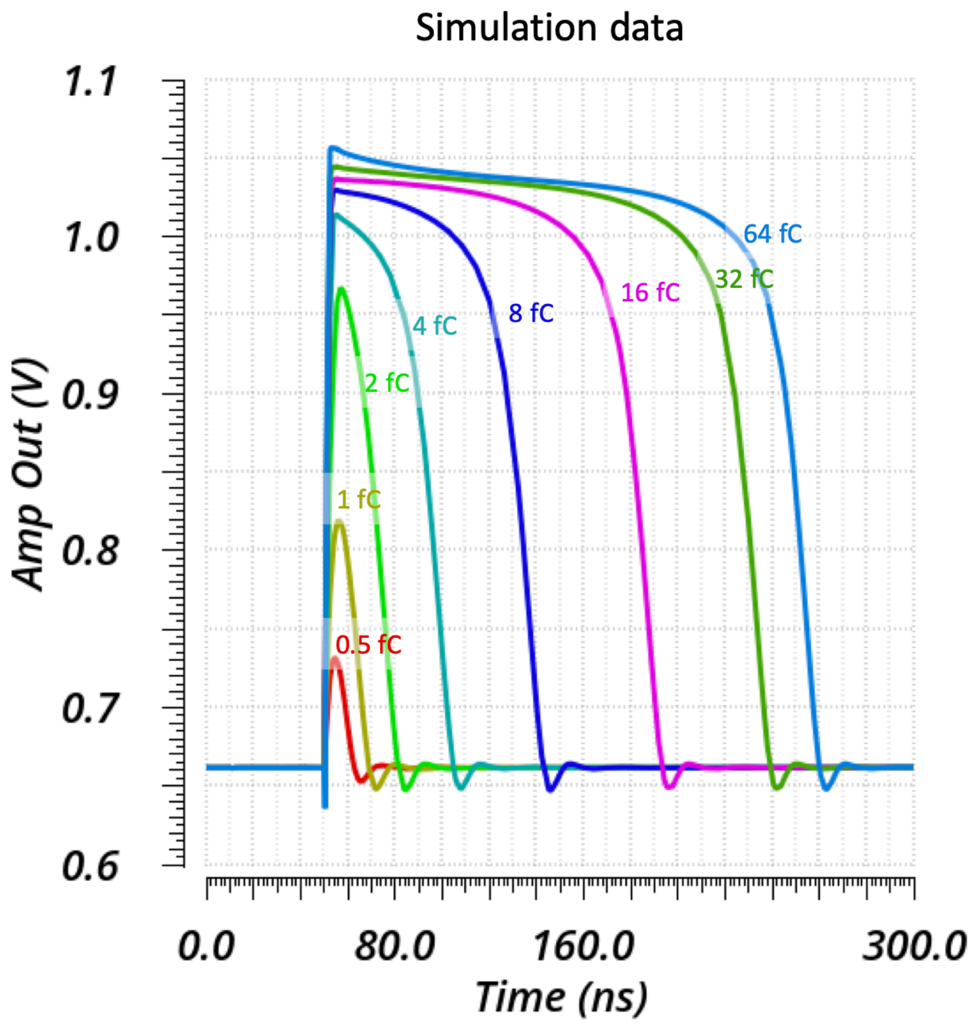
Signal Routing and Crosstalk Suppression

- Signal routed in a **shielded bus** to **minimize crosstalk between neighboring pixels**



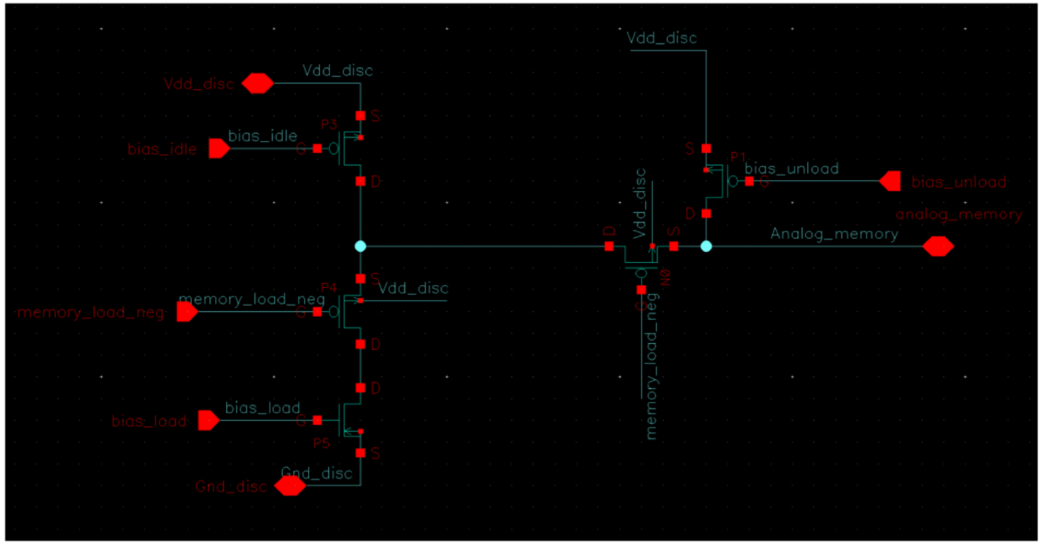


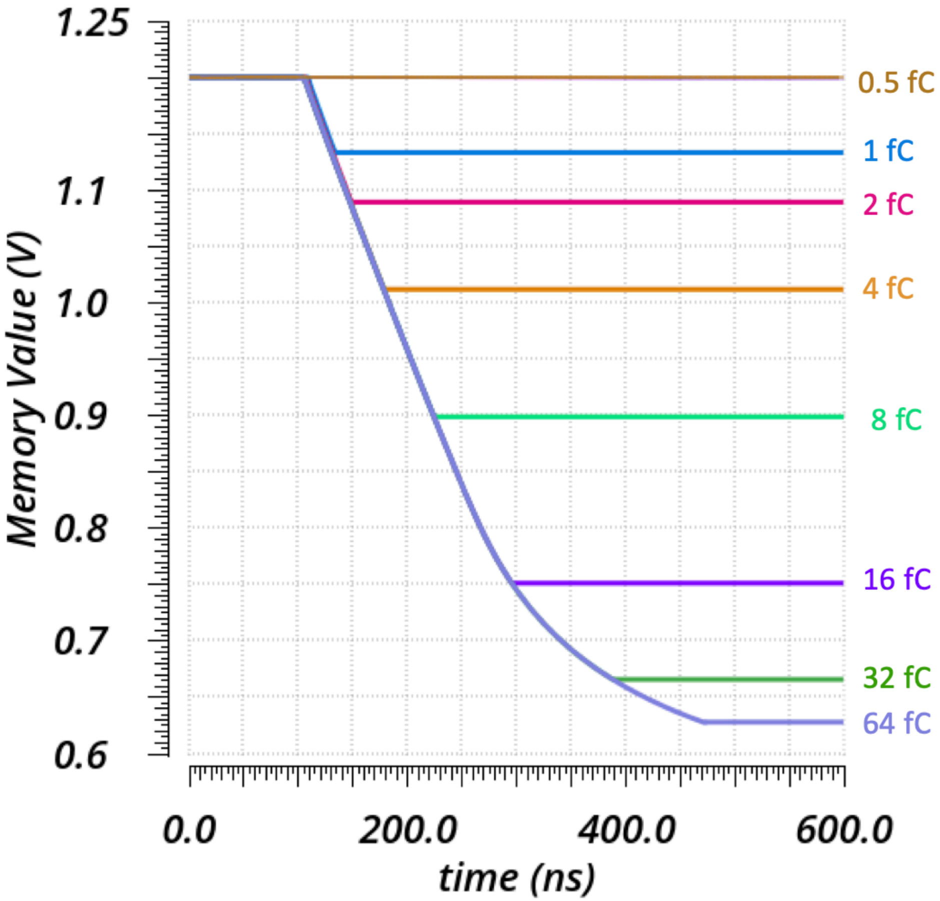
Amplification Stage



- Since we want to measure high charges we convert the charge information to Time Over Threshold
- **For different charges, if the charge increases also the TOT increases but not linearly (almost logarithmic relation)**
- **Saturation at 64 fC (intrinsic saturation of the pixel)**

Memory Control and Analog Memories





- ○ When signal returns below threshold, memory is disconnected and left floating until read by the flash ADC
- ○ Current leakage even if the switch is opened
- ○ It takes 200 µs to degradate the memory value of 30 mV (= 1 bin of our ADC)

After 200 µs we still measure something but we are less precise

Di-Photon Reconstruction Efficiencies

$E_{\gamma 1}$= 1 TeV
$E_{\gamma 2}$= 1 TeV