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Obtaining requirements for the future ATLAS Event Filter Tracking system

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The High-Luminosity LHC shall be able to provide a maximum peak luminosity of 5×10^{34} $cm^{-2}s^{-1}$, corresponding to an average of 140 simultaneous p-p interactions per bunch crossing (pile-up), at the start of Run 4, around 2028. The ATLAS experiment will go through major changes to adapt to the high-luminosity environment, in particular in the DAQ architecture and in the trigger selections. The use of the new high-resolution full-silicon inner tracker (ITk) in the high-level-trigger (also called Event Filter) is of paramount importance to improve the trigger selection and purity and reduce the trigger rates against the large background of low-energy pile-up jets. The Event Filter Tracking system is under design as an heterogeneous and flexible system, able to combine algorithms running in CPUs and on accelerators, like FPGAs and/or GPUs, on commodity servers, to allow both a regional reconstruction at the expected 1MHz L1 rate and the full event reconstruction at 150 kHz. The challenge of the Event Filter Tracking design is to maximize the tracking performance of the algorithms while maintaining an adequate data throughput through the processors farm, using reasonable power. In this presentation, the results of studies performed to evaluate the minimal tracking performance required are presented. In particular, the tracking efficiency and the resolution on the track transverse momentum will impact the leptons selections, while the resolution on the track impact parameters will affect the hadronic selections, including b-tagging and multi-jet selections.

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