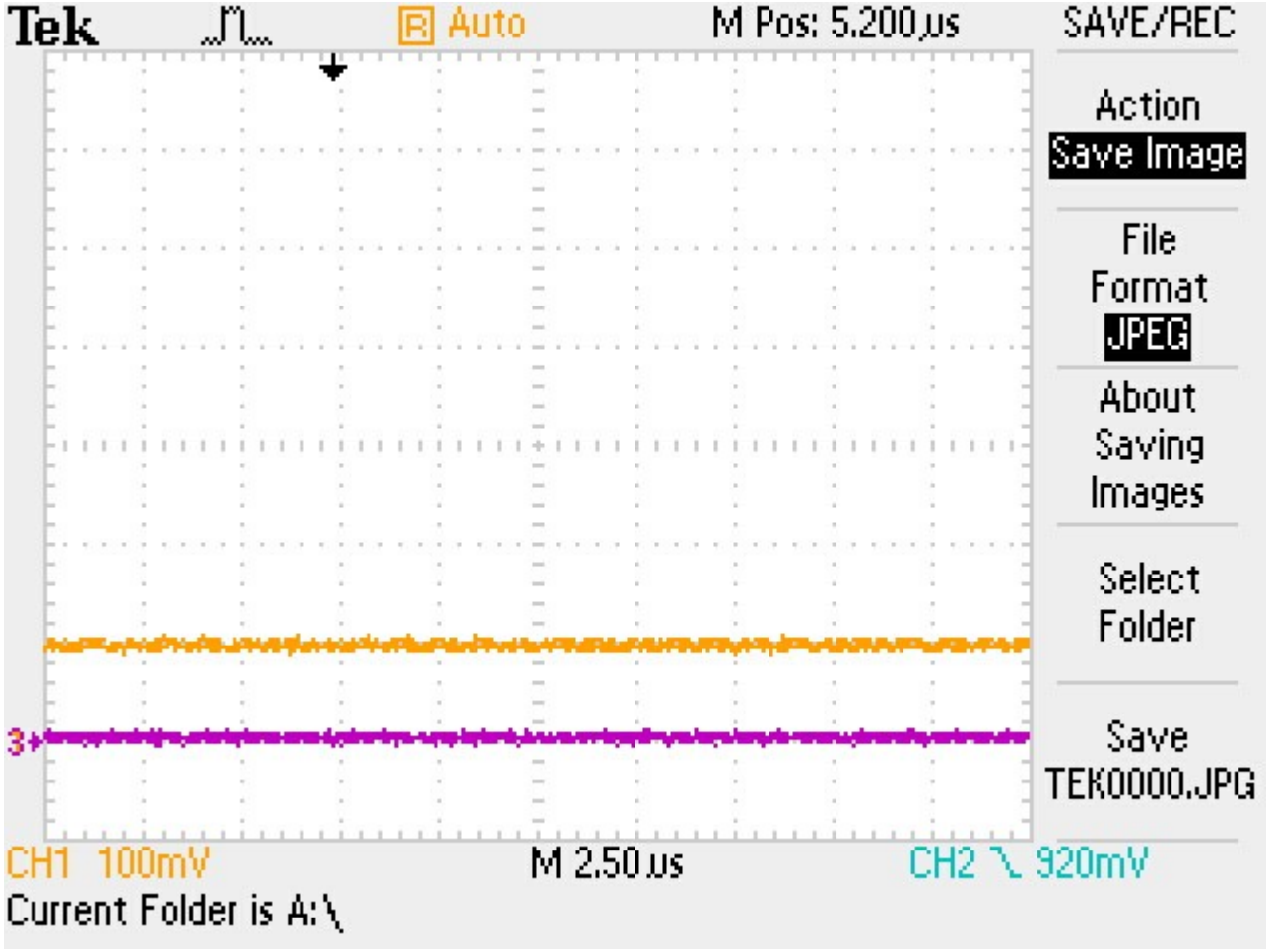
RD50-MPW3 NOISE MEASUREMENTS

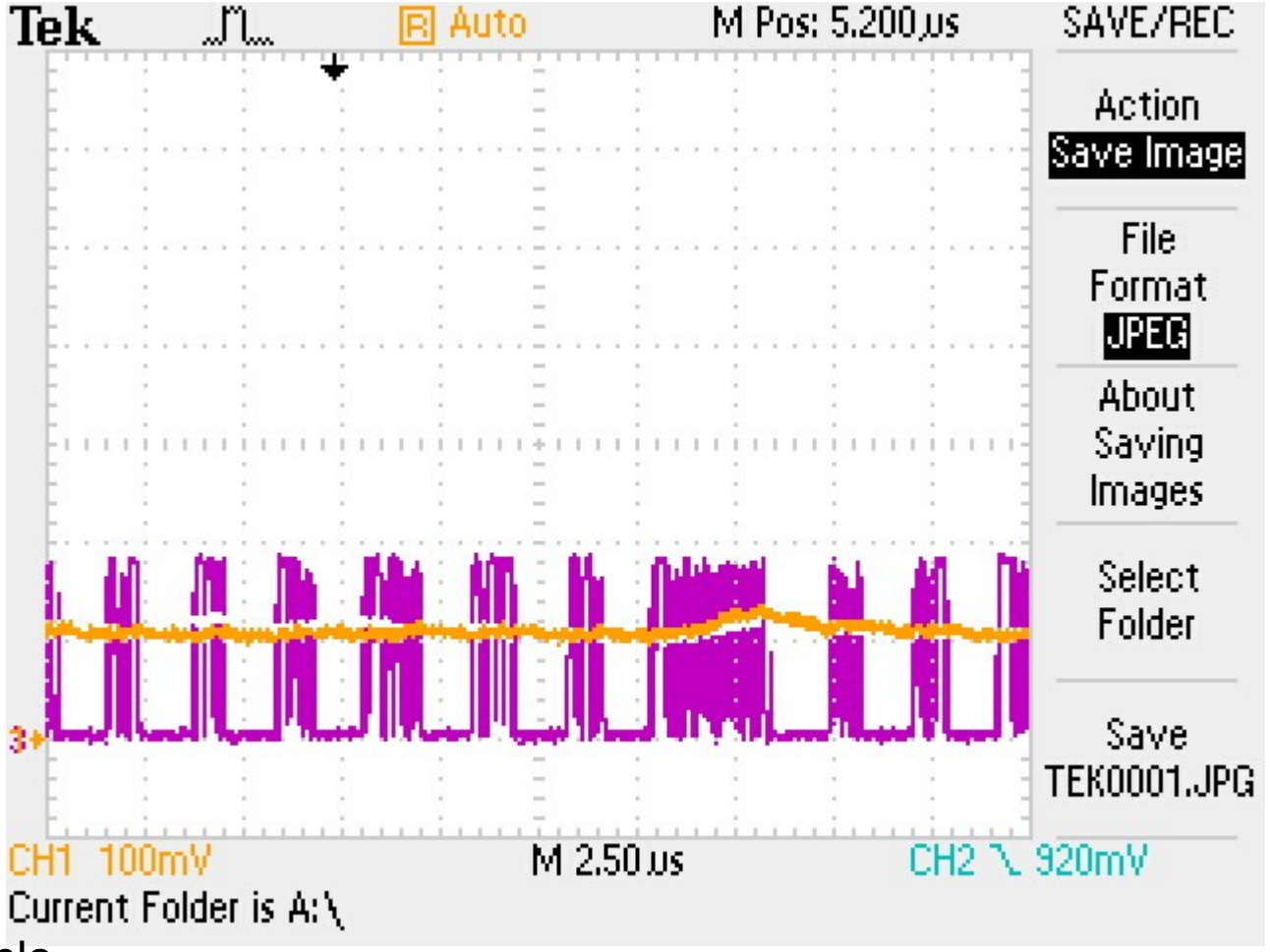
09/02/23

RD50-MPW3 – No clock and no comparator activity



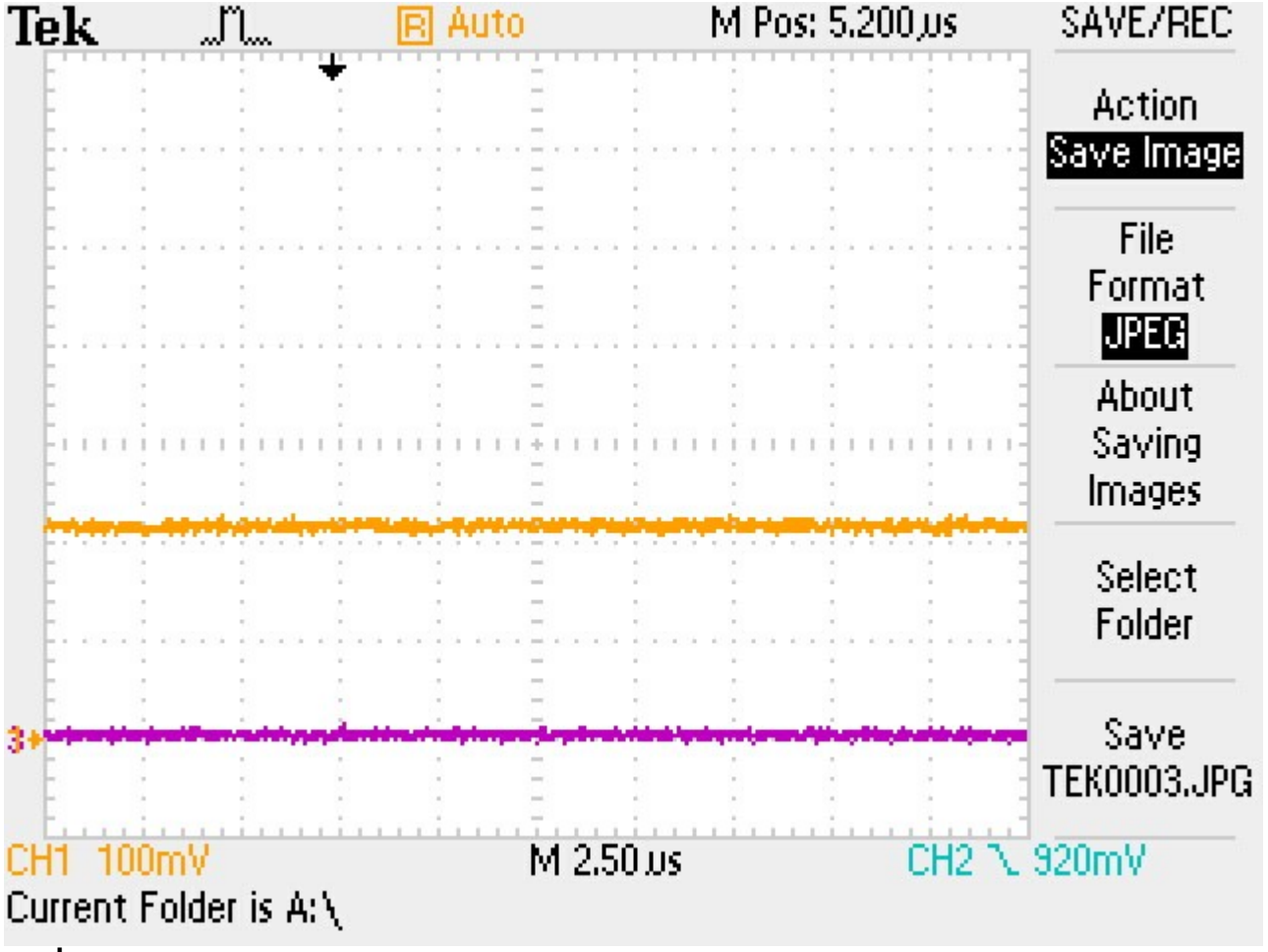
- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 100mV

RD50-MPW3 – No clock with comparator activity



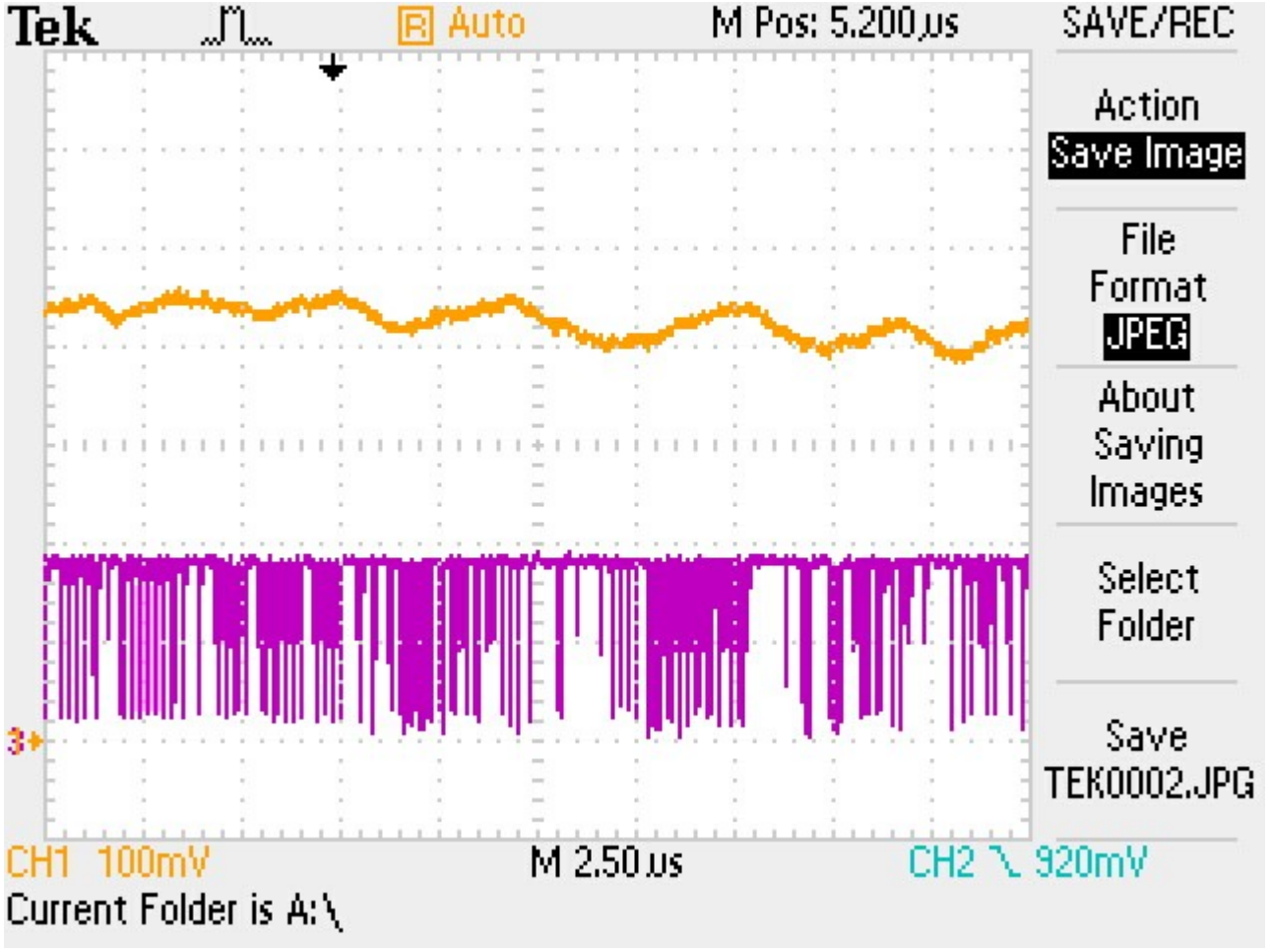
- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 100mV (no significant change but some “charging” of SFOUT during comparator activity)

RD50-MPW3 – With clock and no comparator activity



- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 220mV (increase in offset compared with no clock)

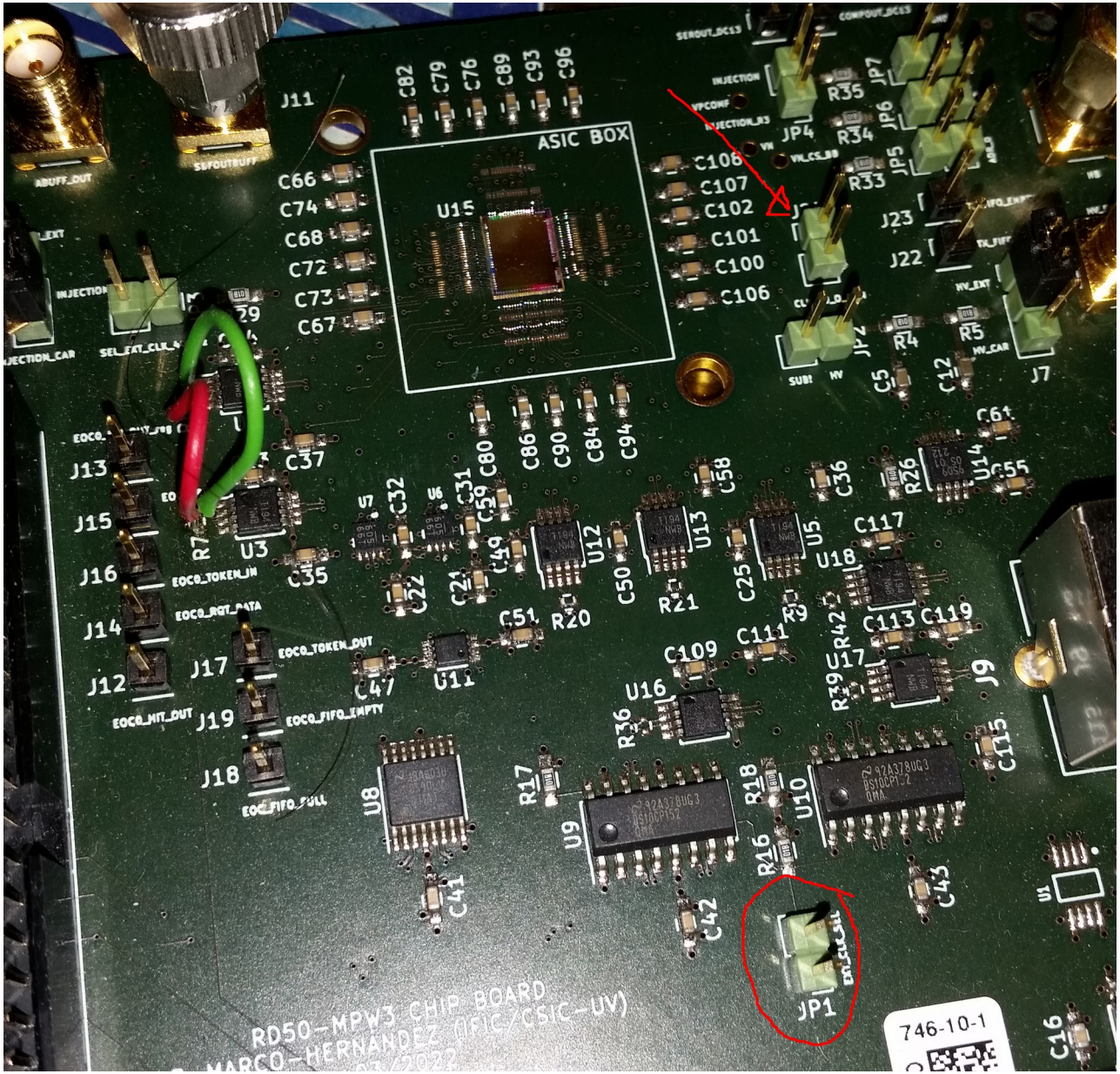
RD50-MPW3



- Compout = purple
- SFOUT = yellow
- DC offset of SFOUT ≈ 420mV

RD50-MPW3 – Clocking

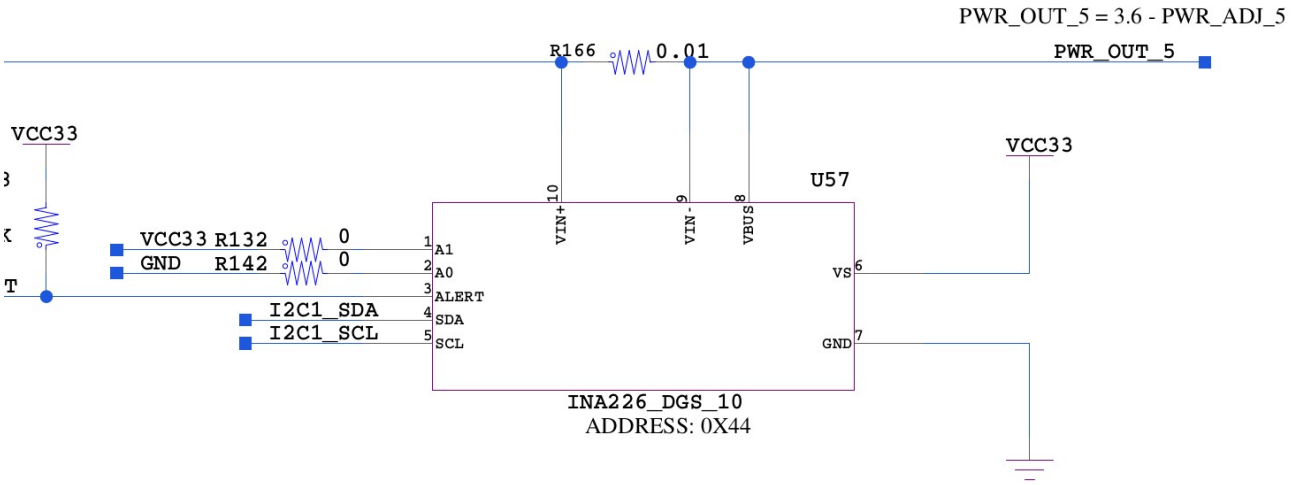
- Firmware modified – DCM added to output different frequencies and duty cycles on external 40MHz clock input to chip
- Chip programmed with JP1 in place (external 640MHz input pin clock used)
- JP1 removed (external 40MHz clock input to chip now used)
- Chip clock monitored on clk_40MHz_p output pin from chip

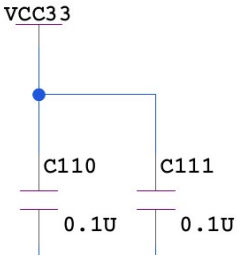


RD50-MPW3 – Clocking

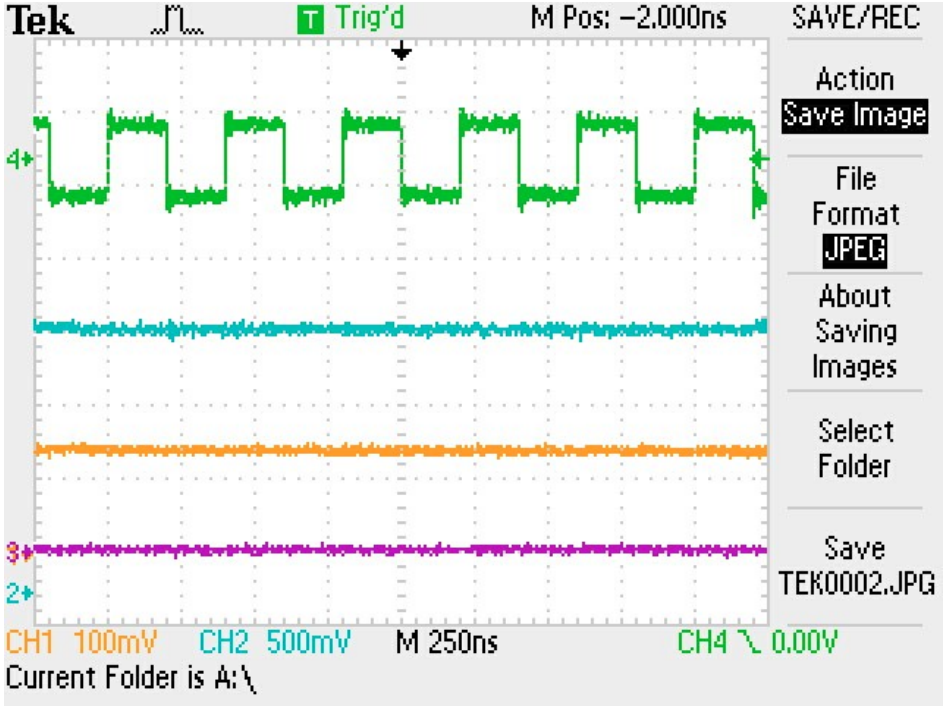
- Current of each supply voltage from caribou measured by reading differential voltage across series resistor
- INA226 ADC used to measure voltage
- I = V(+) - V(-)/ R166

Total chip current (GND current) = $I_{(VDDA)} + I_{(VSSA)} + I_{(VDDC)} + I_{(VDD!)} + I_{(Nwell\ ring)} + I_{(vsensbias)}$





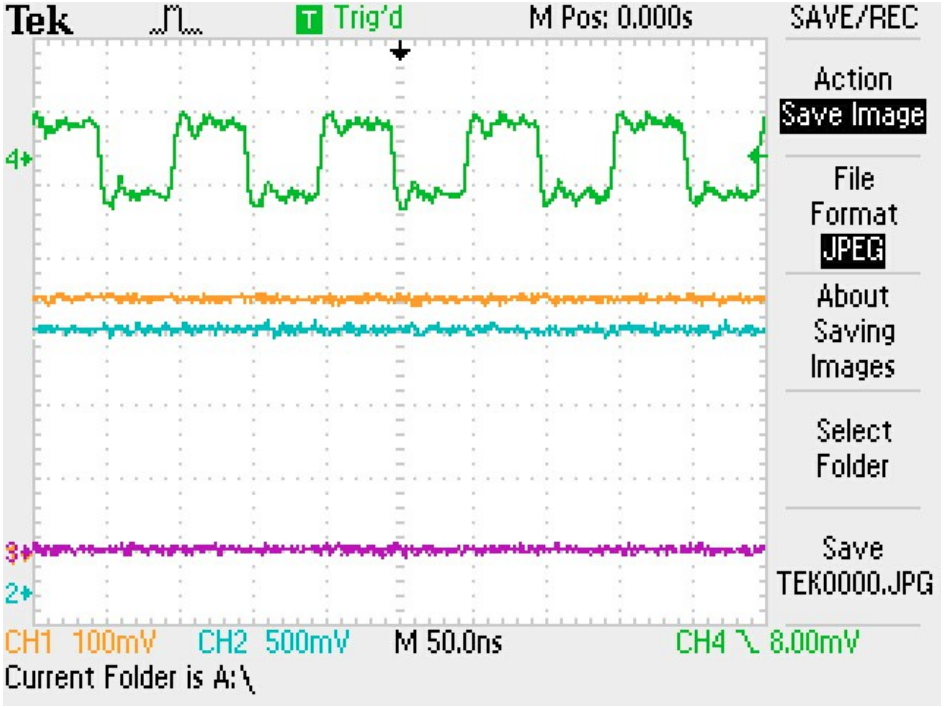
RD50-MPW3 – External clk 2.5MHz 50% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	87.5	8.75
VSSA	15	1.5
VDDC	232.5	23.25
VDD!	1195.0	119.5
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	155	15.5
Total chip GND current		153

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 139mV

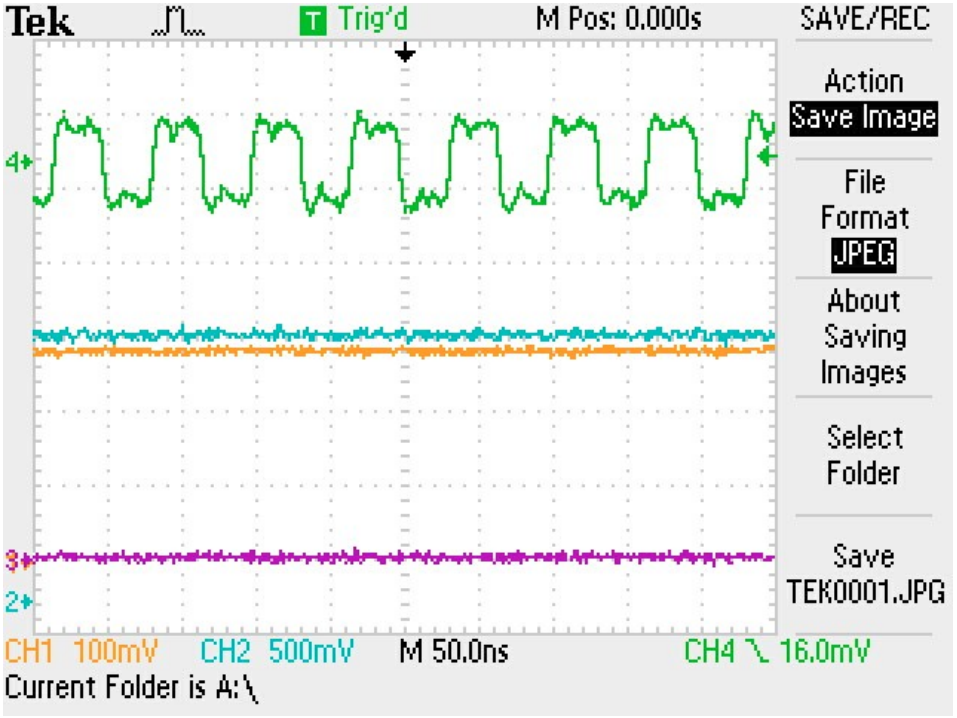
RD50-MPW3 – External clk 10MHz 50% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	125.0	12.5
VSSA	17.5	1.75
VDDC	237.5	23.75
VDD!	1312.5	131.25
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	152.5	15.25
Total chip GND current		169.25

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 355mV

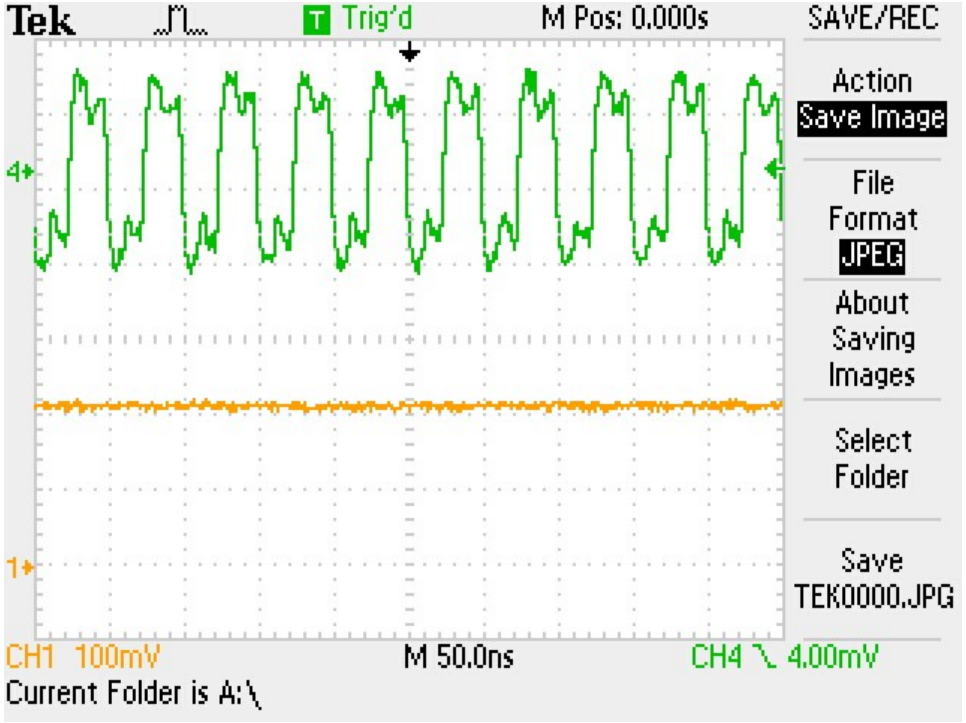
RD50-MPW3 – External clk 15MHz 50% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	130	13
VSSA	15	1.5
VDDC	245	24.5
VDD!	1400	140
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	155	15.5
Total chip GND current		179

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 288mV

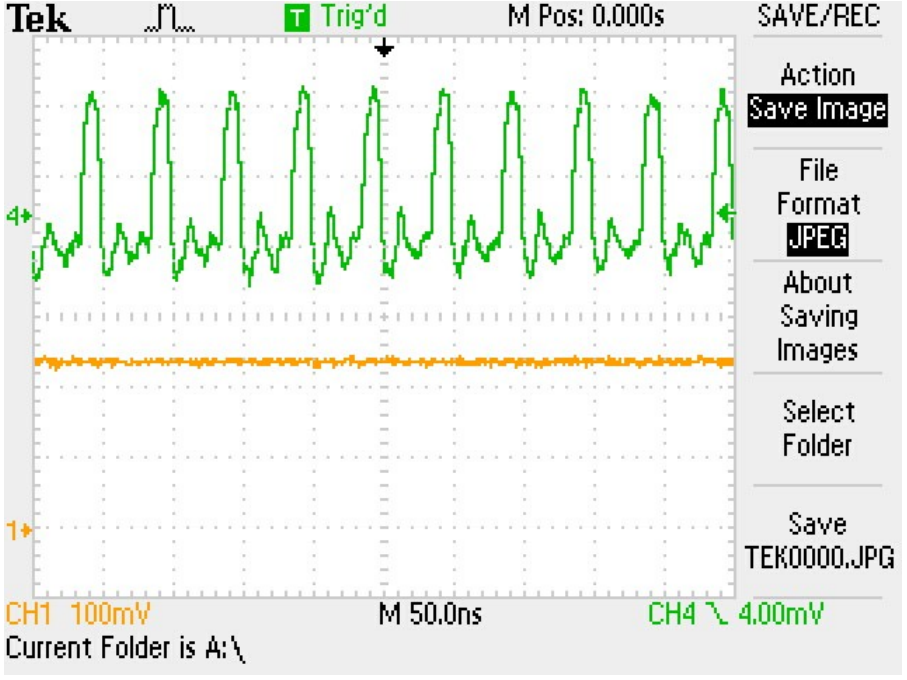
RD50-MPW3 – External clk 20MHz 50% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	127.5	12.75
VSSA	15	1.5
VDDC	242.5	24.25
VDD!	1485.0	148.5
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	155.0	15.5
Total chip GND current		187

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 211mV

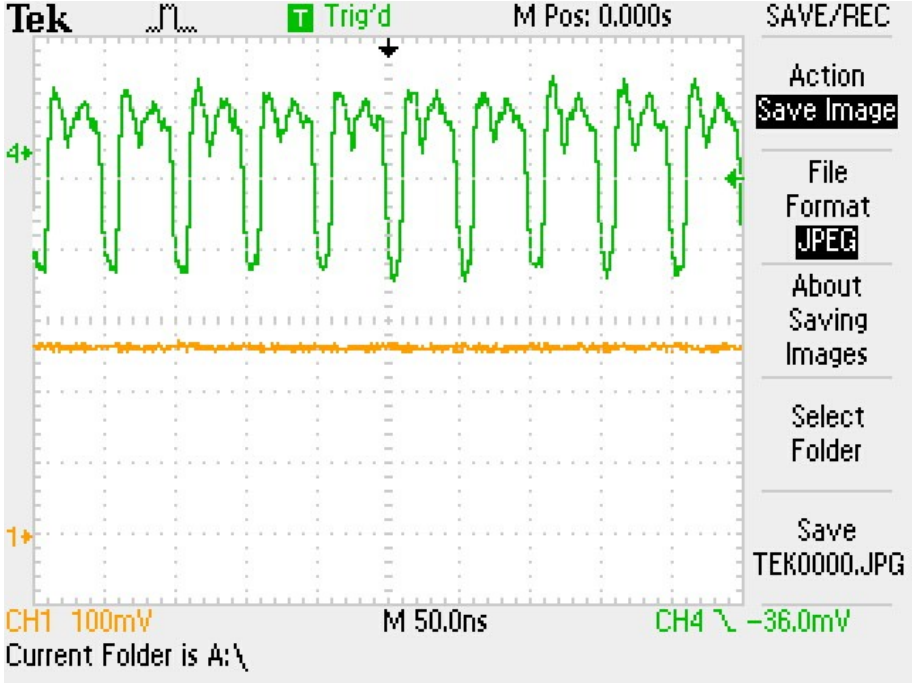
RD50-MPW3 – External clk 20MHz 25% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	127.5	12.75
VSSA	15	1.5
VDDC	242.5	24.25
VDD!	1492.5	149.25
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	155	15.5
Total chip GND current		187.75

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 240mV

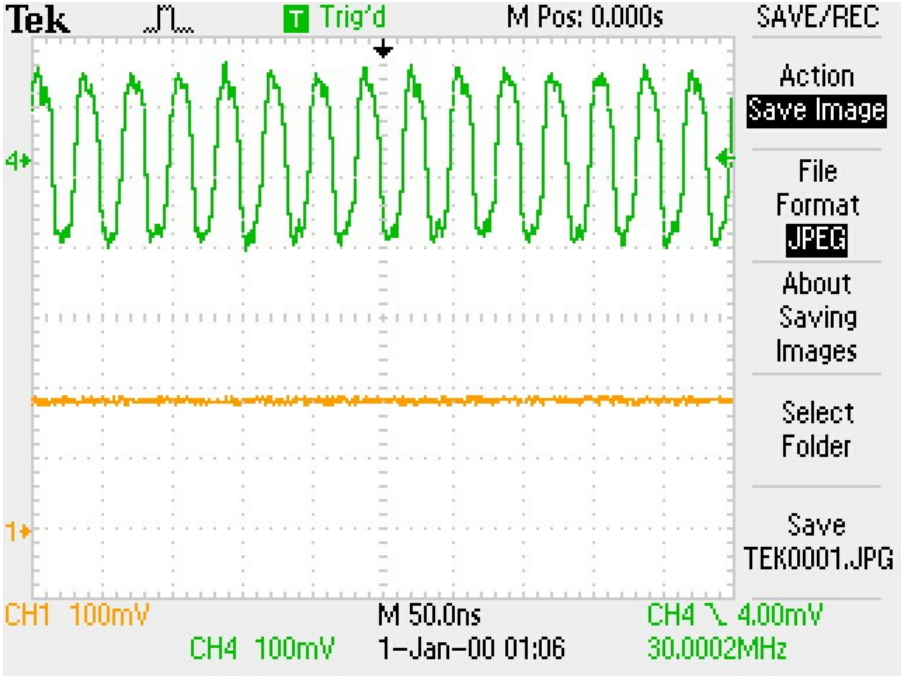
RD50-MPW3 – External clk 20MHz 75% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	127.5	12.75
VSSA	12.5	1.25
VDDC	247.5	24.75
VDD!	1485.0	148.5
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	155	15.5
Total chip GND current		187.25

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 271mV

RD50-MPW3 – External clk 30MHz 50% duty



Supply	Shunt voltage (uV)	Current (mA)
VDDA	75	7.5
VSSA	15	1.5
VDDC	230	23
VDD!	1627.5	162.75
Unused	N/A	N/A
1V8 NWELL RING	0	0
VSENSBIAS	0	0
2V5	157.5	15.75
Total chip GND current		194.75

- clk_40MHZ_p = green
- SFOUT = yellow
- DC offset of SFOUT ≈ 190mV

RD50-MPW3 – Summary of results

CLOCK FREQUENCY (MHz)	SFOUT OFFSET (mV)	DUTY CYCLE (%)	TOTAL CHIP CURRENT (mA)
2.5	139	50	153
10	355	50	169.25
15	288	50	179
20	240	25	187.75
20	211	50	187.0
20	271	75	187.25
30	190	50	194.75

- No effect on SFOUT offset or current by changing state of INI_TS_EXT signal