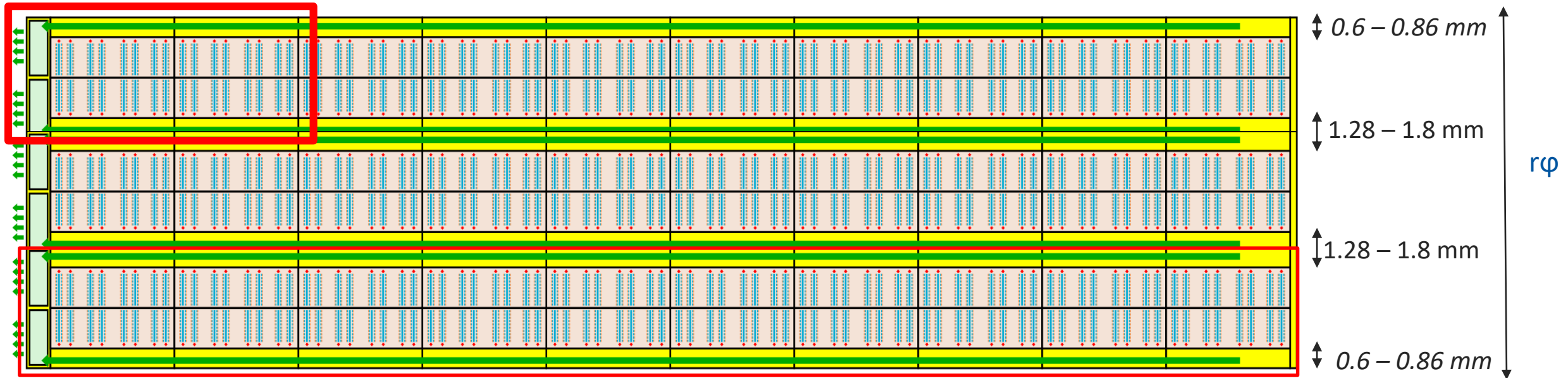


Layout Half Layer 0 Sensor

z
~27 cm



$R_0 * \pi = 56.5$ mm

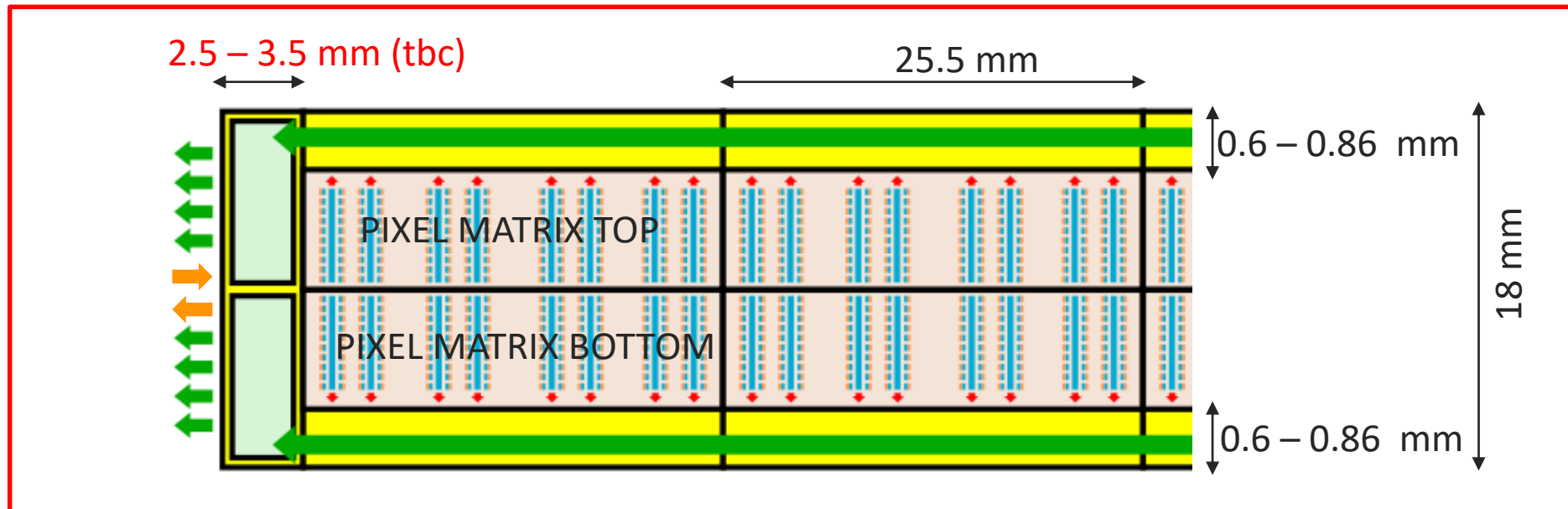
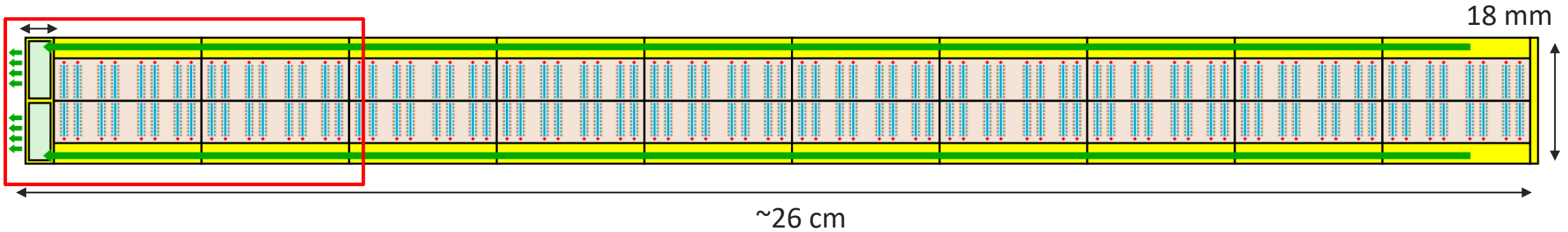


Sub-Module

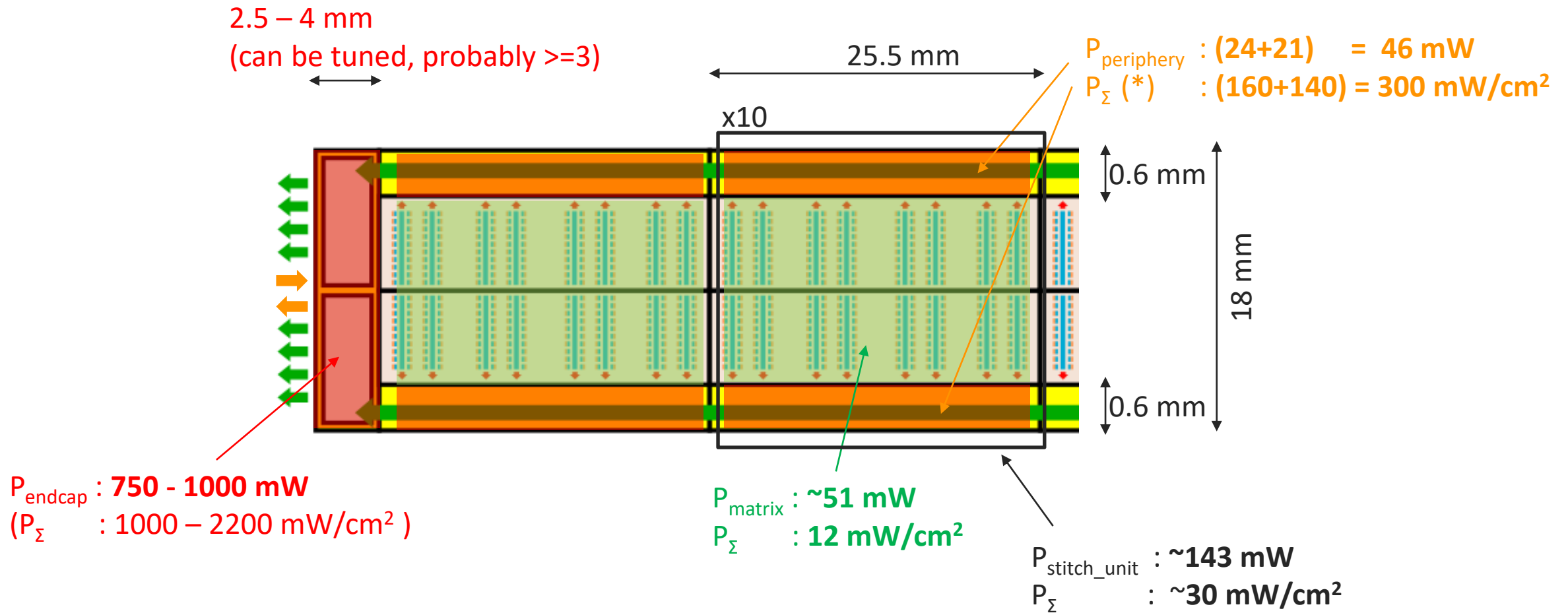
Non sensitive peripheral regions:
3.76 – 5.32 mm
6.7% – 9.5%

Dimensions and layout of one sub-module

Layer 0: 3 sub-modules. Layer 1: 4 sub-modules. Layer 2: 5 sub-modules



Power Densities Estimates



(*) The power dissipation density on the long peripheries will also have a dependence on the z-coordinate. Not included here

Notes



Estimates based on analysis, projections, estimates: best educated guesses.

Included additional dissipation due to on-chip linear regulators

The regulators are assigned on the long edge peripheries. The two values of power are the circuit dissipation and the loss in the pass transistors of the regulators

Did *not* include margin, in particular over the sensing area (matrix)

The power dissipation density will also have a dependence on the z-coordinate.

This is due to the IR drops on the rails and the addition of the on-chip linear regulation. A parabolic dependency with a minimum at $z=0$ is expected at first approximation. This spatial dependency is not shown, the resulting average value was added to the values shown.

The z-dimension of the endcap (short edge periphery) can be fine tuned

The determining value is the power for the endcap. Minimum width is 2.5 mm. Probably will require more width (3 mm or more), bringing possible reduction of power density.