Overview of ATLAS upgrade projects for HL-LHC

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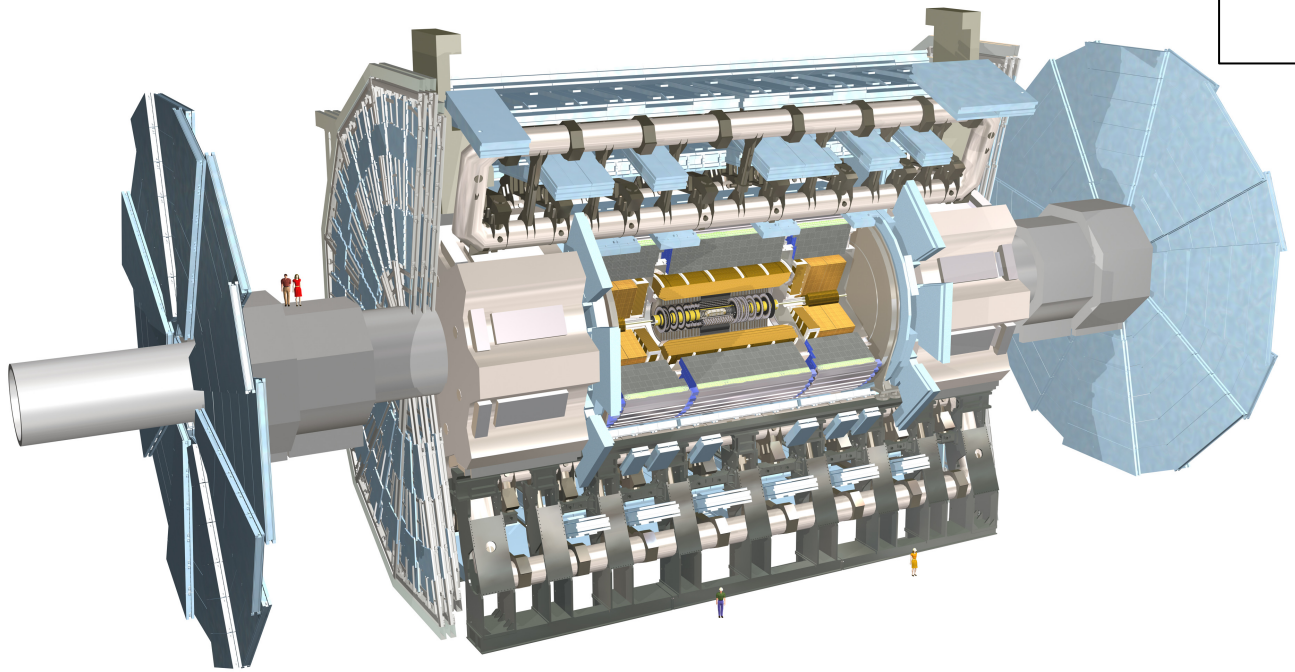
On behalf of the ATLAS collaboration

ATLAS upgrade overview



Forward detector

- Upgrade Luminosity Detector (LUCID) and Zero Degree Calorimeter (ZDC) to cope with the higher rate environment (detailed discussion in poster session)

Upgrade of Trigger and DAQ

- L0 trigger at 1 MHz with 10 μs latency, 10 kHz Event Filter output

Upgrade of Calorimeter

- Electronics upgrade for LAr and Tile calorimeters

New High Granularity Timing Detector (HGTD)

- Additional pileup suppression with timing information
- Forward region ($2.4 < |\eta| < 4.0$)
- Low-Gain Avalanche Detectors (LGAD) with 30ps time resolution
- Contributions to luminosity measurement

Upgrade of Muon system

- Additional trigger layers of RPC and replacement of MDT with sMDT in barrel inner station
- Additional TGC layers in endcap inner station
- Upgrade trigger/readout electronics

New Inner Tracking Detector (ITk)

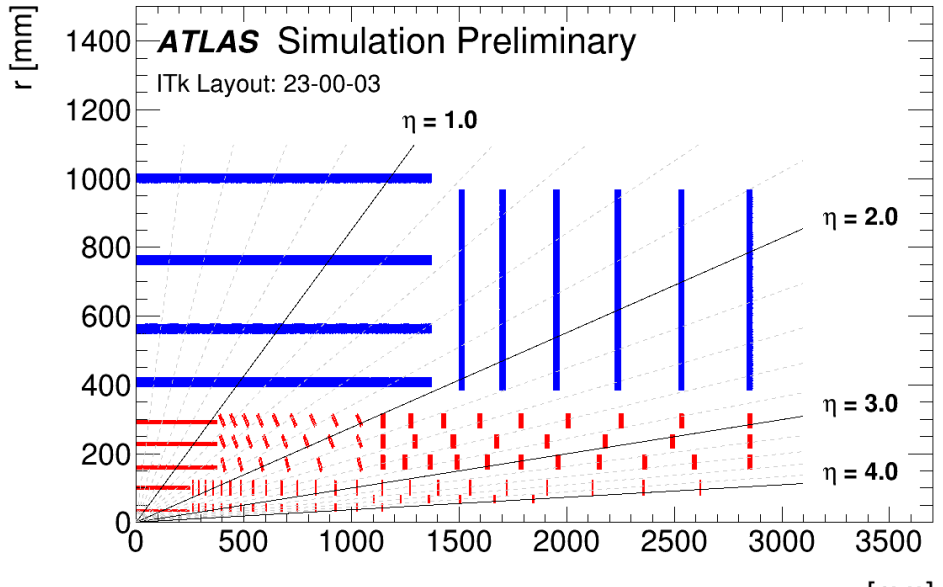
- Full silicon tracker covering up to eta = 4 with at least 9 layers on individual tracks
- Less material, finer segmentation

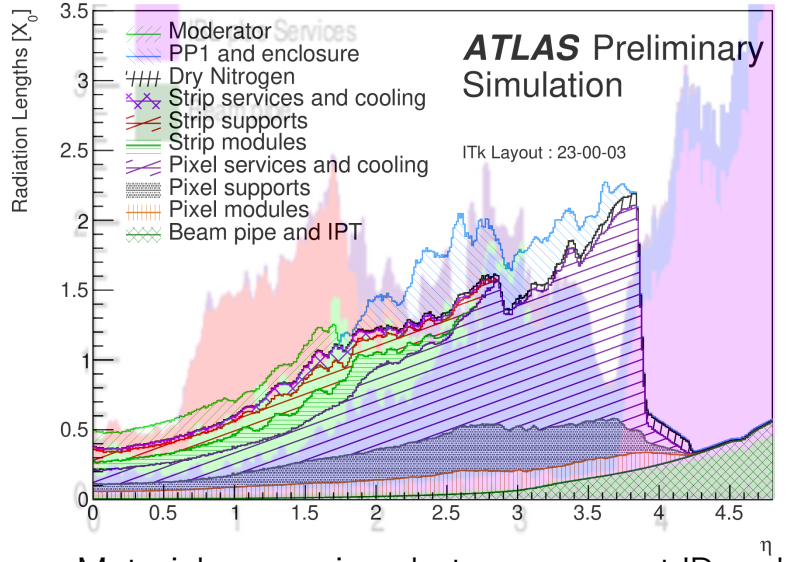
This talk reviews general features, and the latest status for the production and integration

Inner Tracker (ITk)

- **General features**
  - Complete replacement of the current Inner Detector with new silicon Pixel & Strip sensors
    - 13 m^2 of silicon in Pixels, 168 m^2 in Strips.
      - Note: Current ID 2.7m^2 pixel, 8.2m^2 strip
  - Larger angular coverage up to η =4, at least 9 silicon layers on individual tracjectories
  - Higher Radiation tolerant requirement up to 1 x 10^{16} n_{eq}/cm^2
  - Reduced materials

ATL-PHYS-PUB-2021-024
(Run3 detector paper plots)



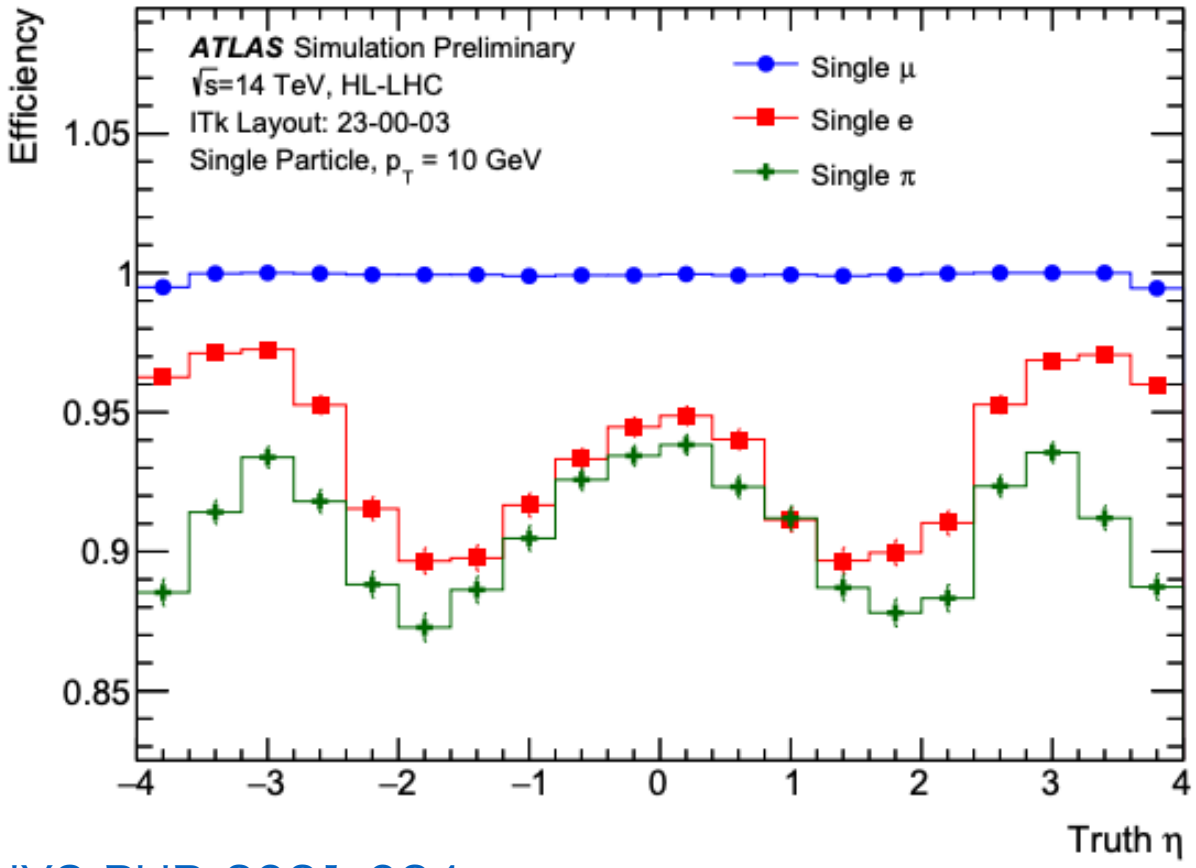


Material comparison between current ID and ITk

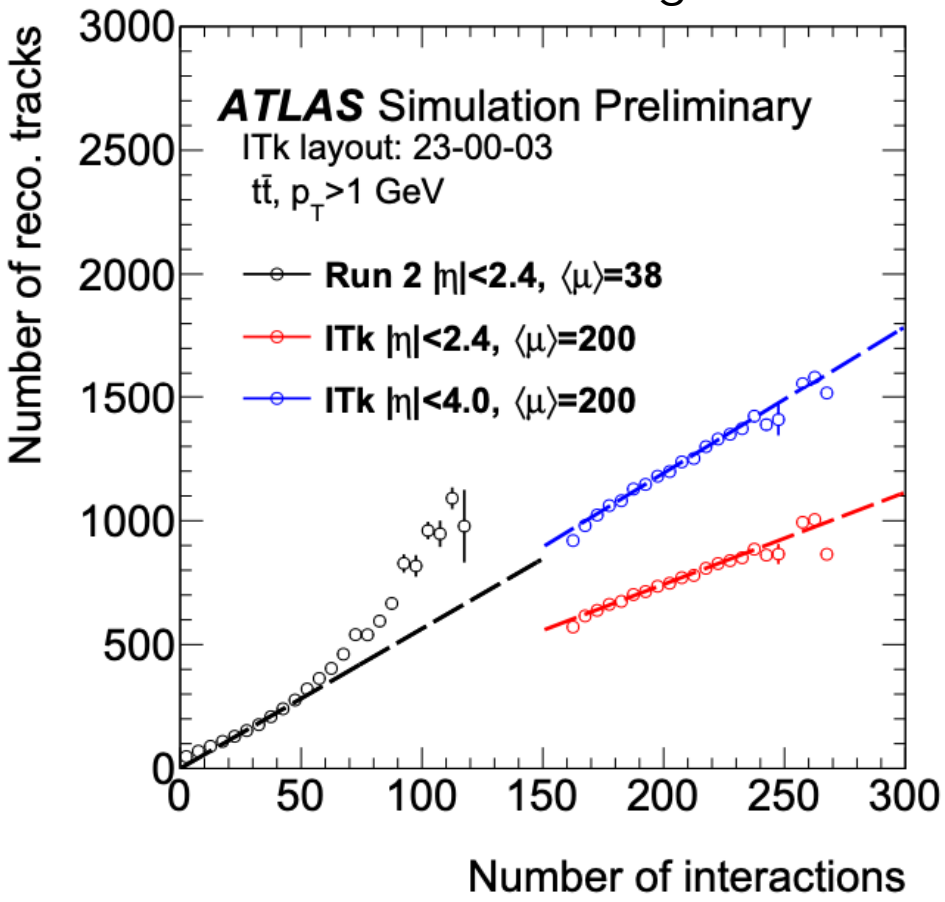
Inner Tracker (ITk)

- Tracking performance with the ITk

Good efficiency typically > 90%



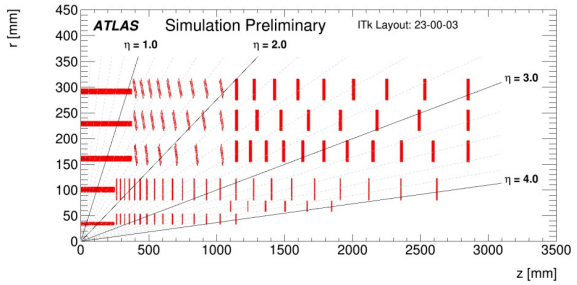
Good suppression of combinatorial backgrounds

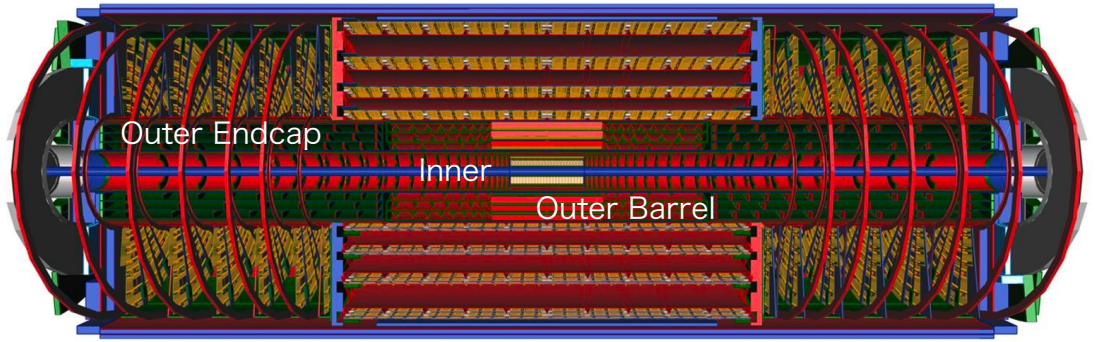


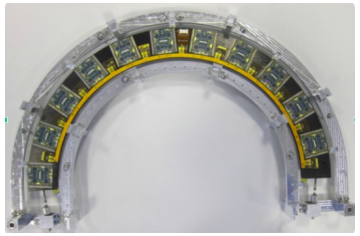
ATL-PHYS-PUB-2021-024

ITk pixel

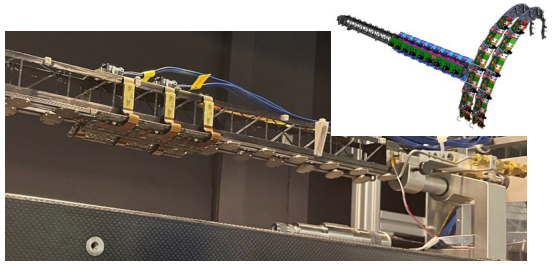
- **General features:**
  - Organized as three systems (inner, outer, outer endcaps).
  - Features of sensors:
    - Different pixel sizes for layers
      - 25 x 100 μm^2 (innermost barrel)
      - 50 x 50 μm^2 (everywhere else).
    - 3D sensors in innermost barrel/disks and planar sensors in the other layers.
    - In total, more than 1.4 x 10^9 channels.
  - Inner system replaceable for radiation damage
- **Production status:**
  - Pre-production of sensors (3D/planar) have been complete
  - Production of FE ASIC is begin started
  - Hybridization is in progress along with thermal tests



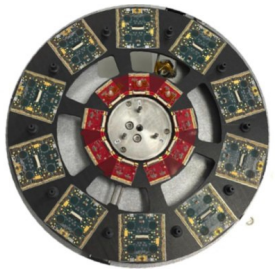




Outer endcap half ring prototype

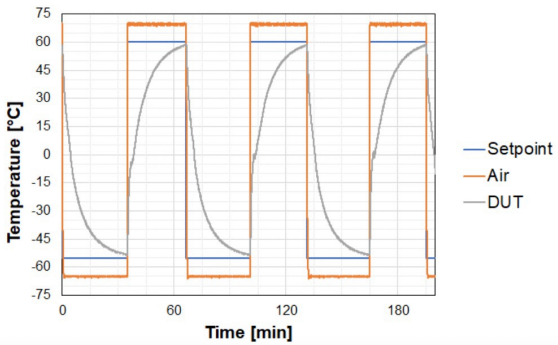


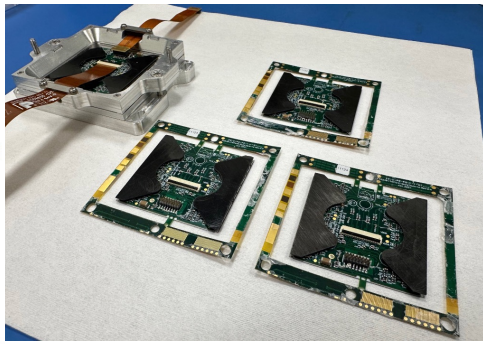
Outer barrel demonstrator @ CERN



Loaded inner ring prototype

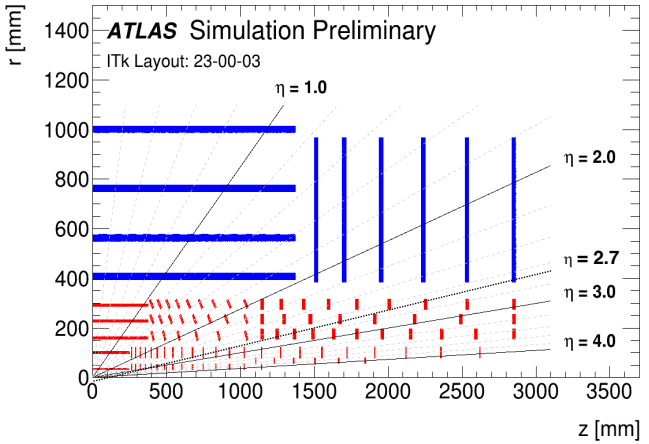
Module thermal tests @ CERN

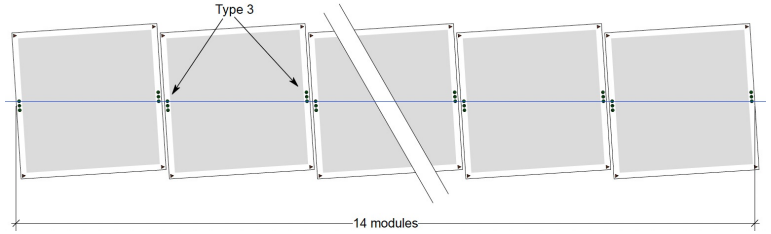




ITk strip

- **General features:**
  - 4-layer barrel and two 6-layer endcaps disks
  - Angular coverage of $|\eta| < 2.7$ with 18,000 modules.
  - Strip width ~75 μm.
  - 60 x 10^6 channels
- **Production status:**
  - First staves/petals are loaded
  - ASIC testing is almost complete
  - Sensor production in progress as planed
  - Extensive studies involving thermal cycling of the modules on-going
  - Construction of large-scale structure in progress
    - Outer cylinder arrived at CERN
    - L3 cylinder at CERN, L2 expected to be at CERN this month
    - Installation of L3 and L2 cylinders into outer cylinder will start in July

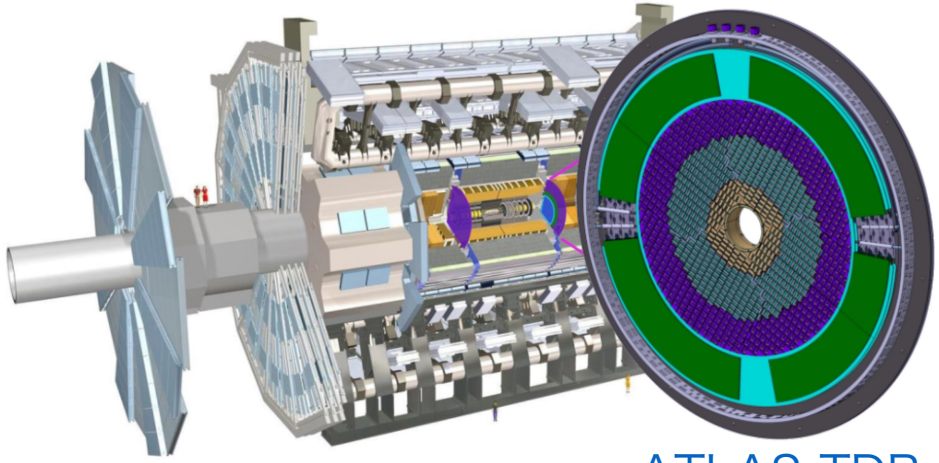




Module-loaded staves

High Granularity Timing Detector (HGTD)

- **General feature**
  - Completely new detector to be inserted between ITk and endcap calorimeter
    - Mitigate pile-up with hit-timing information
    - Especially in the high eta region where the vertex position separation is limited
    - $2.4<|\eta|<4.0$, $12<R<64$cm.
  - Four layers of LGAD modules to achieve a good timing resolution
    - 70 ps per hit and 30-50 ps per track
  - Pixel size of LGAD is 1.3 x 1.3 mm^2



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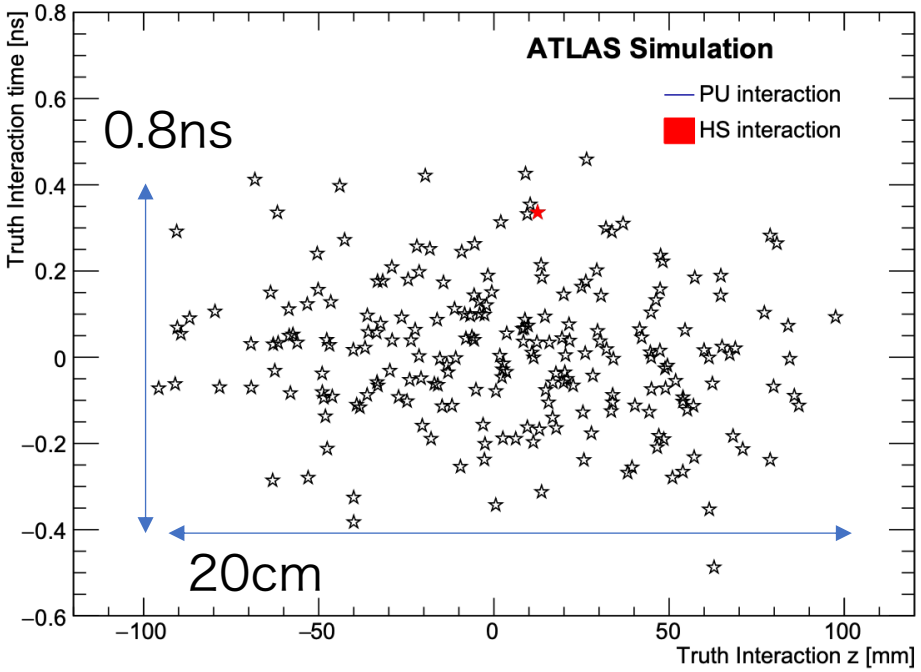
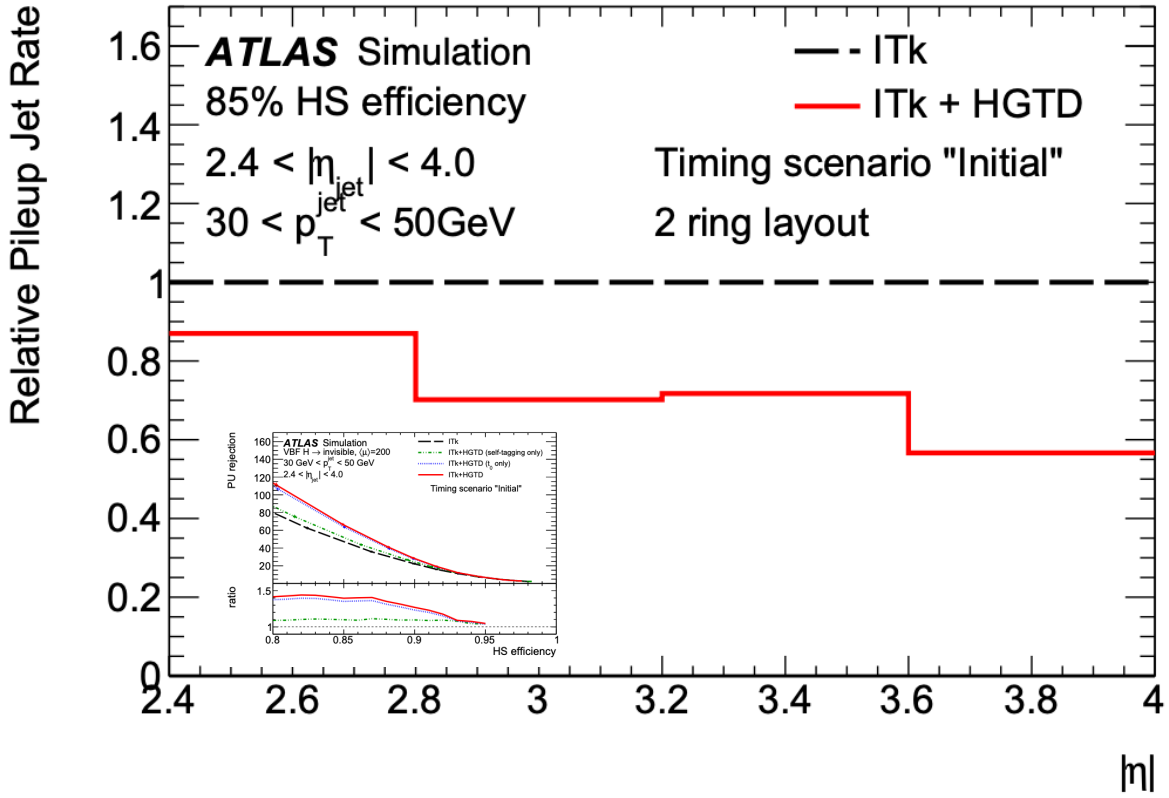
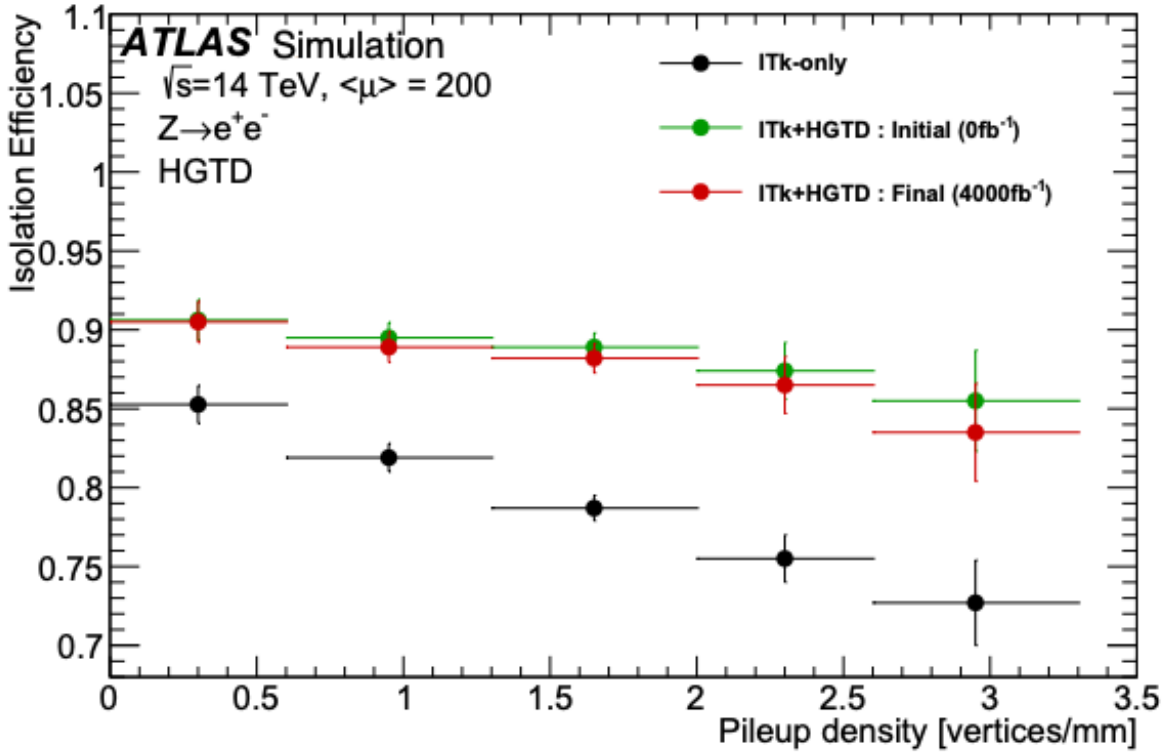


HGTD

- **Pileup rejection performance with HGTD**
  - Additional rejection of pileup jets with timing information
  - Improved track-based isolation, removing PU track contribution



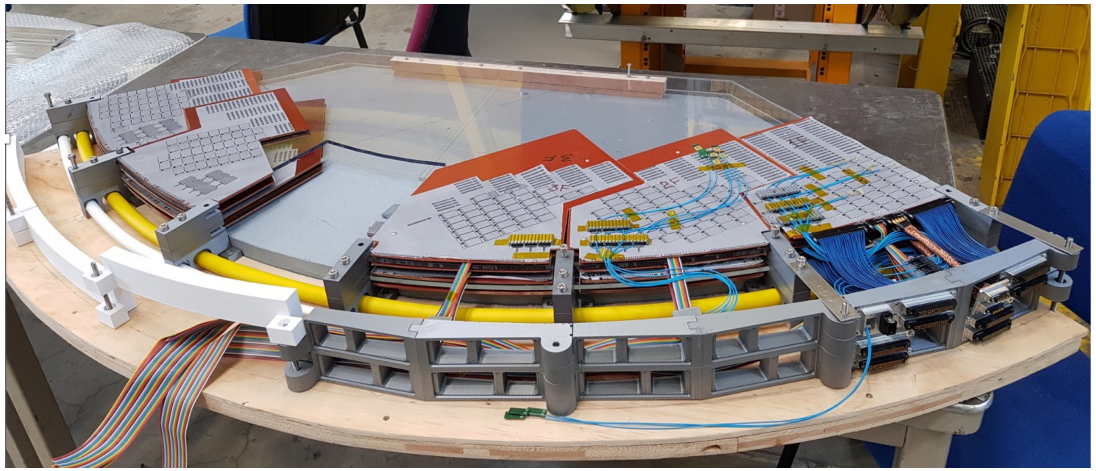


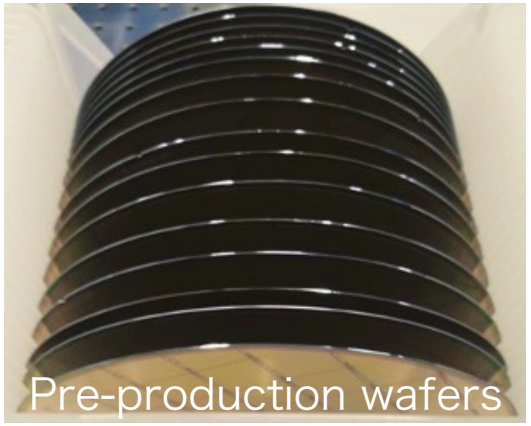
ATLAS-TDR-031

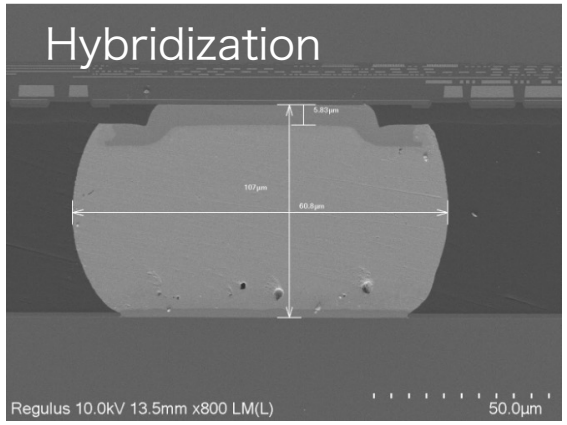
HGTD

- **Project status**
  - ASIC preproduction (ALTIROC-A) have been launched after extensive testing of prototype (ALTIROC3) in lab and test beam
  - Tests of hybridization with pre-production LGAD sensors and prototype ASIC shows good performance
  - First prototype of the Peripheral Electronics Board (PEB) being tested in assembled demonstrator
  - Careful assessment of assembly with mock-up

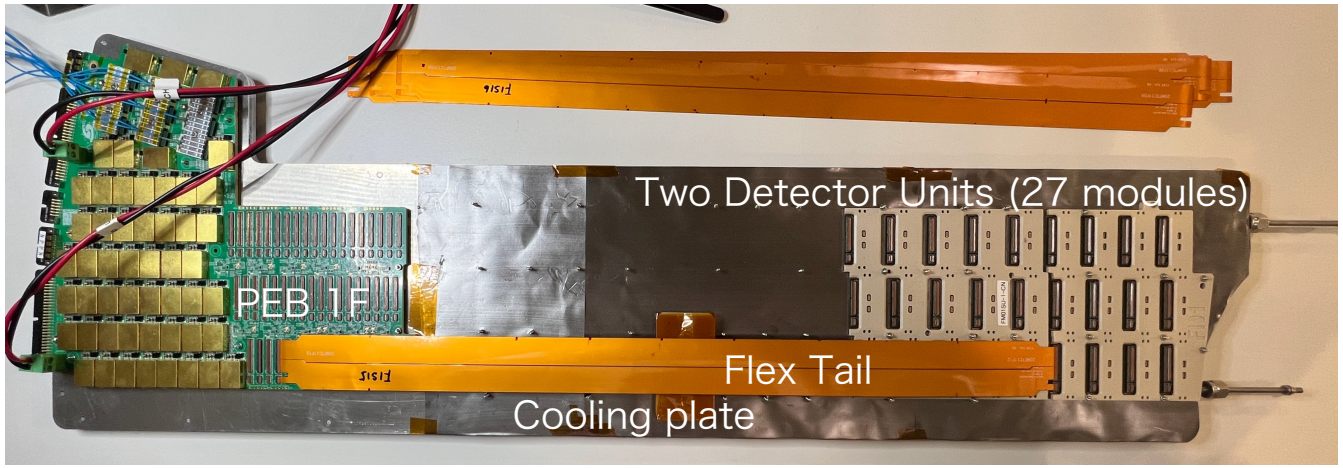
Mock-up to assess assembly





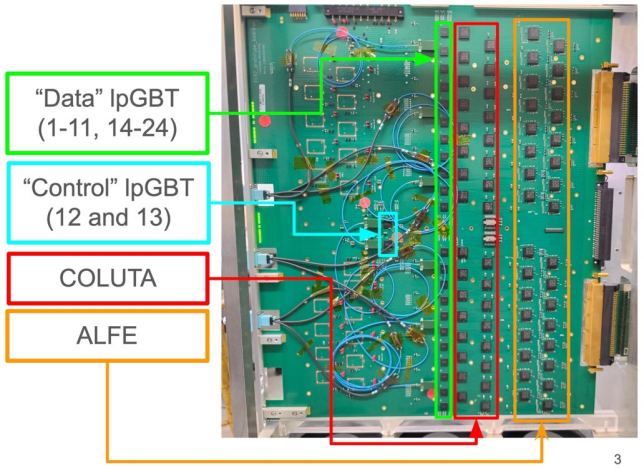


PEB and demonstrator



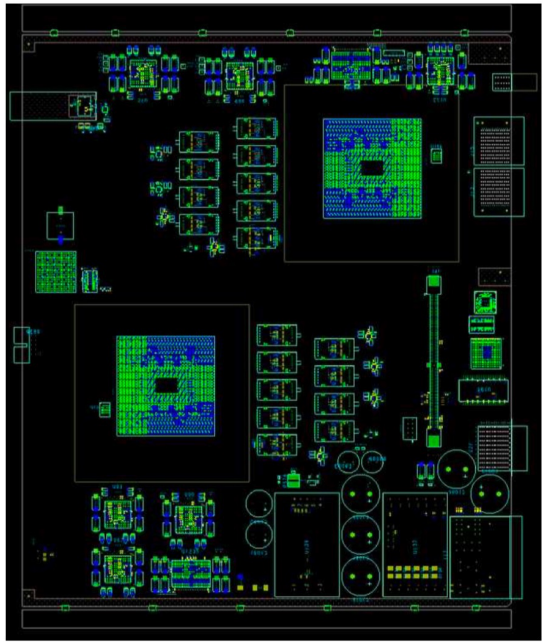
Calorimeter

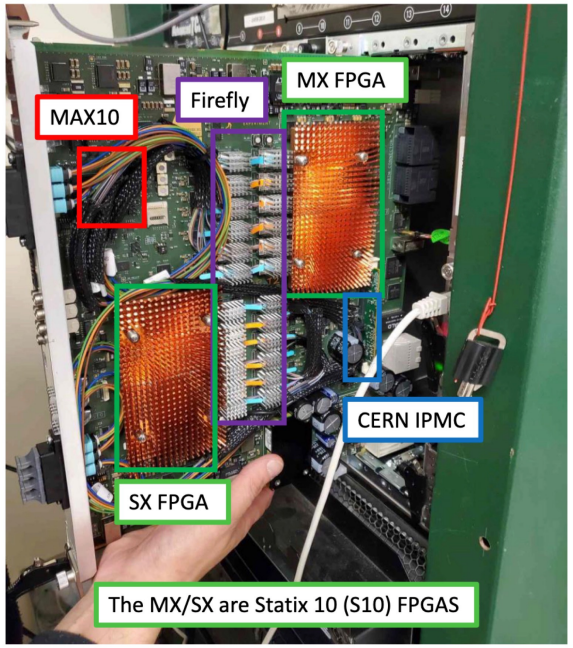
- **Liquid Argon Calorimeter (LAr)**
  - Upgrade both on- and off-detector electronics
    - Continuous readout at 40 MHz.
    - Total bandwidth of 345 Tbps.
    - New high precision frontend electronics
      - 16-bit dynamic range with nonlinearity < 0.1 % up to 300 GeV
      - Electronics noise < MIP energy
    - 128-ch Front End Board (FEB2)
    - ATCA blade for waveform feature extraction (LAr Signal Processor)
      - Hosts ~33k links at 10 Gbps
  - Status
    - Custom LAr-specific ASICs in production
    - FEB2v2 prototype fabricated and assemble
    - Off Detector prototype boards becoming available



FEB2v2

LASP-TEST board at EMF

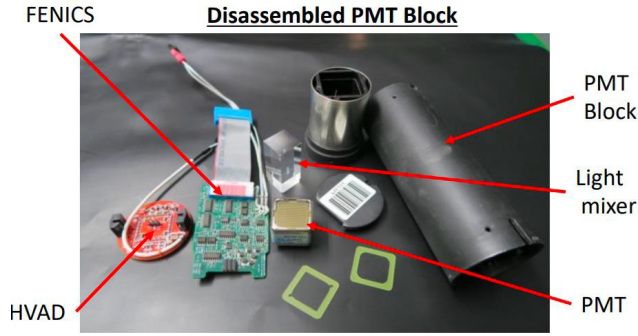


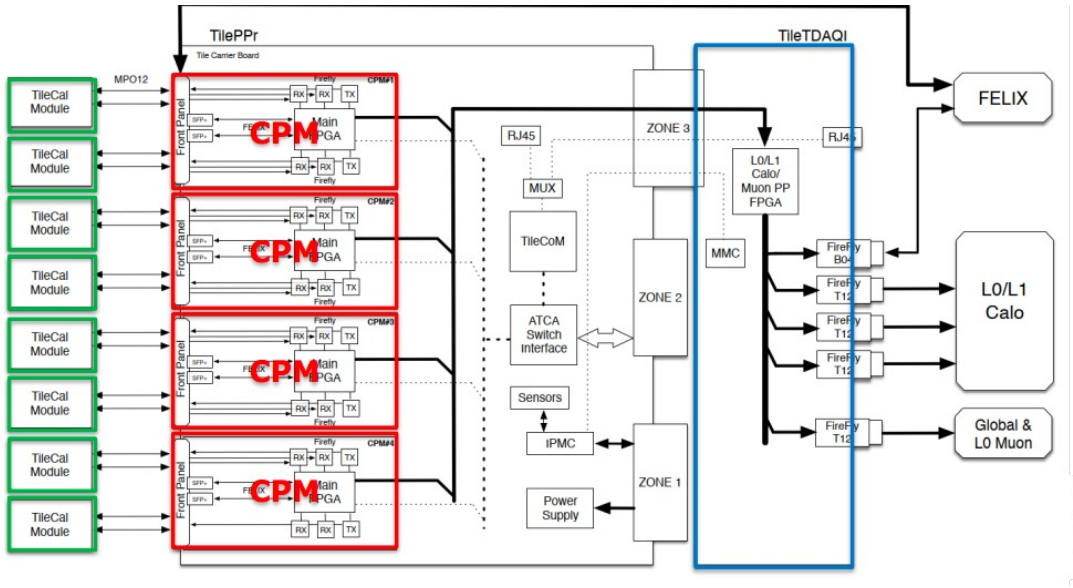


Calorimeter

- **Tile Calorimeter:**
  - Replacement of all electronics to fulfill the Phase-2 readout and trigger specification
    - Digital trigger with improved precision and full radial granularity
    - Higher data bandwidth with 40 MHz readout
  - Reassemble and upgrade PMT blocks
    - Active HV divider
    - Replacement of the most exposed PMTs (about 10%).
  - New frontend mainboard
  - New TileCal PreProcessor (PPr) ATCA blade (CPM, Carrier, RTM) is being developed
  - Status
    - Frontend mainboards have arrived at CERN,
    - Phase-2 demonstrator installed in ATLAS and is taking data
    - Off detector electronics are on the Final Design stage

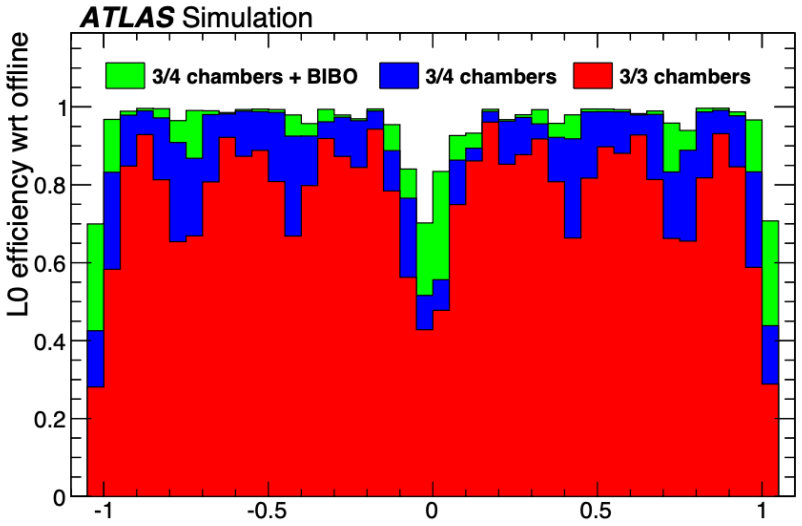
PMT Block



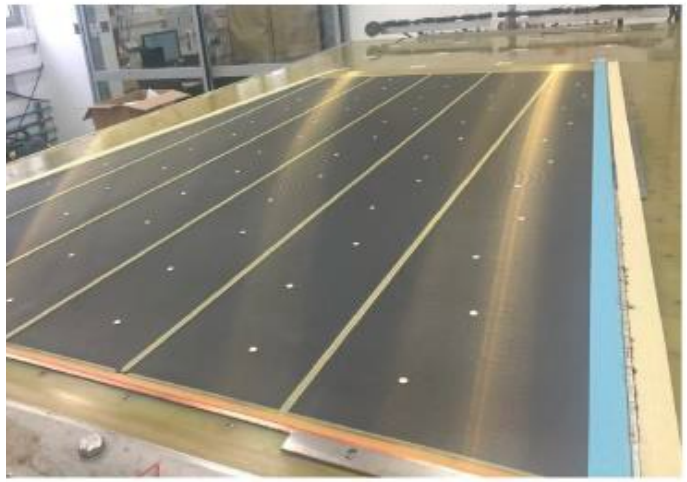


Muon

- **General features**
  - Replacement of electronics
  - Barrel Inner station upgrade
    - New triplet RPC layers
    - sMDT in small sectors
  - EI TGC upgrade
    - Replacing doublet TGC with triplet TGC
- **Project status**
  - sMDT production complete
  - Many of electronics components are in production phase
  - Activities at cavern are being extended
    - First new EI TGC sectors to be installed in YETS 24-25 to sort out potential problems
    - "Dry run campaign" of electronics instllation
    - Demonstrator of electronics installed in P1

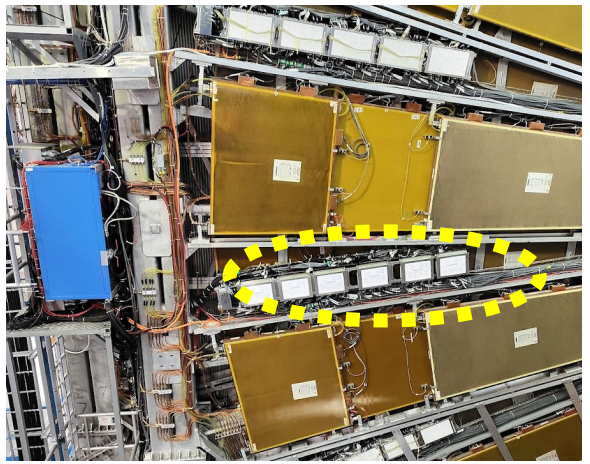


RPC trigger improvement



TGC chamber production

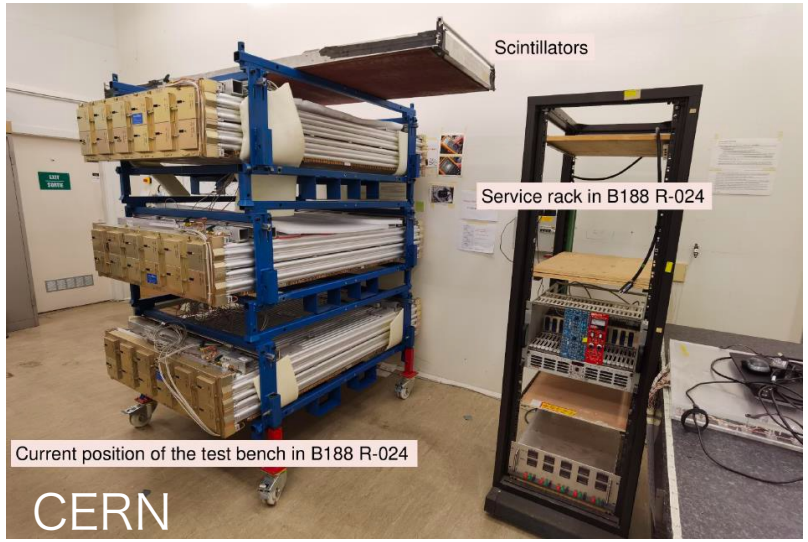
Mockup installation

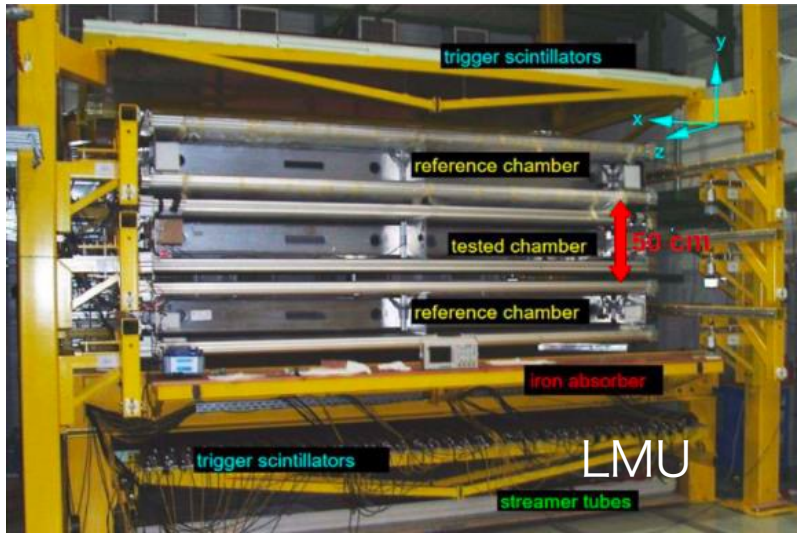


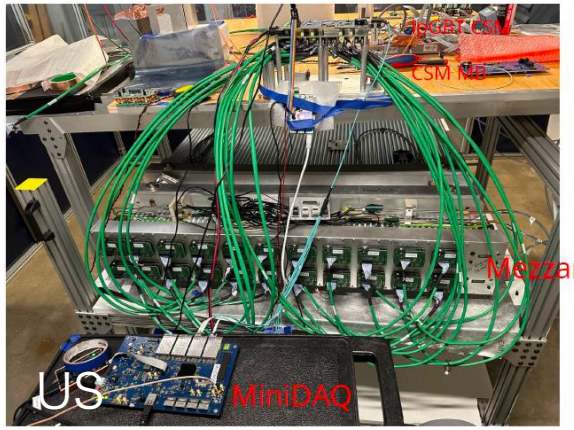
Demonstrator in cavern

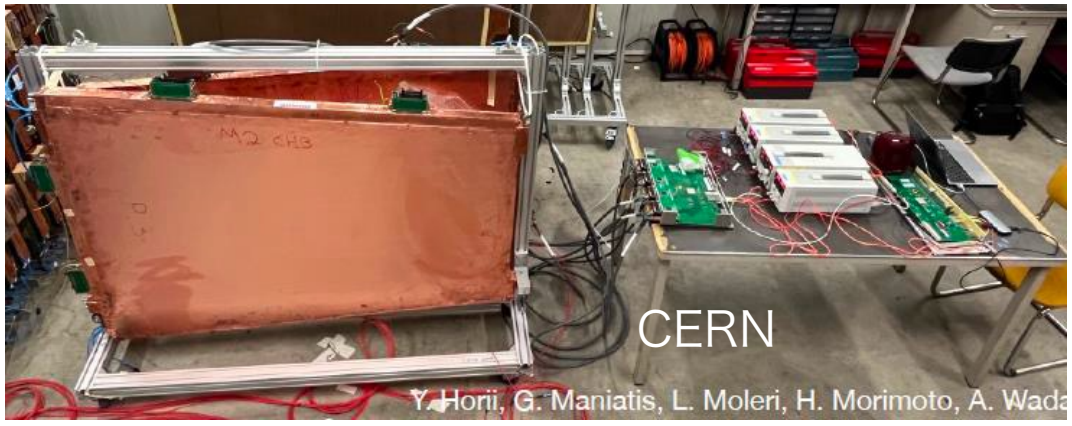
Muon

- Testing and integration at test facilities



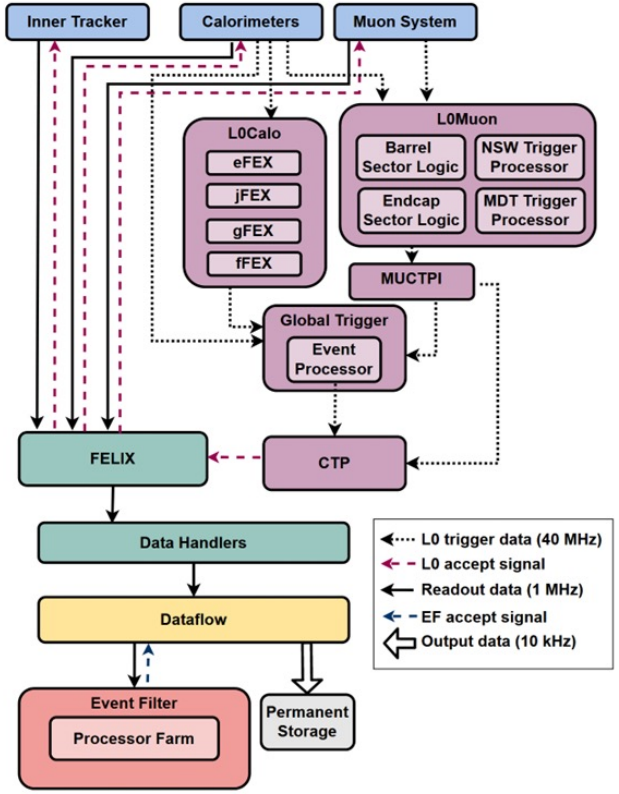




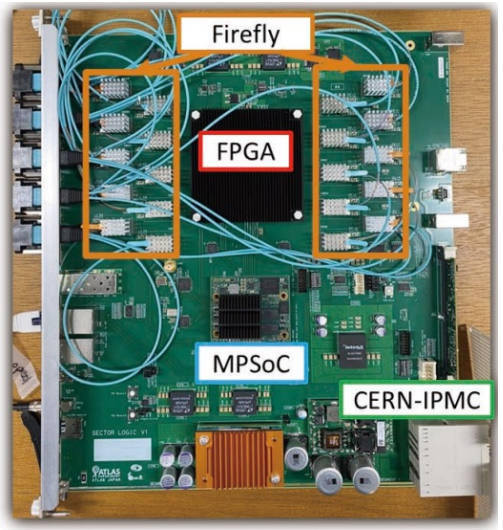


Trigger DAQ

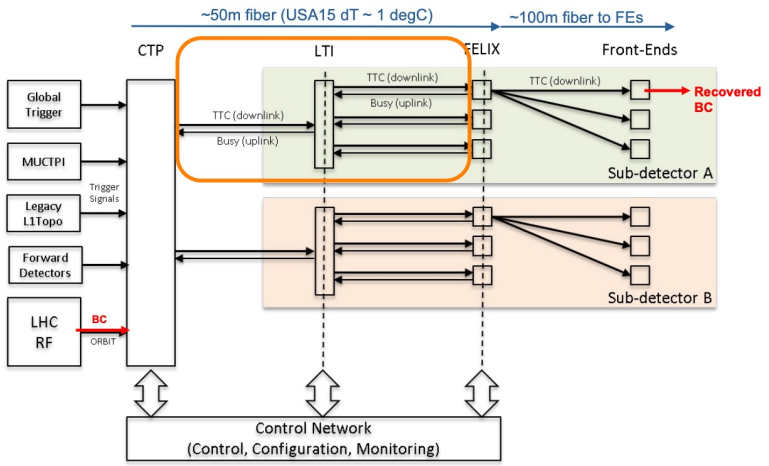
- **Phase II TDAQ specifications**
  - L0A rate 1 MHz with 10us latency
  - EF output rate 10 kHz
  - Estimated event size of 4.6 MB

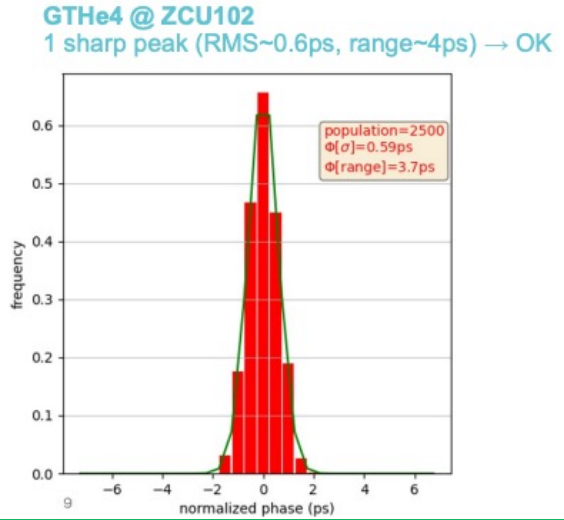


- **L0 Trigger**
  - Prototyping and testing
  - Integration tests are ramping up:
    - Communication tests between subsystems are being conducted
    - Demonstration of functionalities in system-level tests



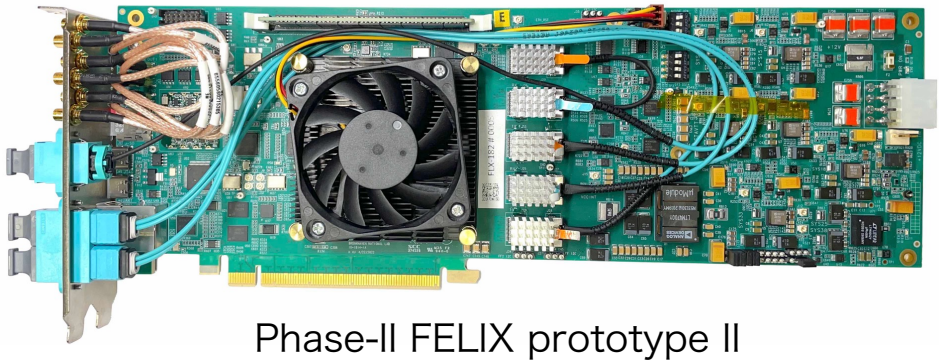
Example of system-level demonstration
Phase-2 TTC distribution tests to check phase reproducibility



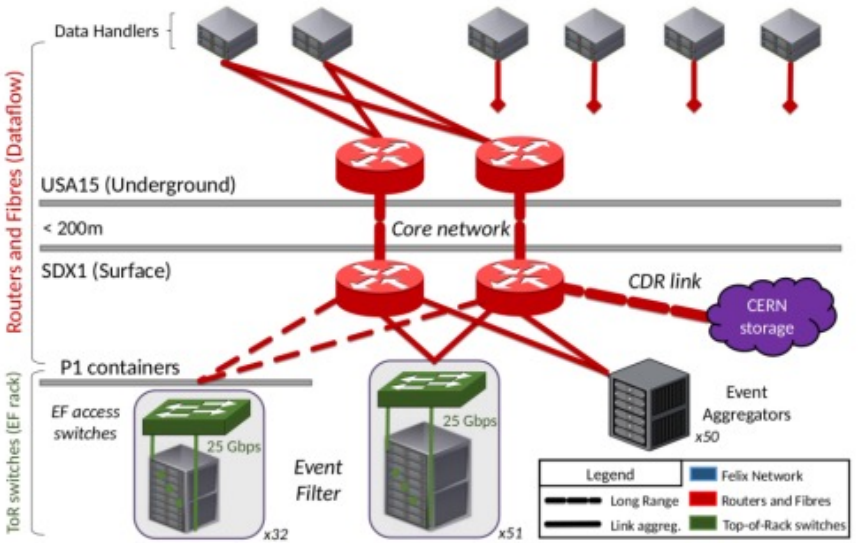


Trigger DAQ

- **Data Acquisition**
  - Phase 2 system is designed as high-speed DAQ with high throughput network
    - The prototyping for high throughput network is in progress
  - FELIX prototype testing is on going
  - Test campaigns at P1 was conducted in the last YETS
    - Specifically for dataflow part and online software components
    - Performance close to requirements



Phase-II FELIX prototype II



- **Event Filter**
  - Demonstrators mostly progressing well and on track
  - Very good progress on GPU and FPGA support in ATLAS software (Athena)
  - Final demonstrator phase later this year for EF track, that will provide input for the hardware technology choice in 2025

Conclusion

- **To cope with the demanding conditions of HL-LHC, ATLAS will undergo a major upgrade in the next long shutdown LS3 starting 2025 right after Run3 ends**
  - New detector components:
    - **ITk**, a new all-silicon tracker with an improved coverage up to $|\eta|<4$.
    - **HGTD**, an LGAD based timing detector for pileup mitigation with additional precise timing information
    - **New muon chambers** of sMDT, TGC, RPC
  - Electronics upgrades:
    - **LAr and Tile calorimeters and muon systems** upgrading cope with HL-LHC trigger and readout specification **with extended bandwidth and enhanced computing power**
  - TDAQ upgrades:
    - L0 trigger system upgrade at 1 MHz L0 rate and
    - High throughput networking using the cutting edge electronics and computing architectures.
- **Phase-II upgrade activities continually progress into production**
- **The phase of testing, integration, and planning for the installation is starting**
- **Significant effort for software in both online EF and offline reconstruction**
  - Covered in “Software upgrades for HL-LHC”