3rd CERN System-on-Chip Workshop

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Workshop – Summary

3rd CERN Workshop on System on Chip, follow-up from the 2nd WS held in June 2021 using zoom only

Across CERN experiments, ATS, RCS and Radiation Protection

- **146** registrations
- Hybrid workshop at CERN and via ZOOM
- **8** vendors presentations
- **19** presentations from different uses of SoC :

  CERN Experiments, Equipement Groups (**ATS**) and Radiation Protection (**HSE**)

- **3** Tutorials and demos
- **7** System oriented presentations

Workshop – Vendors Exhibition

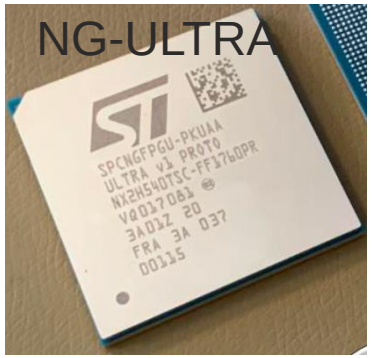
Hardware demonstrations

6 Booths (AVNET-SILICA, Microchip, NanoXplore, Enclustra, Trenz, TOPIC)

Exhibition took place in 500/1-201 "Mezzanine"!

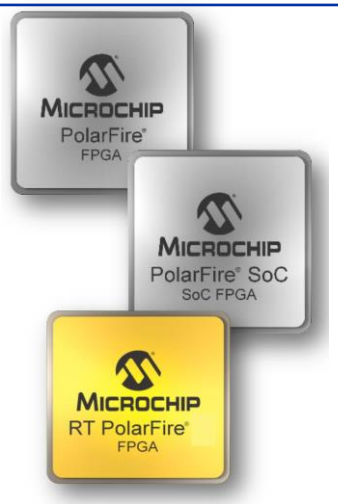
Workshop – Vendors Presentations

NanoXplore | AMD XILINX | MICROCHIP | ENCLUSTRA FPGA SOLUTIONS | NVIDIA | TOPIC EMBEDDED SYSTEMS | trenz electronic GmbH



- ST 28nm FD-SoI
- Fully European supply chain
- SEU immune (heavy ions) up to 62Mev.cm^2

- Versal family is growing
- New Kria module
- Zynq EOL up to 2035



- PolarFire SoC
- RISC V (Open source ISA)
- High REL and RAD-TOL options
- Less power hungry than SRAM based SoC

- DPU (Data Processing Unit)

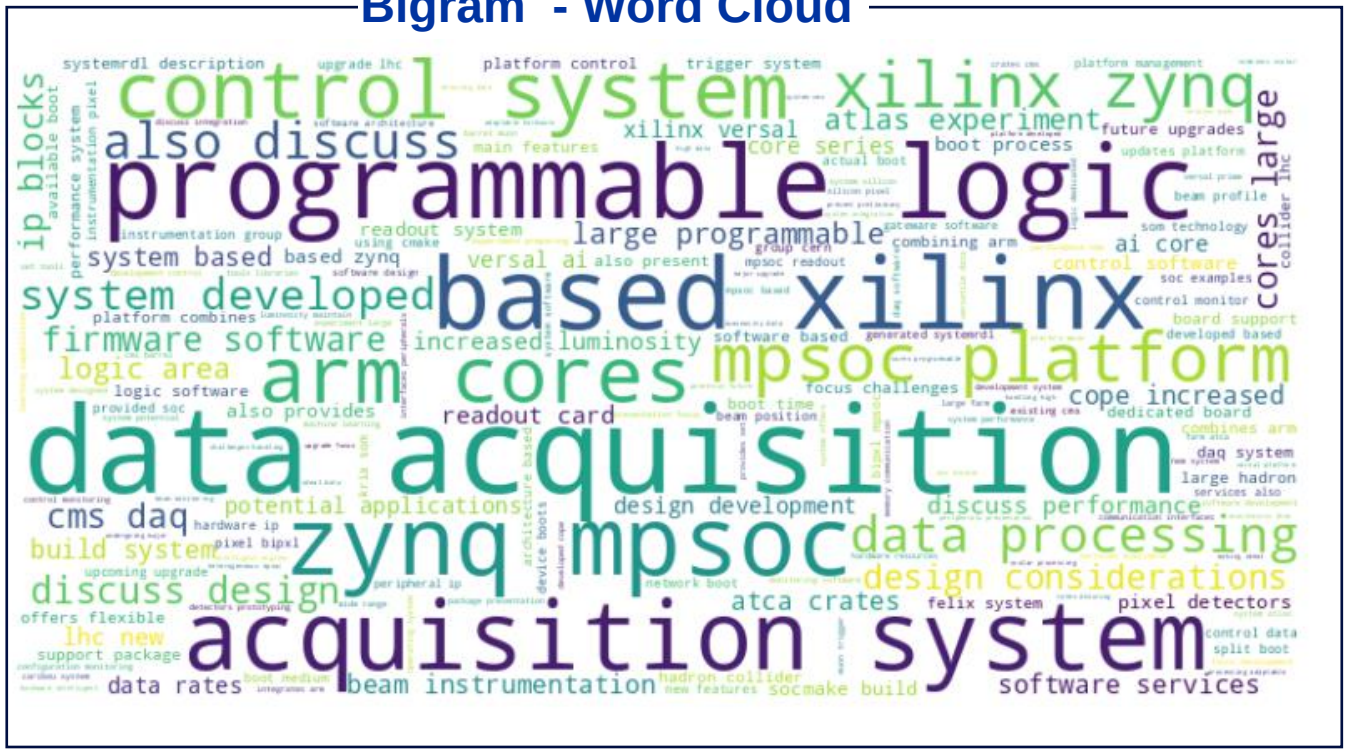
- Various SoMs from AVNET, TOPIC, Enclustra and TRENZ

Workshop – Projects Presentations

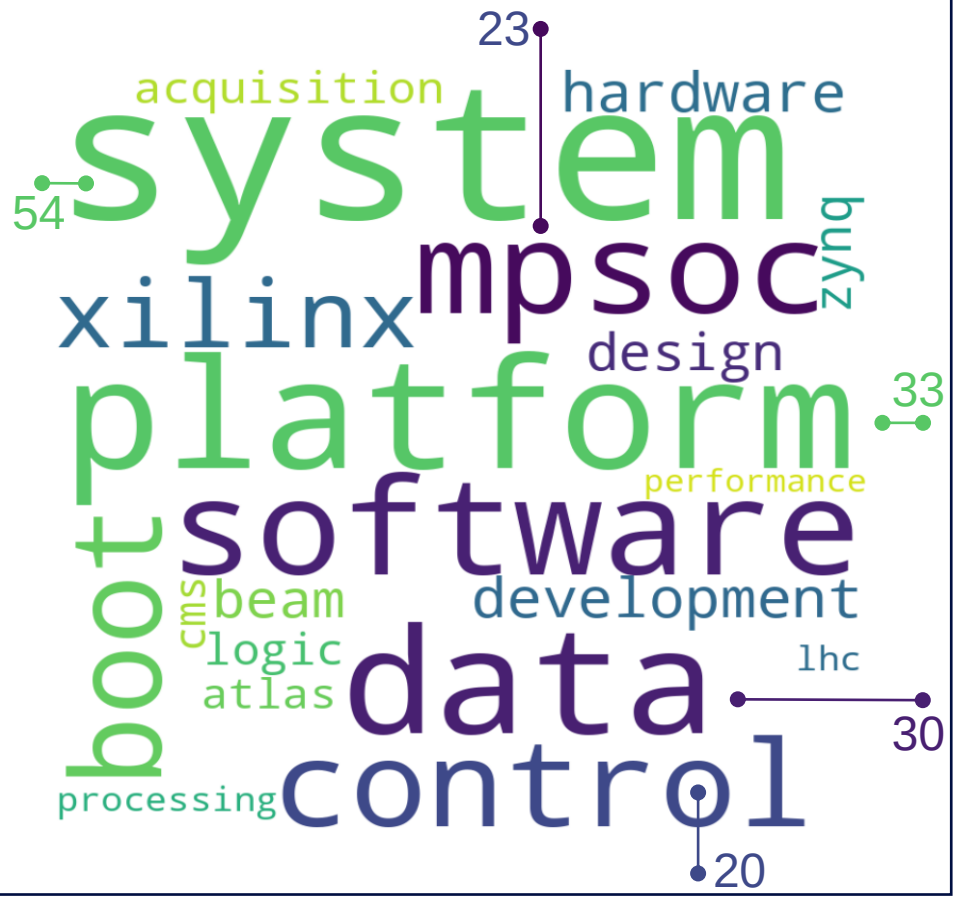
19 presentations from different uses of SoC :

CERN Experiments, Equipment Groups (ATS) and Radiation Protection

Bigram - Word Cloud



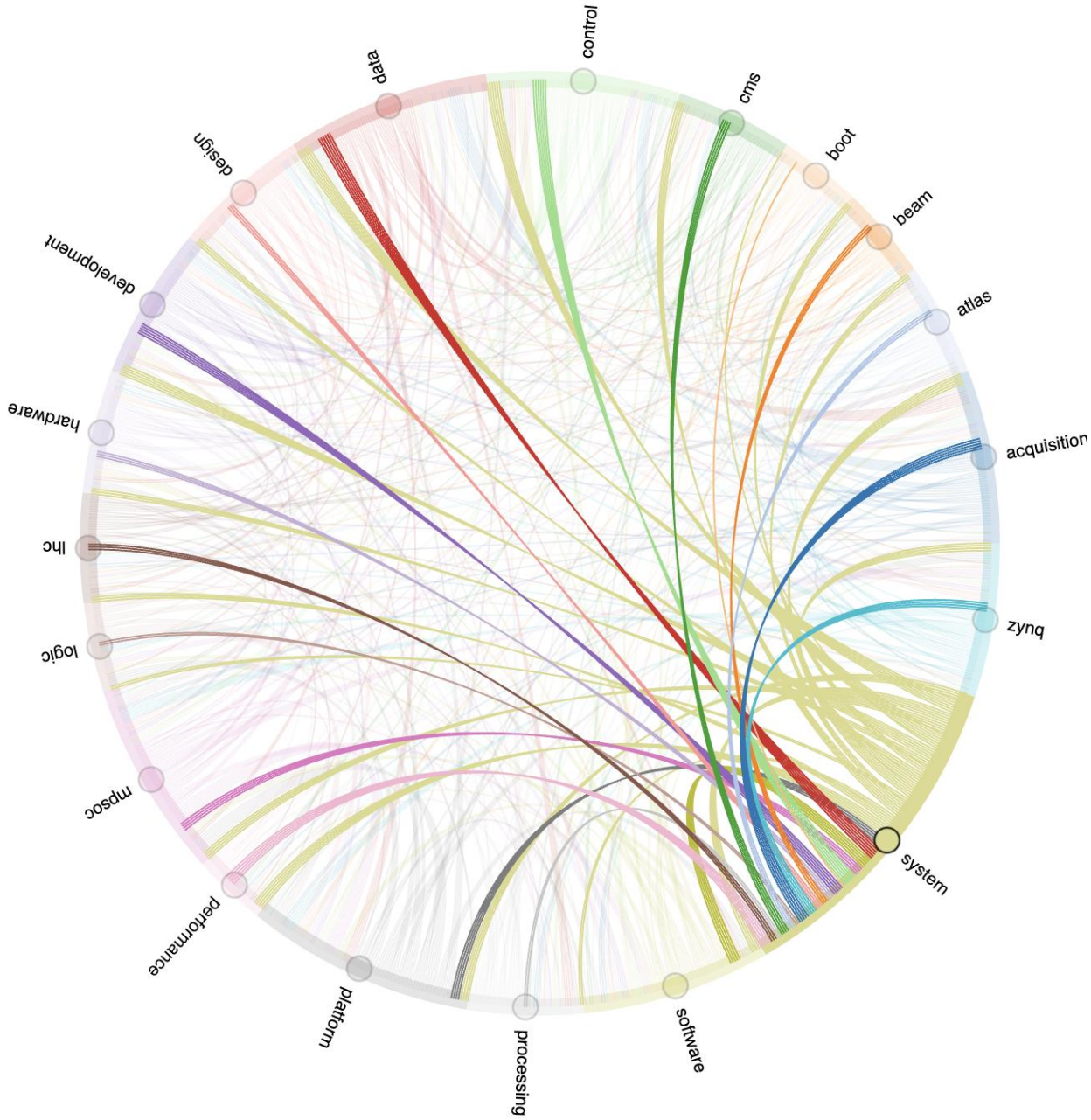
Keywords - Word Cloud



Workshop – Projects Presentations

Quick analysis

- SoCs are always integrated into a more complex system
- An increase of SoC/SoM usage
- Across all sectors and experiments
- Although we do not have a precise number, we estimate for LHC Phase-2 (Run 4, 2029-2033): between 2300 and 3600



Workshop – Projects Presentations

Quick analysis

The 19 presentations cover all the topics identified in the survey of May 2022 (summary report: CERN-OPEN-2023-001**,** **http://cds.cern.ch/record/2847967**) :

1. Hardware platforms and integration
2. Beam Instrumentation and monitoring
3. Data acquisition and processing
4. Monitoring and platform management
5. Software development and SoC tailored tools
6. Real time processing and control
7. Networking and communication

Workshop – Projects Presentations

Since the last SoC Workshop (June 2021)

- **Very mature projects with different strategies**

- For ATS
  - **DIOT expect to deploy 500** platforms for LS3. The system board of the DIOT is using Zynq US+ without SOM. The SoC is not running Petalinux neither Yocto → Xilinx GIT repos + Debian to build their images. The boot process was aligned with the FECs boot process and uses GRUB
  - **FGC4 Power Converter Controller** : Usage of asymmetric processing (2 core CPU of the A53 CPU running Linux and 2 cores for bare metal) to achieve real-time regulation constraints
  - **Beam Instrumentation Pixel (BIPXL)** used for the measurement of the beam profile. 2 operational BGIs at the PS and planned to be installed at the SPS during YETS 2023. Their SoCs are running petalinux (APU) and FreeRTOS (RPU).
  - **HL-LHC Beam Position Monitor** is using an RFSoC to exploit the very good performances of the embedded ADCs and potentially reduce the costs of their development.
  - Most probably will use FESA to interface SoCs with FECs (Under approval of ATS CTTB)

Workshop – Projects Presentations

Since the last SoC Workshop (June 2021)

- ATLAS :
  - **Embedded Monitoring Processor** (EMP), a common electronics platform for detector controls, exploiting SoCs (Trenz SoM in v1) to interface on-detector lpGBT links to the experiment's controls network via dedicated quasar servers. The SoC is running Petalinux + CS8 rootfs (Alma 9 in progress)
  - **gFEX or The Global Feature Extractor**, is part of the ATLAS hardware trigger getting input signal from the calorimeters. Zynq US+ MPSoC is used for monitoring and control. Yocto based OS (from open source release to yocto-manifest) and Considering moving to the Petalinux system to inherit a common approach and support
  - For the Phase-2 upgrade, a new **Central Trigger Processor (CTP)**, new **Local Trigger Interfaces (LTIs)**, and new firmware for the **Muon-CTP Interface (MUCTPI)** will be developed. All modules will be ATCA blades and use most likely Xilinx Kria SoM. Usage of Petalinux with Centos 7 rootfs and moving to Alma 9
  - Development of **SoC to DAQ communication library** using HTTP + nginx server. A protype is ready !
  - Exploration of the the VERSAL Premium :
    - **FLX182**, a prototype card for Front-End Link eXchange for Run 4
    - **Global Comon module v3** for ATLAS Global Trigger

Workshop – Projects Presentations

Since the last SoC Workshop (June 2021)

- CMS :
  - **X20 Platform** will be applied for the upcoming phase II upgrade of L1 trigger (ATCA standard). The SoC of power module was upgraded from Zynq 7000 to Zynq US+ MPSoC using the Xilinx KRIA SoM
  - **Serenity-S1 ATCA Card** : Developed mainly for CMS HL-LHC Level-1 Trigger (700 are expected). Split Boot v2 (Usage of QSPI to **synchronize** the main software stack in the eMMC with the network at boot time) on Kria K26 SoM
  - **DAQ and Timing Hub (DTH)** board developed by the CMS DAQ group for the Phase-2 upgrade second prototype is fully tested. ATCA form factor with a Zynq US + MPSoC in the RTM. Currently using a Trenz SoM → possible change to Xilinx Kria
  - Phase 2 **Barrel Muon Trigger system** (ATCA form factor) controller is based on Zynq US+ using an Enclustra SoM. The SoC is used for control and Realtime monitoring of the payload. Currently using Centos and plan to move to Xilinx Kria
  - Exploration of the the VERSAL :
    - Quasi-real time data processing applications in a high-energy physics exploiting neural networks. Comparison between VERSAL and Zynq shows clear performance differences

Workshop – Projects Presentations

Since the last SoC Workshop (June 2021)

- **Cross CERN experiments**

  - **Caribou** : a versatile data acquisition system used by multiple collaborative frameworks (CERN EP R&D, RD50, AIDAinnova) for the qualification of novel silicon pixel detector prototypes. Entrening its upgrade phase with new features – Yocto based OS Migration from Zynq 7000 to Zynq US+ (Enclustra SoM)
  - **HyperFPGA** is an experimental cluster developed with the philosophy of HPC platform. Interoperability with an open SoM form factor and pinout. Custom OS accommodate remote management requirements using JupyterHub
  - **SoC Development Platform :** fully open-source initiative that ambition to provide a RAD-TOL SoC ecosystem for high energy physics. Among the advantages : replacing FSMs ASIC with CPU, reduce design and verification efforts

Workshop – Tutorial Presentations

I. Streamlining of the build process for **boot files using Yocto layers** for a team plated approach

II. Harnessing the Power of **Continuous Integration** for Multi-Board Projects

III. Advancing Automated Firmware Testing using Modern Infrastructure such as **Kubernetes/Container**

Quick Take Away

Concluding the 3rd CERN SoC Workshop

Workshop – Quick Take Away

From Vendors :

- Better **lead time :** 66 weeks → 13 weeks
- Some efforts are being made on standardization

From Projects :

Still a growing increase of SoC Usage across all sectors and experiments:

- ATLAS and CMS has already widely adopted SoCs for Detector control and their applications
- CERN new radiation monitoring system CROME was deployed at the booster, PS, SPS, the NA, SM18 …
- DIOT, Beam Instrumentation Pixel (BIPXL) are already in operation

A Wide adoption GIT CI → Becoming a standard approach for SoC ?

Wide adoption of SoM. Very few projects are directly using SoCs

Most systems are using Zynq US+ MPSoC, Zynq-7000 used were necessary

Workshop – Quick Take Away

From Projects :

Experiments specific :

- Geographically Aware Network Configuration (as specified by ATCA specs) is being introduced
- Full Network Boot for CMS and ATLAS
- **SoC will play a major role in custom ATCA electronics during ATLAS phase 2 upgrade**
- Focus is being moved towards infrastructure and network services for SoCs
- Many projects are considering moving to Xilinx Kria
- **Exploration is ongoing to use ACAP VERSAL**

Workshop – Quick take away

General remarks :

- Still very broad strategies on how to use SoCs
- ? Common need for an OS, basic software support for peripherals & common firmware blocks ?
  - → Initiatives to harmonize OS for SoCs and FECs for ATS sector
  - → Initiative to standardize the communication between SoCs and FECs using FESA at ATS (needs validation from the CTTB)
  - → Initiatives to harmonize the SoC infrastructures at ATLAS and CMS. Harmonization of network management and booting mechanisms for SoCs over their respective TNs
- IT is consolidating a strategy to provide support for SoCs CI

- General willing to share designs, codes and strategies :
  - → Example of EPOS framework (ATLAS EMP) can be used for other projects
- Long-term maintenance and support are still open questions

Outlook

How to continue from here:

- **Interest group: *system-on-chip@cern.ch*, SystemOnChip (Mattermost)**
  - **Continue with regular meetings: https://indico.cern.ch/category/11883**
  - **Use twiki page to exchange information/documents: https://twiki.cern.ch/twiki/bin/view/SystemOnChip/WebHome**
  - **Use gitlab for sharing software: https://gitlab.cern.ch/soc**
- **SoC organising committee, SoC-Workshop-Organisers@cern.ch :**
  - **Follow up with CERN-IT on Linux**
  - **Follow up with CMS&ATLAS SysAdmin on system aspects**
  - **Anything else we can do to facilitate sharing, e.g. common test environments, common software?**
- **Next SoC workshop in 1 to 2 years from now?**

A Big Thank You

- To all presenters for the presentations and tutorials!
- To all vendors for their presentations and for time and efforts to set booths
- To the conveners
- To Cinzia Pinzoni, Fabio Pigozzi and Andre Pinho for their help with the workshop logistics
- To CERN-IT for support of Indico and Zoom, … To all of you for the interesting discussions!
- To the groups leaders and sections leaders who funded the coffees breaks (EP-ESE, SY-EPC, EP-CMD, EP-ADT)

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