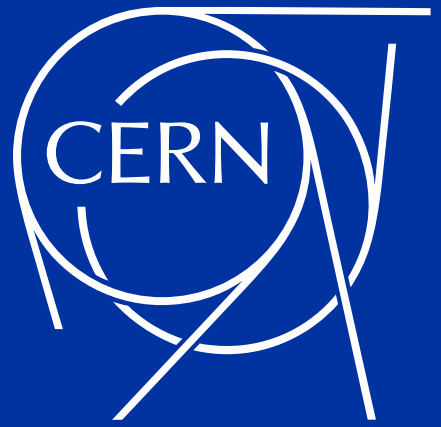

RFSoC-based Development for HL-LHC Beam Position Monitors

Irene Degl'Innocenti – SY-BI-BP

HL-LHC BPM team: Elif Balci, Manuel Gonzalez Berges, Andrea Boccardi, Stephen Jackson, Michal Krupa

03/10/2023 – 3rd CERN System-on-Chip Workshop: Project Session #1

Outline

- Overview of HL-LHC Beam Position Monitor Project
- Resources estimation for the HL-LHC BPM Digital Processing
- RF System-on-Chip Technology
- RFSoC Scope: beam raw data acquisition prototype
- Next steps for HL-LHC BPM Electronics
- Conclusions

Outline

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- **Conclusions**

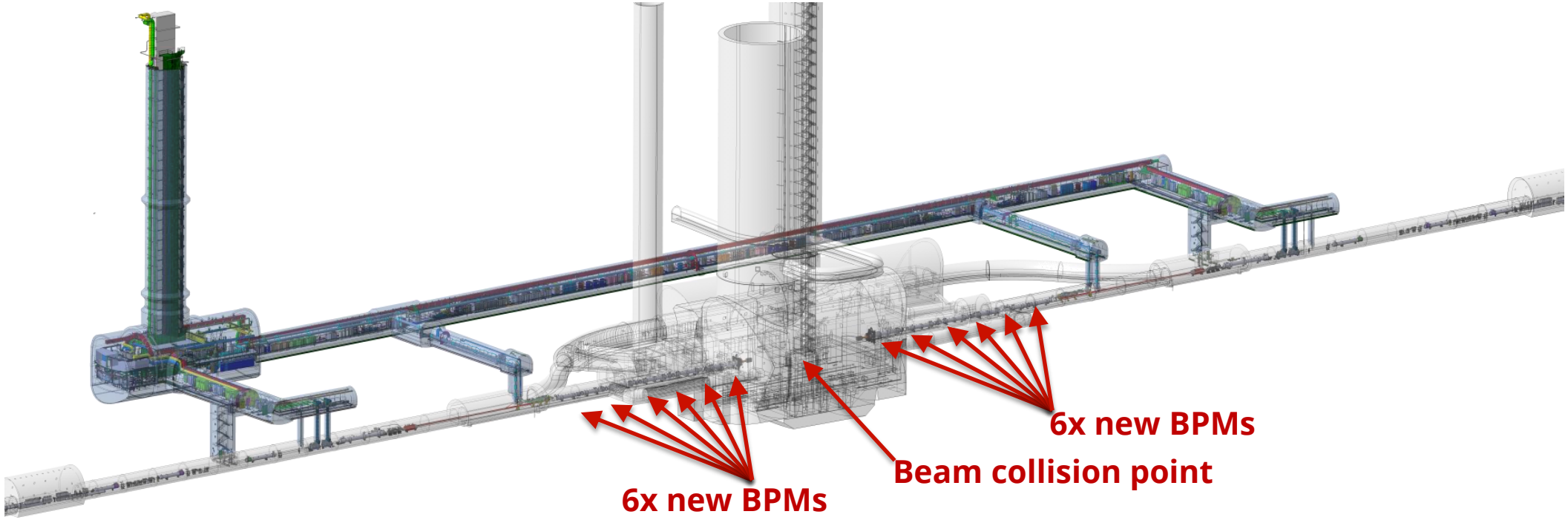
HL-LHC Beam Position Monitor Upgrade

What is a Beam Position Monitor?

HL-LHC Beam Position Monitor Upgrade

New BPMs close to interaction regions

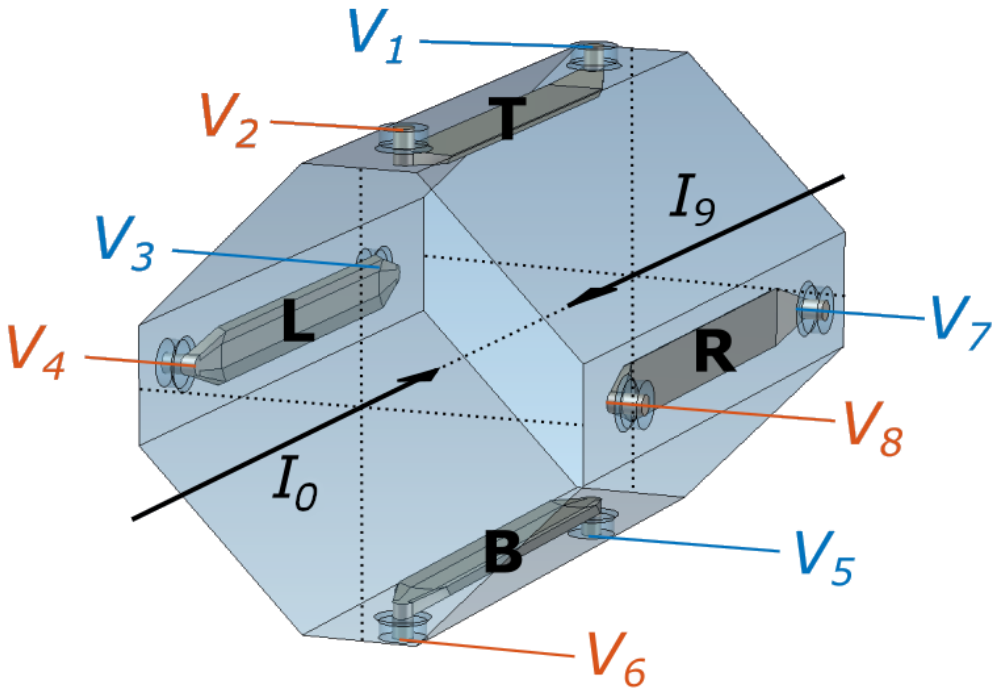
New BPMs in the immediate vicinity of interaction regions 1 (ATLAS) and 5 (CMS), where the two beams coexist within a single pipe

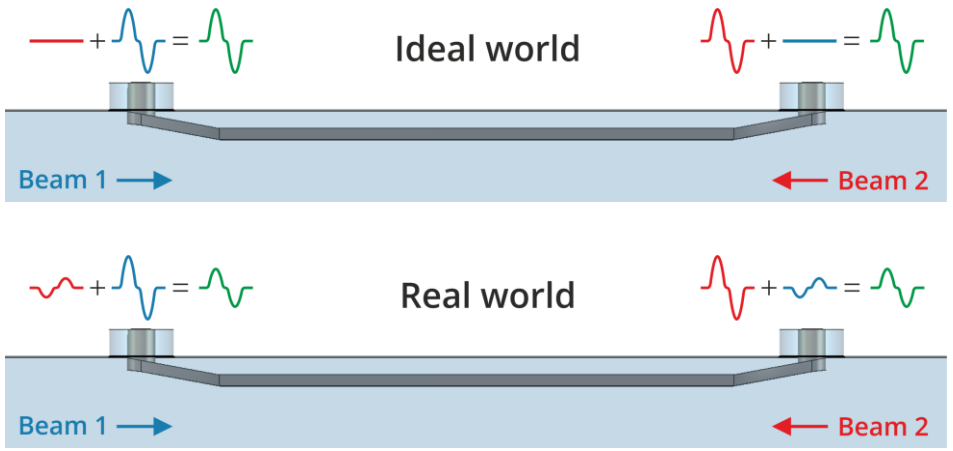


HL-LHC Beam Position Monitor Upgrade

Directional Couplers

In a good directional coupler a signal is seen mostly at the upstream ports





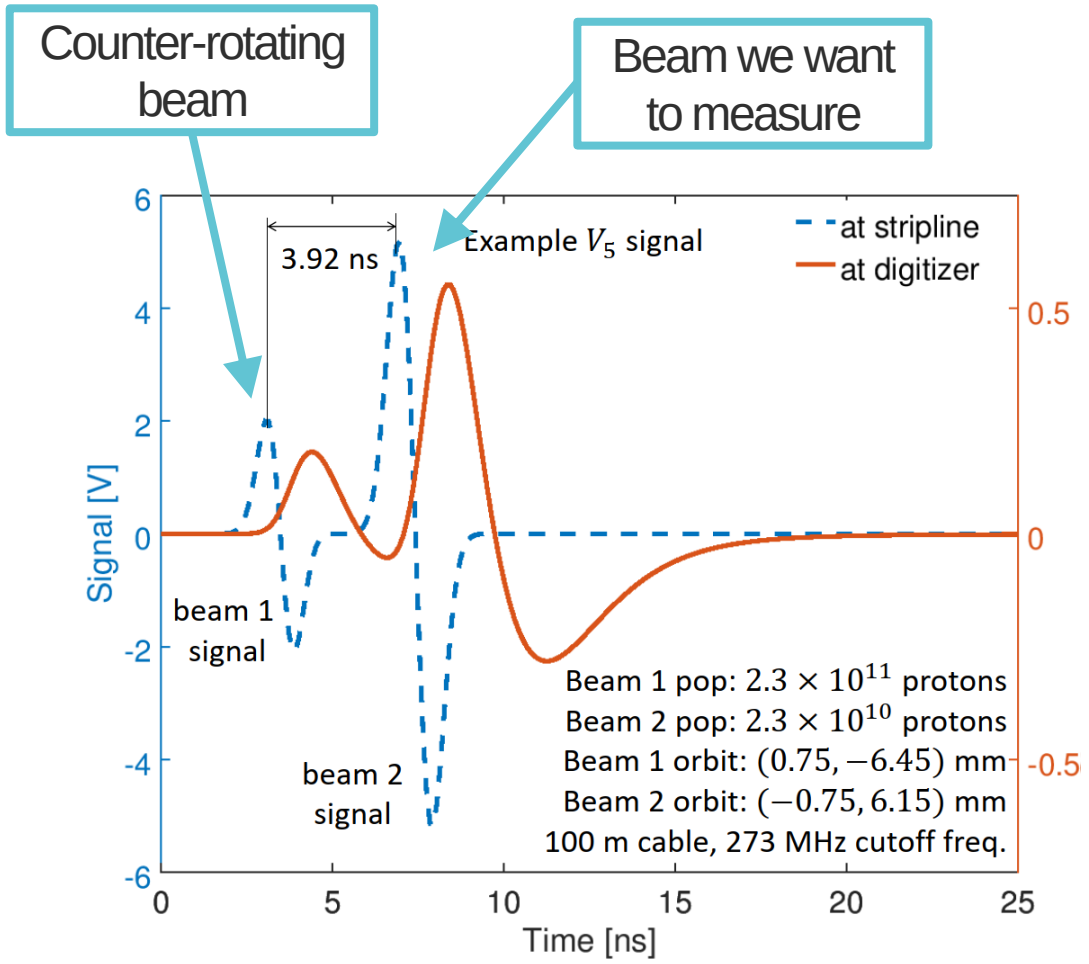
HL-LHC Beam Position Monitor Upgrade

Beam to beam distortion

The presence of the other beam affects the measurement when:

- Short bunch crossing time
- Intensity of other beam significantly higher

The distortion of the beam signals due to the presence of the other beam must be compensated for



Outline

- Overview of HL-LHC Beam Position Monitor Project
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- Summary

Resources Estimation for HL-LHC BPM
Digital Acquisition Requirements per Stripline

- **Fast digital acquisition of 8 waveforms** → 8 ADCs: > 2 GSps, > 8.5 ENOB
- **Digital Signal Processing implementation**
  - **Power** computation
  - **Power Compensation algorithm** (each waveform: 4 multiplications + 1 division + 2 square root) [IBIC21]
  - **Beam Position Monitor** functionality
    - **Continuous log of averaged low-volume data**
    - **On demand storage of high-volume data**
    - Calibration → 8 DACs

→
- Logic
- Memory Size
- Memory Bandwidth
- Transmission Bandwidth

Resources Estimation for HL-LHC BPM

Resources estimation

Resources	Required qty.
ADCs	8
DACs	8
Internal memory	30 Mb
DSP	172
LUT	20521
FF	50644
DDR	768 Mb
DDR WR peak BW	22 Gbps
Read-out BW	54 Mbps

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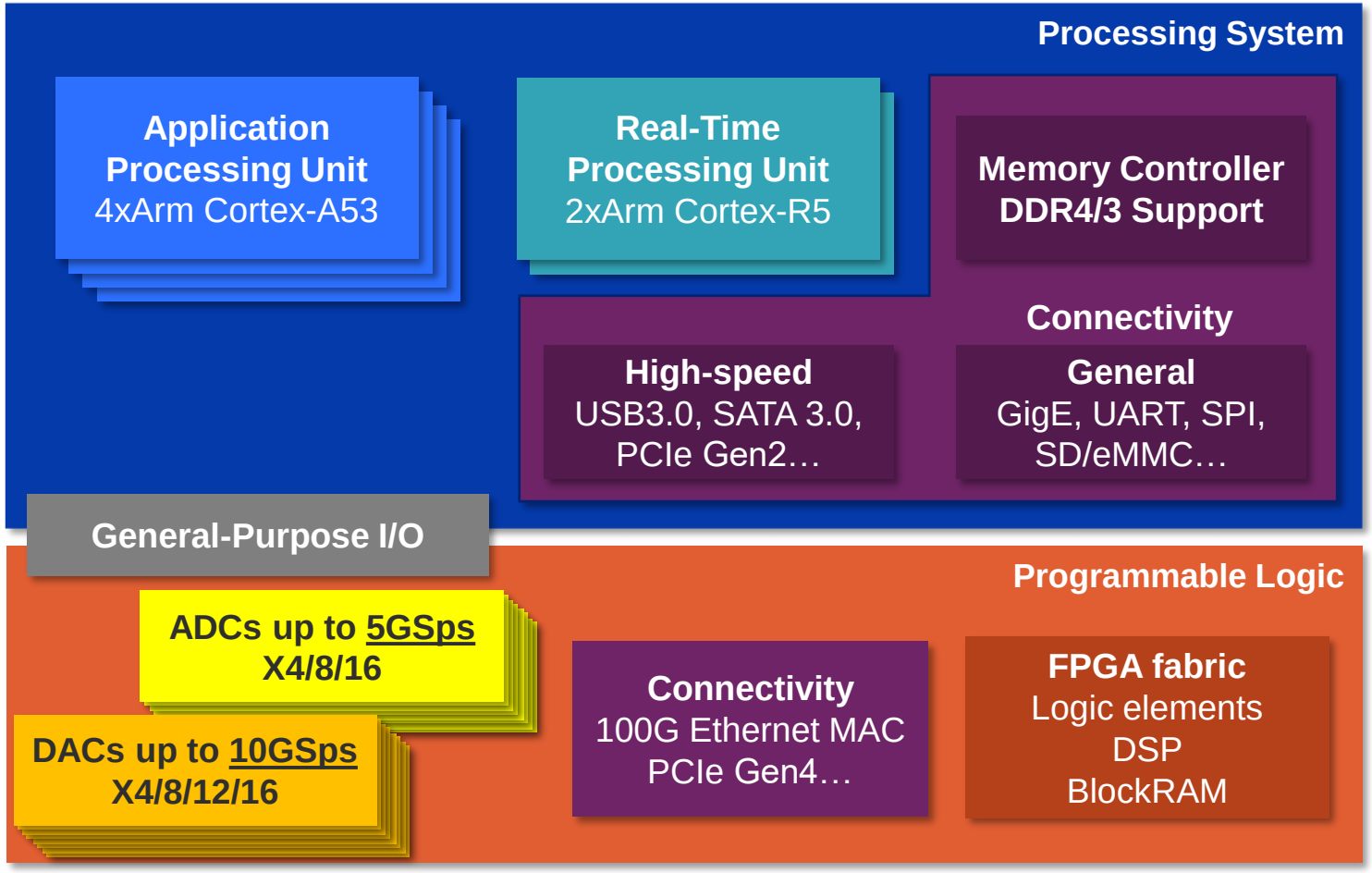
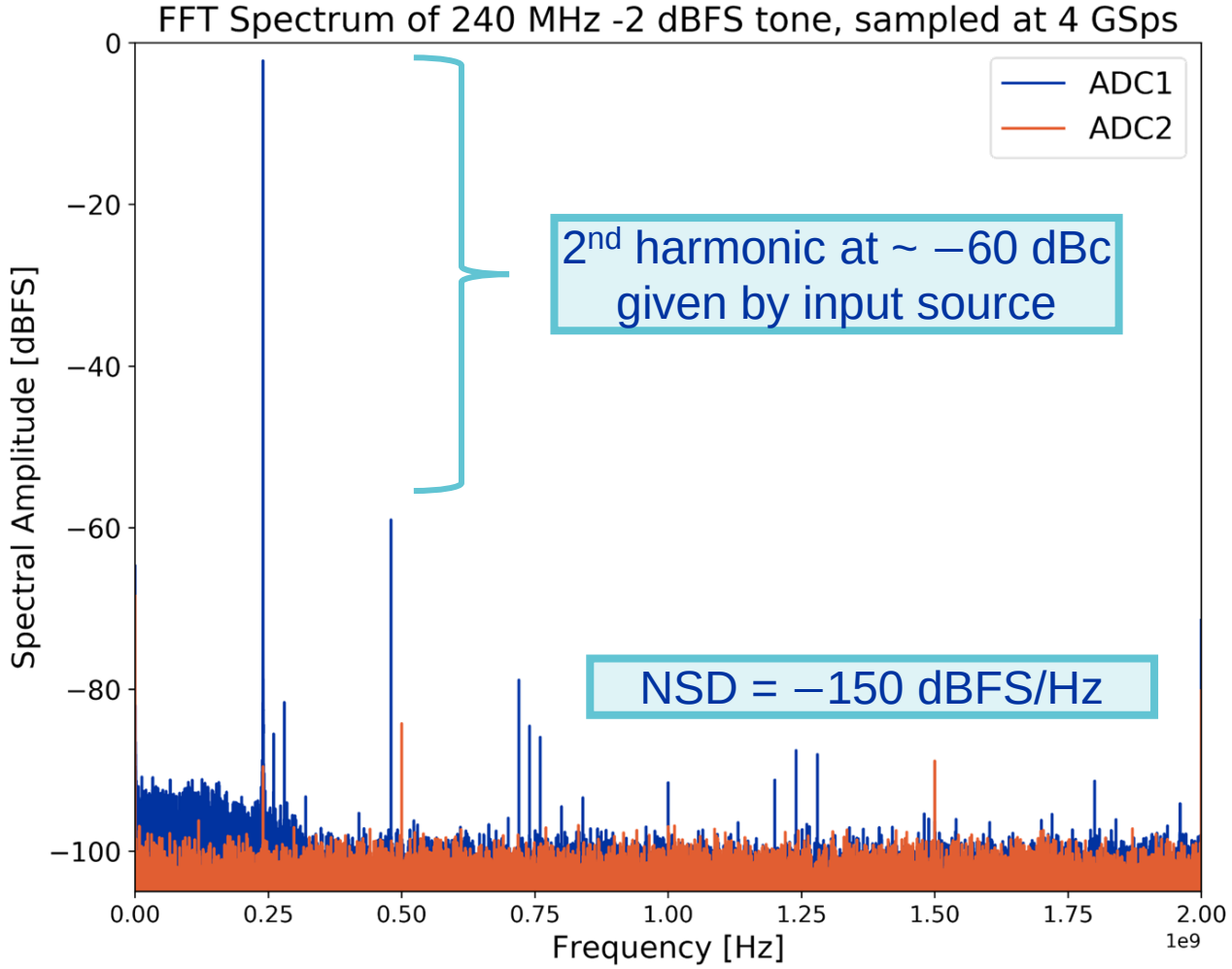
The RF System-on-Chip Technology
Definition



The RF System-on-Chip Technology

ADC Performance

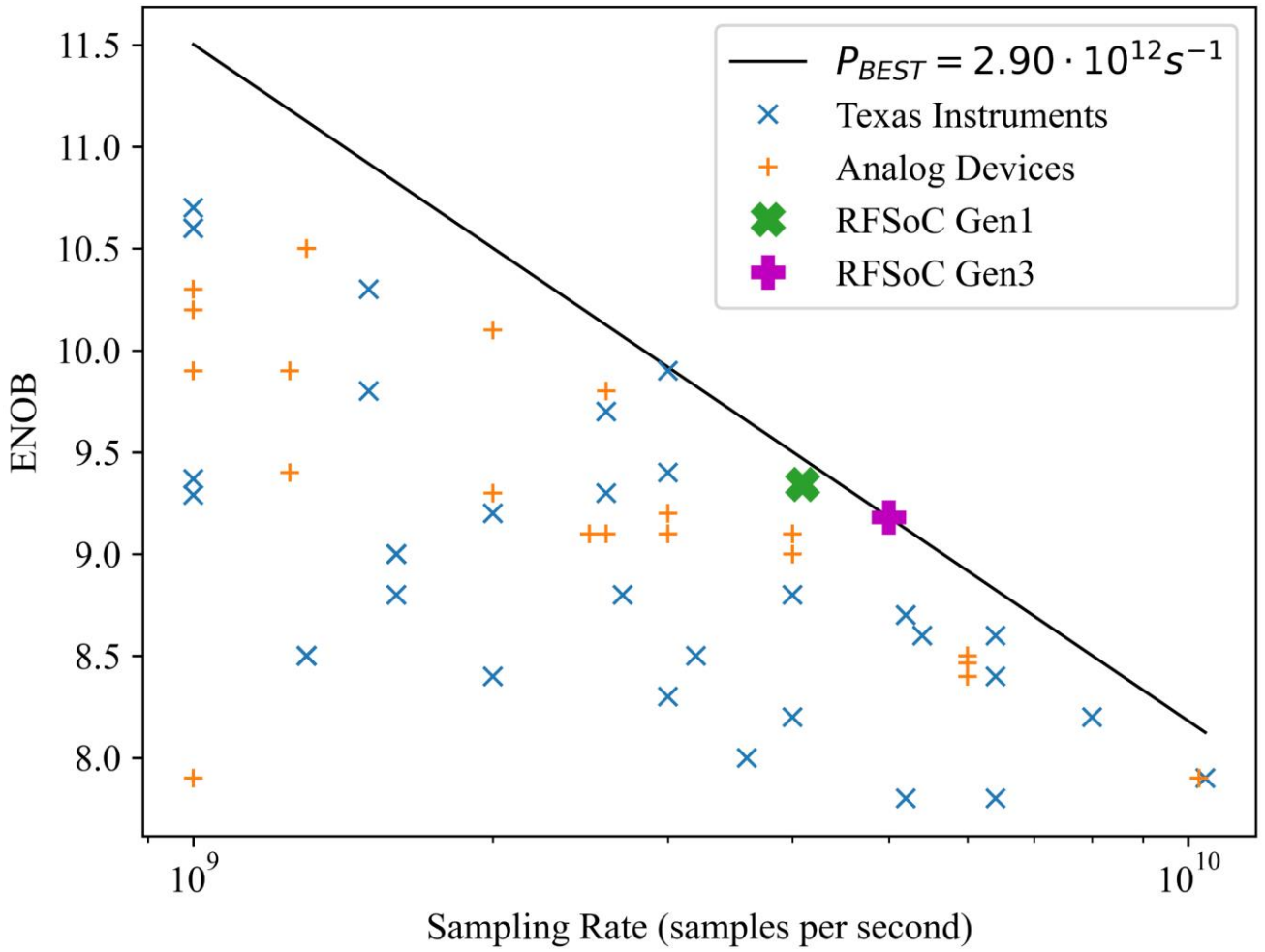


	SNR (dBFS)	SFDR (dBFS)	ENOB
AD9208[1] (14b, 3 GSps)	60.2	78	9.7
RFSoC (12b, 4 GSps)	*58*	74[3]	*9.3*
TI 12DJ4000RF[2] (12b, 4 GSps)	57	67	9.0

1. Analog Devices, AD9208 Data Sheet link
2. Texas Instrument, ADC12DJ4000RF Data Sheet, link
3. J.E. Dusatko, “Evaluation of the Xilinx RFSoC for Accelerator Applications”, in *Proc. NAPAC'19*, Lansing, MI, USA, Sep. 2019, pp. 483-486. link

The RF System-on-Chip Technology

ADC Performance

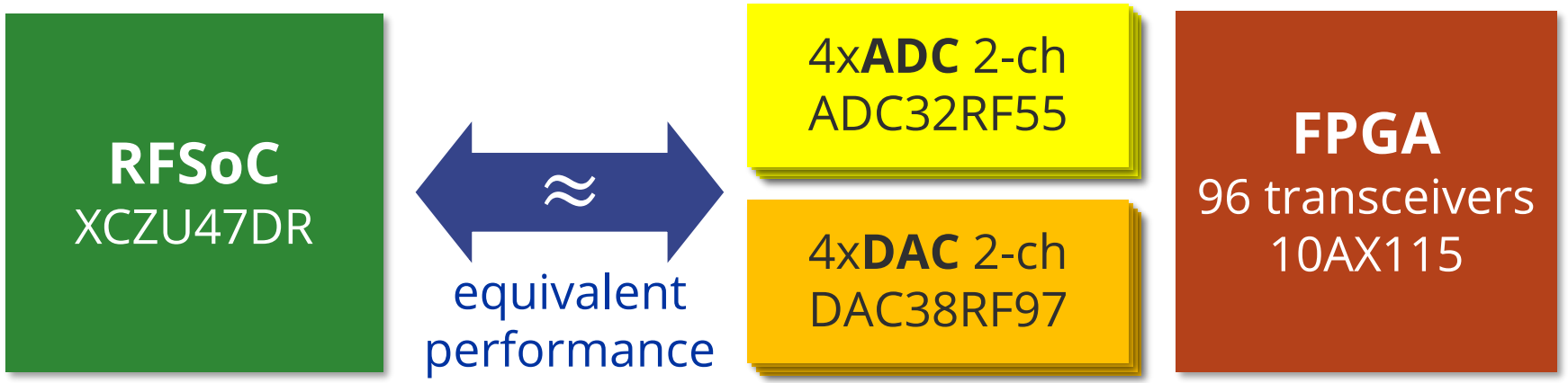


Measurement of performance

$$P = 2^{\mathrm{ENOB}} \times F_s$$

RFSoC Gen3 ADCs have **excellent P**

The RF System-on-Chip Technology
Comparison with discrete solution



	Discrete	RFSoC
Cost (k$)	18.0	20.3
IC count	9	1

Total cost per architecture for IC, indicative prices for small quantities found online.

Cost

IC
~ 10% pricier

Vendor lock-in

PCB
1/9 of IC
Less PCB area
Less power

Development
Less interfaces
OS and CPU

Outline

- Overview of HL-LHC Beam Position Monitor Project
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- **RFSoC Scope: beam raw data acquisition prototype**
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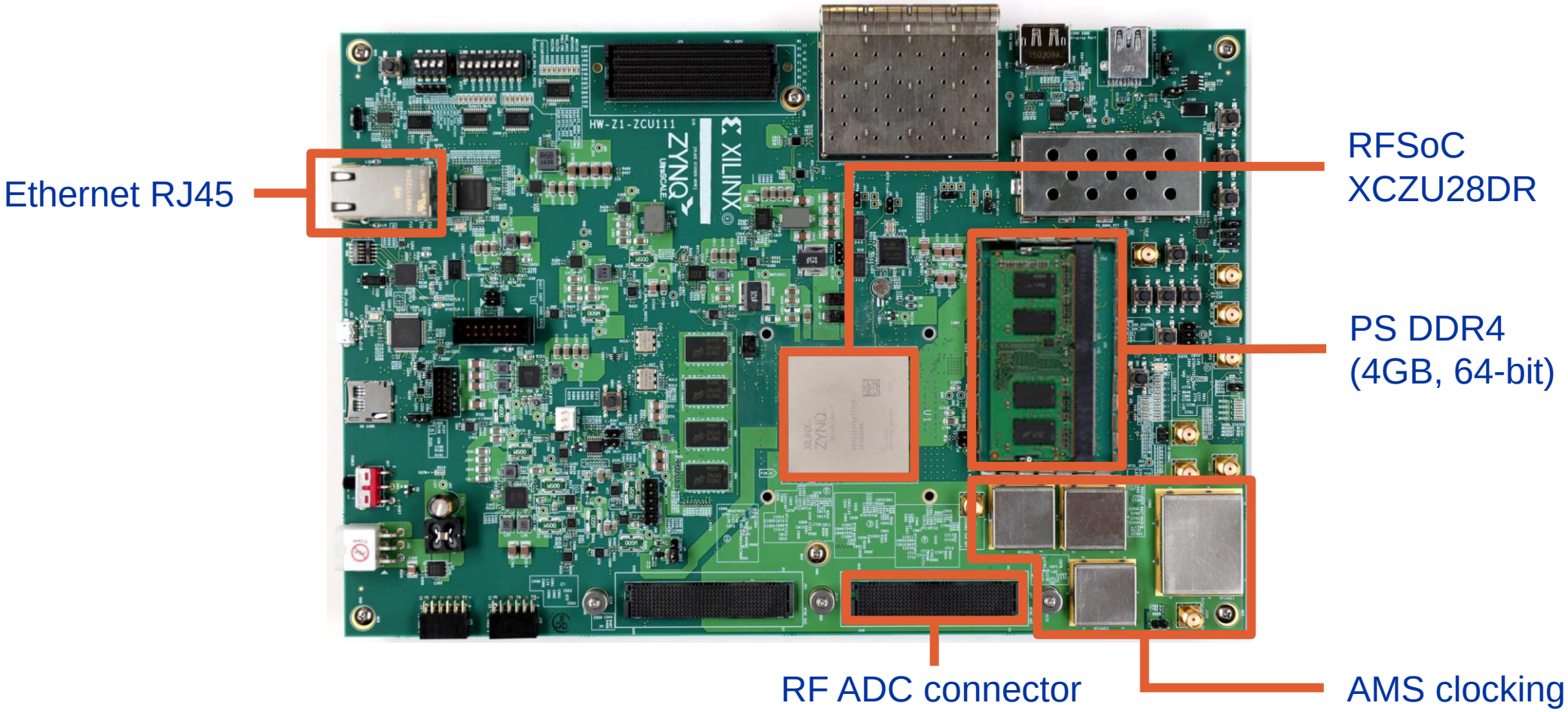
- Conclusions

RFSoC Scope: Beam Raw Data Acquisition

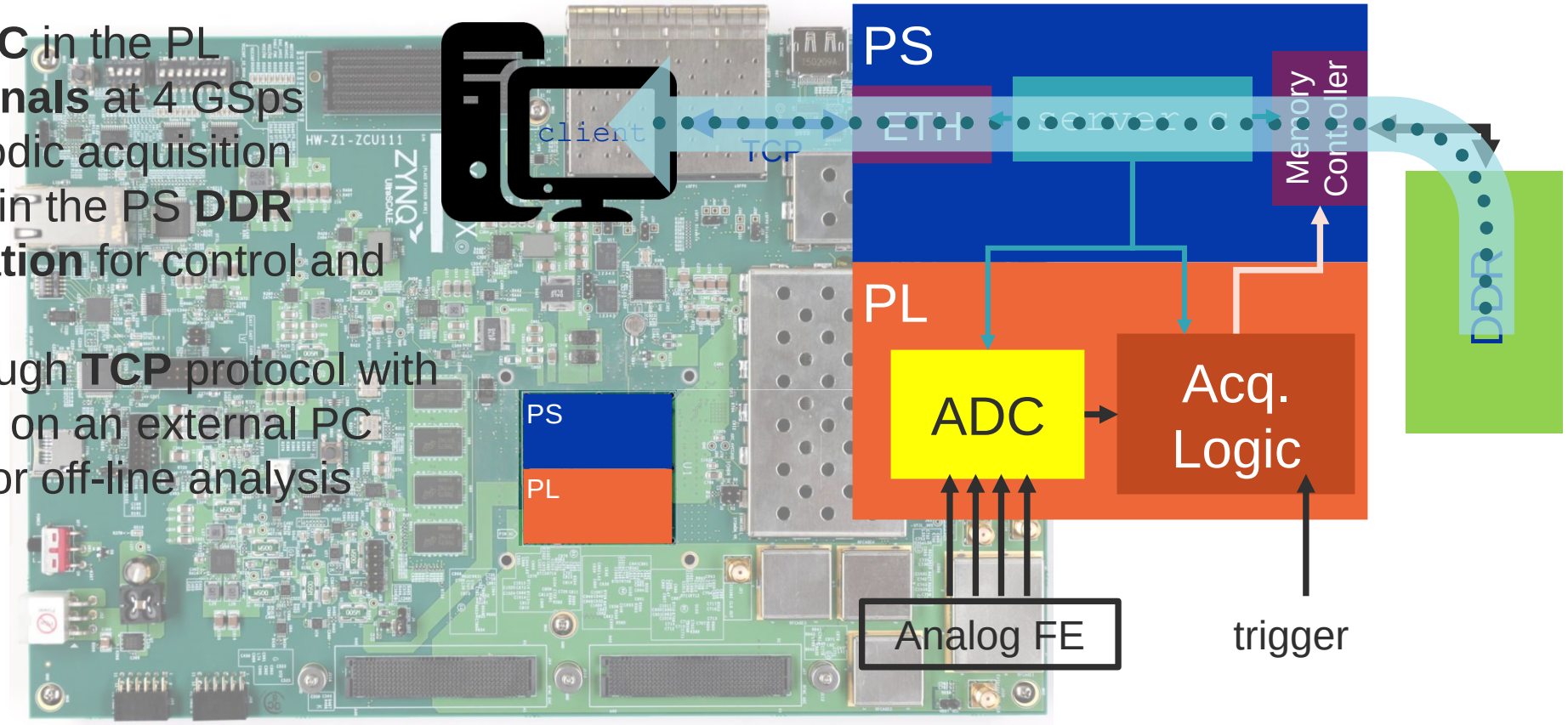
RFSoC 4-channel scope on ZCU111 evaluation board



RFSoC Scope: Beam Raw Data Acquisition

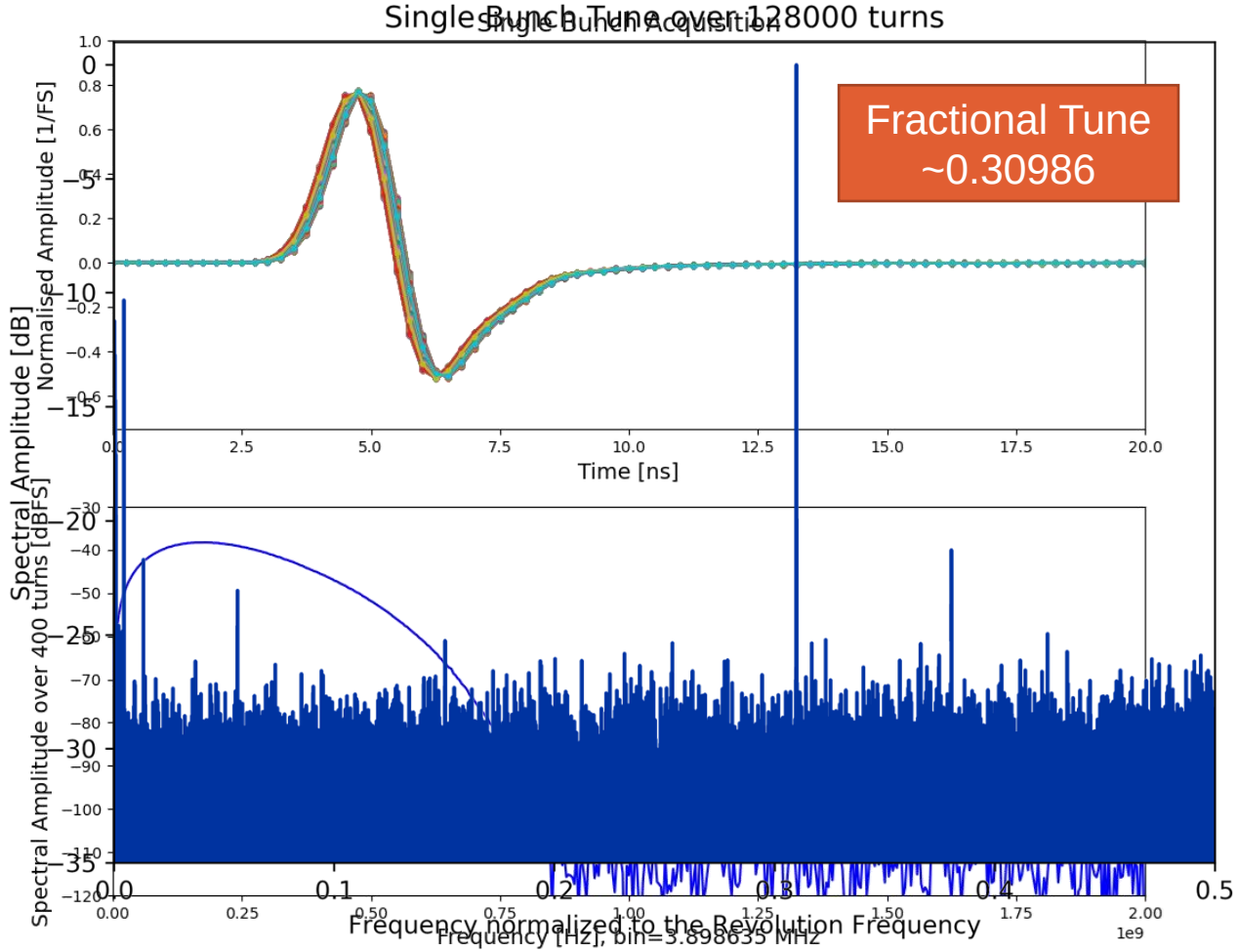
RFSoC 4-channel scope on ZCU111 evaluation board

- **FPGA logic** and **ADC** in the PL
  - digitization **4 signals** at 4 GSps
  - segmented periodic acquisition
- Storage of raw-data in the PS **DDR**
- **APU server application** for control and data transfer
- Communication through **TCP** protocol with the software running on an external PC
- Raw-data read-out for off-line analysis



RFSoC Scope: Beam Raw Data Acquisition

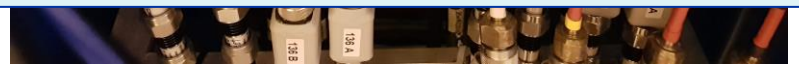
Measurements of LHC Stripline



Several raw data acquisitions for the HL-LHC BPM studies

- 4 channels at 4 GSps
- Memory per acquisition: ~**2 GB**
- Longest acquisition (<400 MB) single bunch for **128000 consecutive turns** (more than 11s of observation)

- **First Results: IPAC23-THPL119**



RFSoC Scope: Beam Raw Data Acquisition

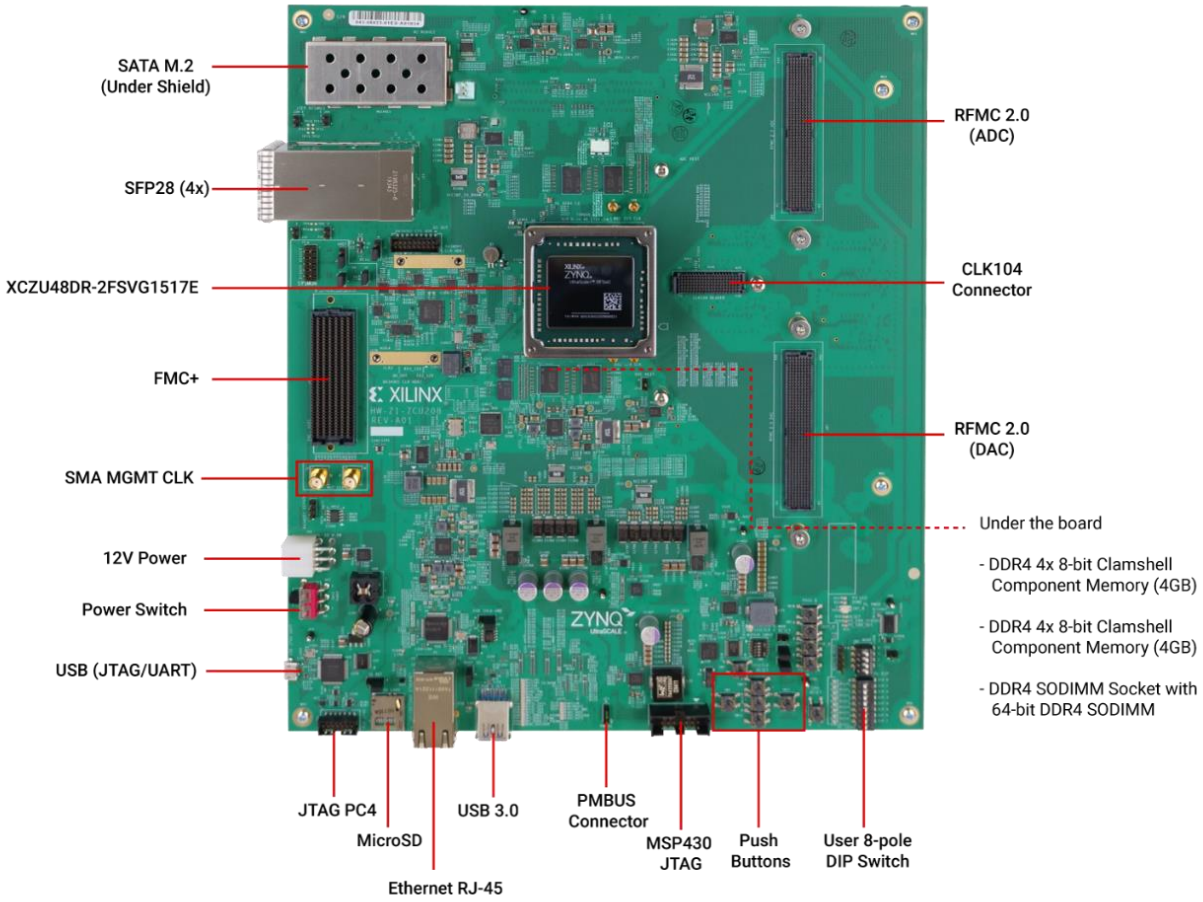
RFSoC Gen3 Development

Purchase #2 ZCU208 Evaluation Kits mounting RFSoC Gen3

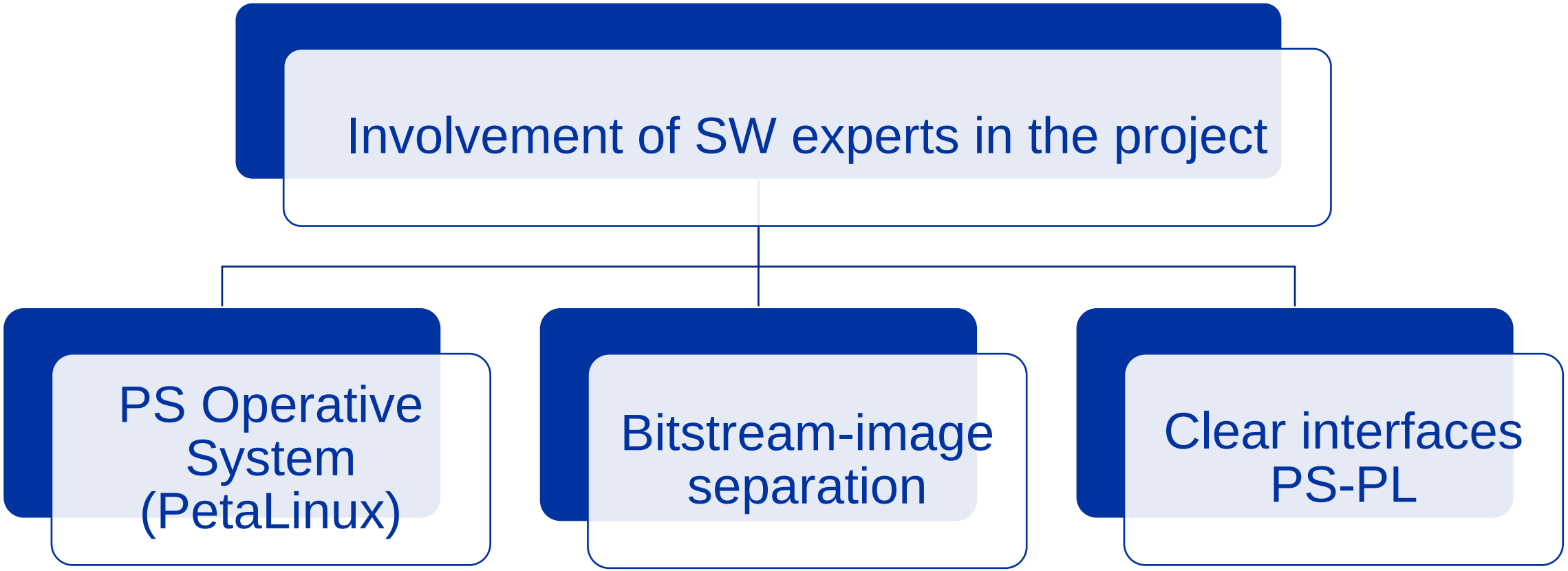
- **Main difference between Gen1 and Gen3:**
  - Increased maximum sampling rate

    ADC: 4.096 GSps → 5.0 GSps

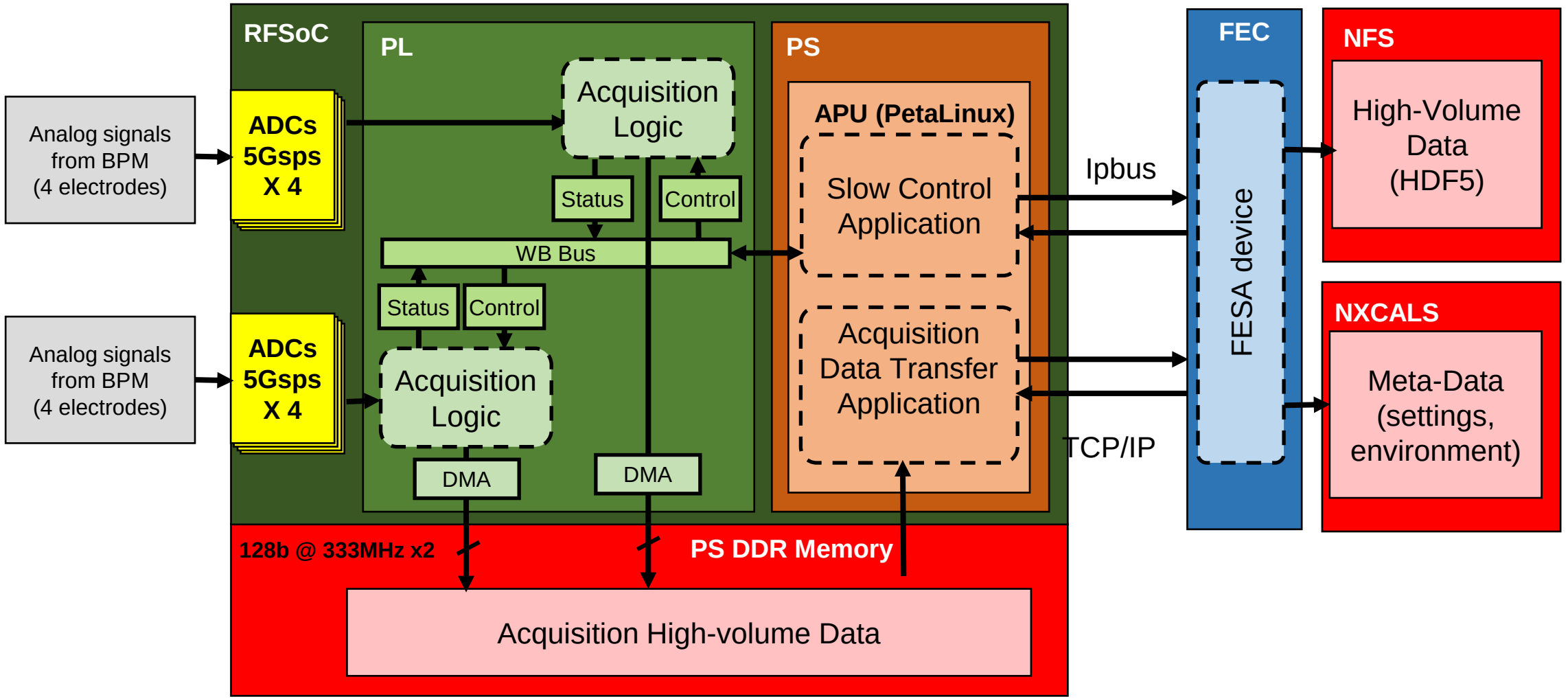
    DAC: 6.554 GSps → 10.0 GSps
- **DAQ Gateware & Firmware upgrade:**
  - 8 channels at 5 GSps
  - Integration with accelerator control system



Integration with CERN Accelerator Control System

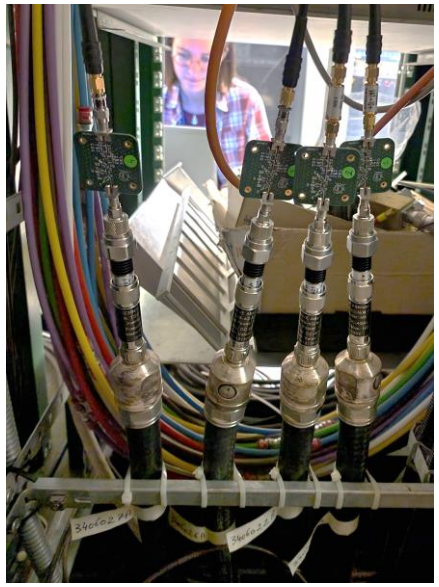


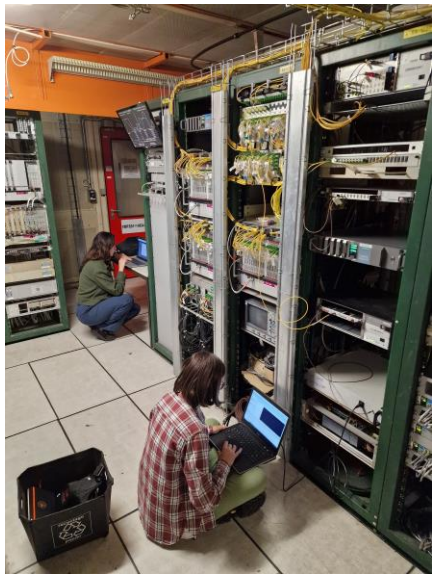
Integration with CERN Accelerator Control System

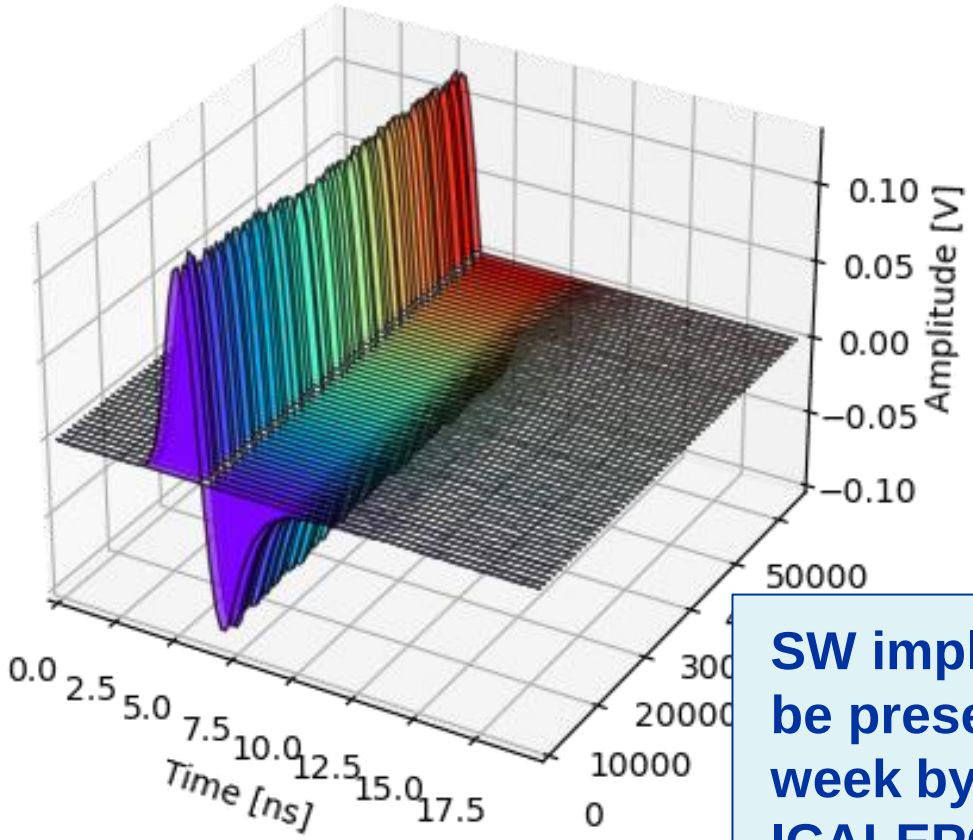


Integration with CERN Accelerator Control System

Measurements of SPS Button







SW implementation to be presented next week by Elif Balci at ICALEPCS 2023

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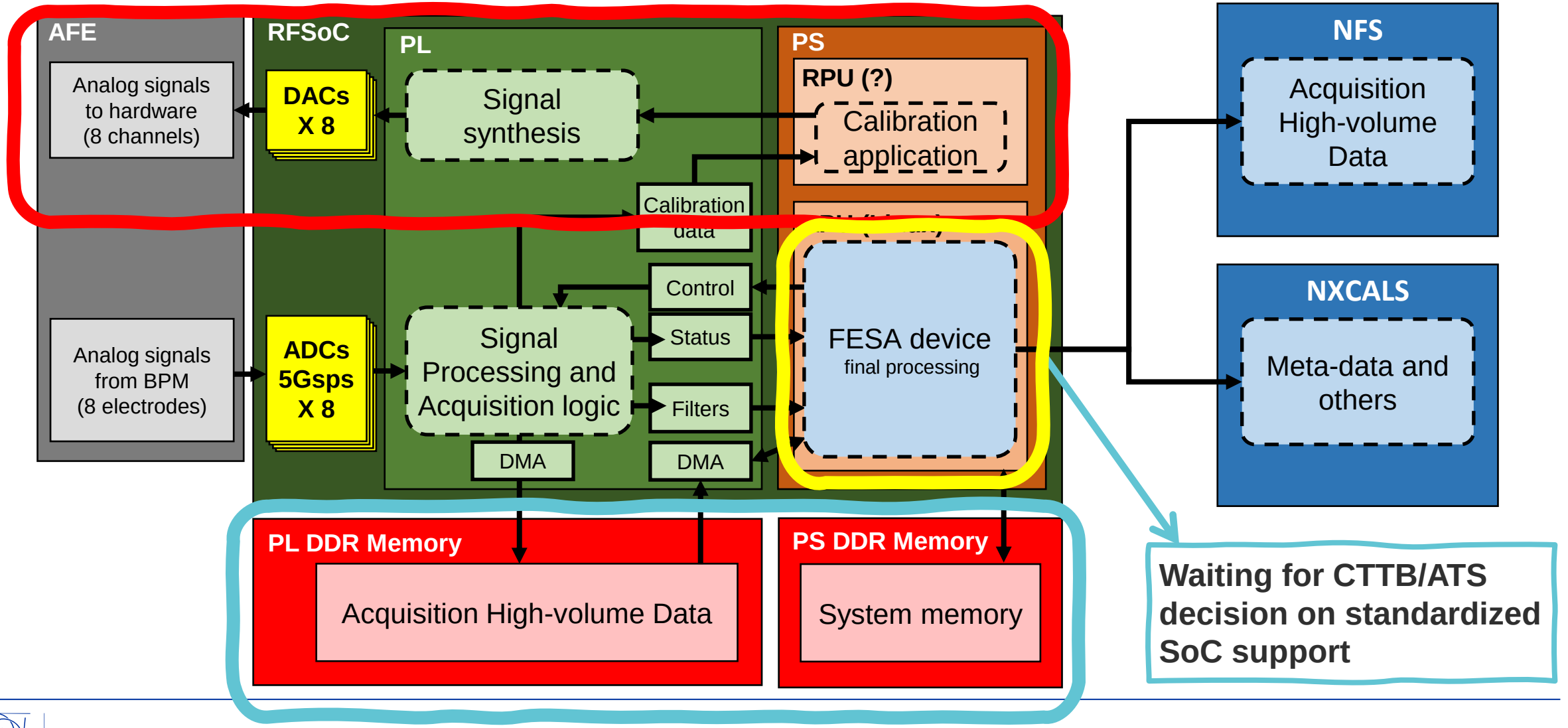
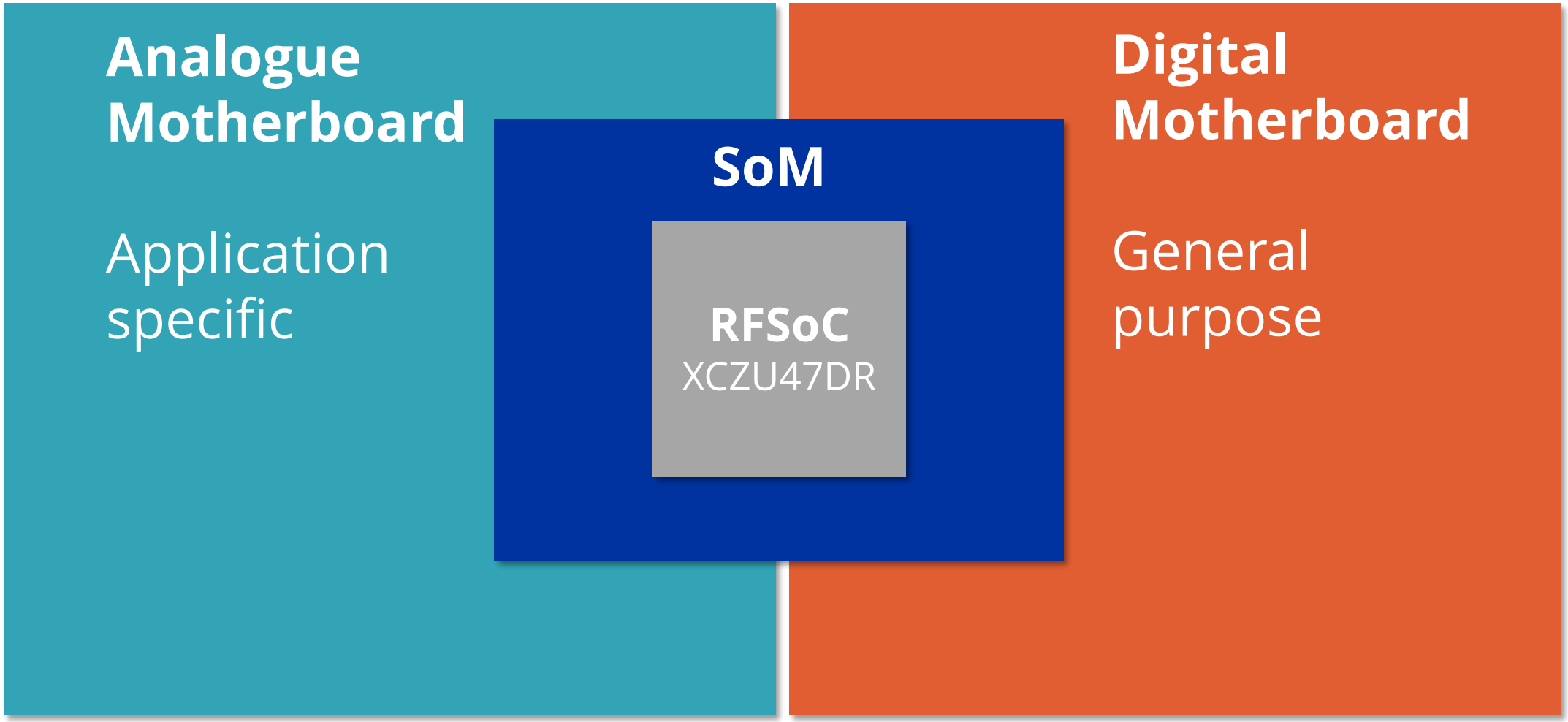
Next steps for HL-LHC BPM Electronics

GW-FW-SW architecture



Next steps for HL-LHC BPM Electronics

Definition of hardware architecture



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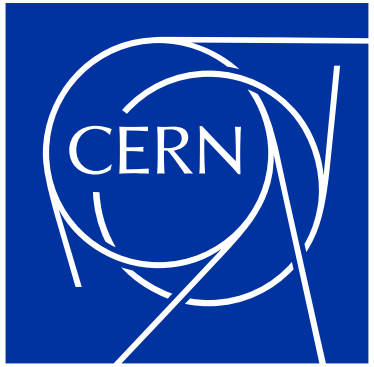
Conclusions

- **Development of the digital electronics for the HL-LHC BPM is a challenging task requiring fast digitization and fast digital signal processing of 8 signals**
- **RFSoC by Xilinx is a promising candidate, combining multi-channel multi-giga samples per second RF converters with programmable logic and CPUs**
- **The RFSoC Scope project and its history was presented as an example of RFSoC based development and collaboration effort**
- **Next steps for HL-LHC BPM Electronics:**
  - HW: investigation of SoM architecture
  - GW: implementation of PL DDR Controller, alongside with dedicated signal processing
  - SW: **great potential for standardization** (Linux image, booting, FESA-on-SoC)



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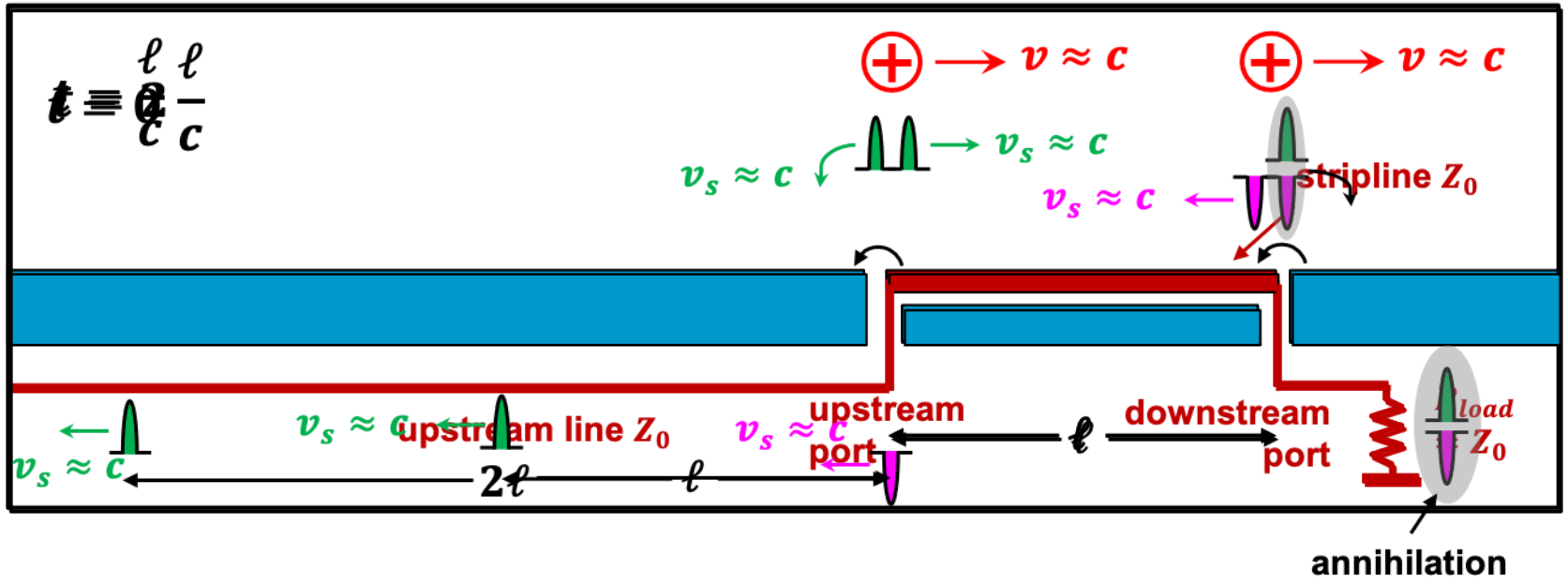
HL-LHC Beam Position Monitor Upgrade

Directional Couplers



Power compensation algorithm

BEAM DISENTANGLEMENT ALGORITHM

The **power compensation method** subtracts the power of the counter beam from the total power measured on each port in order to recover the main beam power. A full derivation of the algorithm is available in [6]; here, we note the beam disentanglement algorithm amounts to **solving a quadratic equation for each port** to give the value of κ, the amplitude of the main beam signal in each case.

$$\kappa_1^2 + \left(2\frac{\chi}{\psi_c}\sqrt{\frac{\psi_2}{\psi_c}}\right)\kappa_1 + \left(\frac{\psi_i}{\psi_c}\frac{\psi_2}{\psi_c} - \frac{\psi_1}{\psi_c}\right) = 0$$

where $\psi_1 = \sum_{n=1}^{N} V_1[n]^2$

$V_1[n]$ represents the sequence of samples observed on port 1

ψ_c, ψ_i and χ also represent the sums of sequences of samples, but they are calculated from **predictions of the signals** induced by the passage of a **reference beam**. ψ_c and ψ_i correspond to the predicted coupled and isolated signals multiplied by themselves; χ corresponds to the cross-term.

Courtesy of Michal Krupa and Douglas Bett

Resources Estimation for HL-LHC BPM

Digital Signal Processing distribution