BIPXL MPSoC Readout

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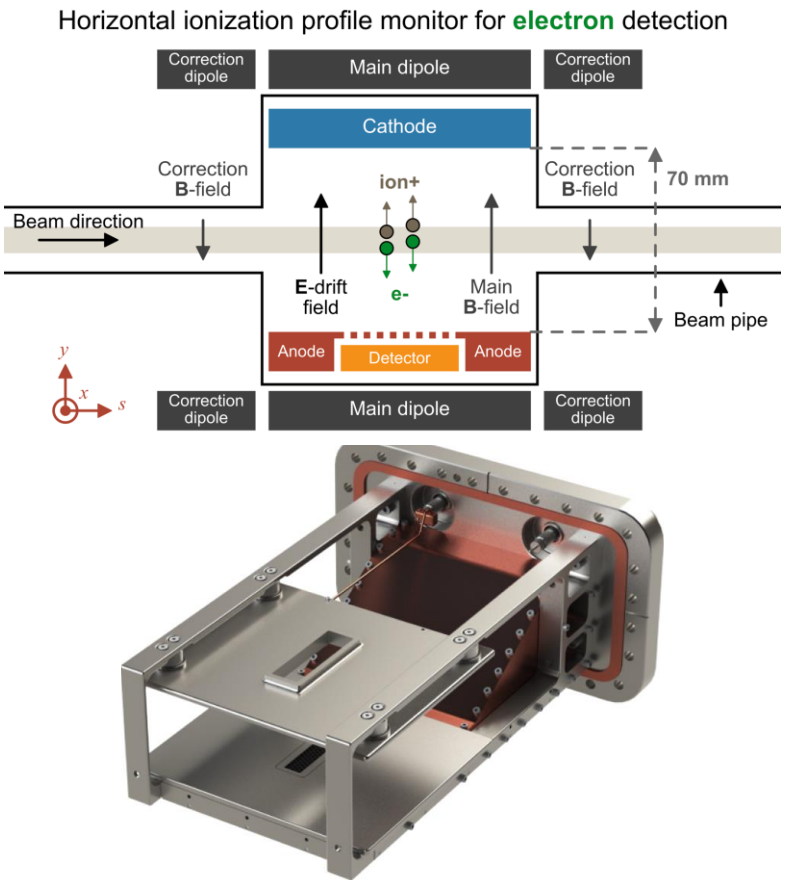
Outline

- Beam Gas Ionisation, BGI
- Readout overview
- MPSoC Back-end
- Back-end External View
- Back-end Internal View
- Future plans

Beam Gas Ionisation, BGI

- Non-invasive measurement of the beam profile:
  - 1. Beam ionizes rest gas particles in the beam pipe
  - 2. Transport ionization electrons with E-field and B-field
  - 3. Image ionization electrons with a detector
- Based on Timepix3:
  - Position (65k pixels with 55um pitch)
  - ToA (1,56 ns of resolution)
  - ToT (< 2KeV of energy resolution)
- Two operational BGIs installed in PS since 2021

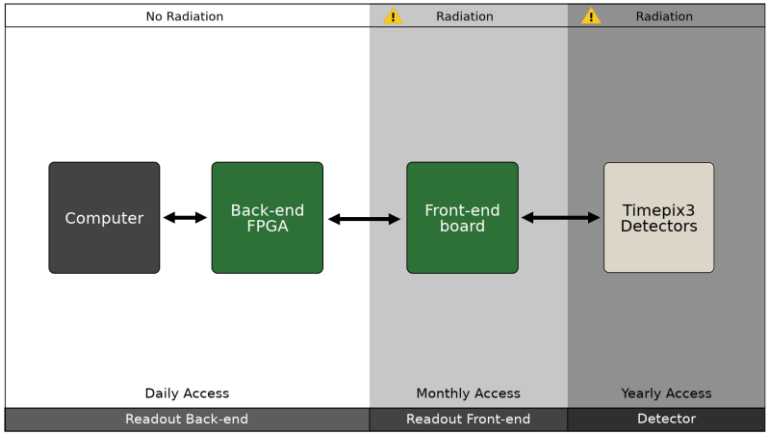


System requirements

- 4 TPX3 → 8 DataOut each one of 320 Mbps = 10,24 Gbps
- Processing requirements:
  - To publish all the data before the next cycle starts.
  - Around 10k events per profile and about 1 profile per 2ms.
    - 60 bits per event
    - Typical case: 2ms acq window every 10ms → 60 Mbps
- Beam loss removal → offline.

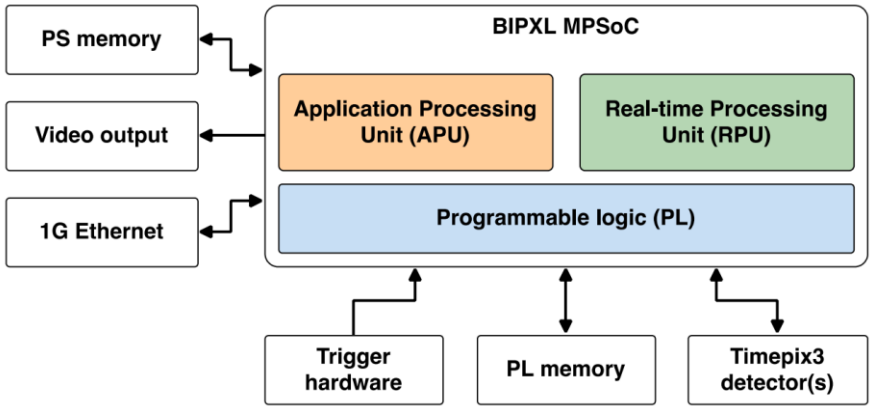
Readout overview

- The readout consists of 3 parts: **Back-end**, **Front-end** and the **detector(s).**
- Back-end:
  - Until July 2022 → Virtex 7 FPGA VC707
    - Limited profile processing capabilities just using FPGA.
  - Back-end requirements:
    - Generic platform for all the Timepix applications.
    - Real-time processing of Timepix events.
      - Bunch by bunch
    - Simply debug, development and deployment.
    - Long term availability.
    - Support and expertise at CERN.



→ Zynq UltraScale+ MPSoC

Zynq Ultrascale+ MPSoC Back-end



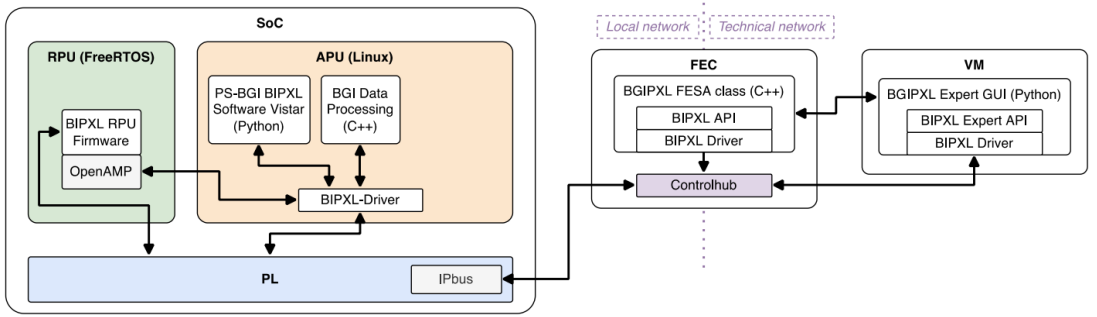
ZCU102 board

- HDMI/DP output
- 1G ethernet (PS)
- 4 SFP
- Trigger FMC mezzanine

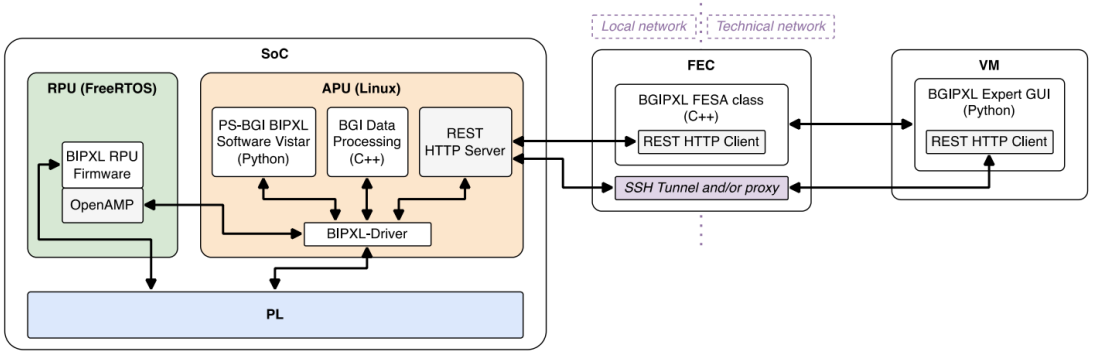
APU runs Linux.
RPU cores will run in lock-step mode with FreeRTOS.
PL does the low-level assembly and transfer of bits and packets.

External view: REST

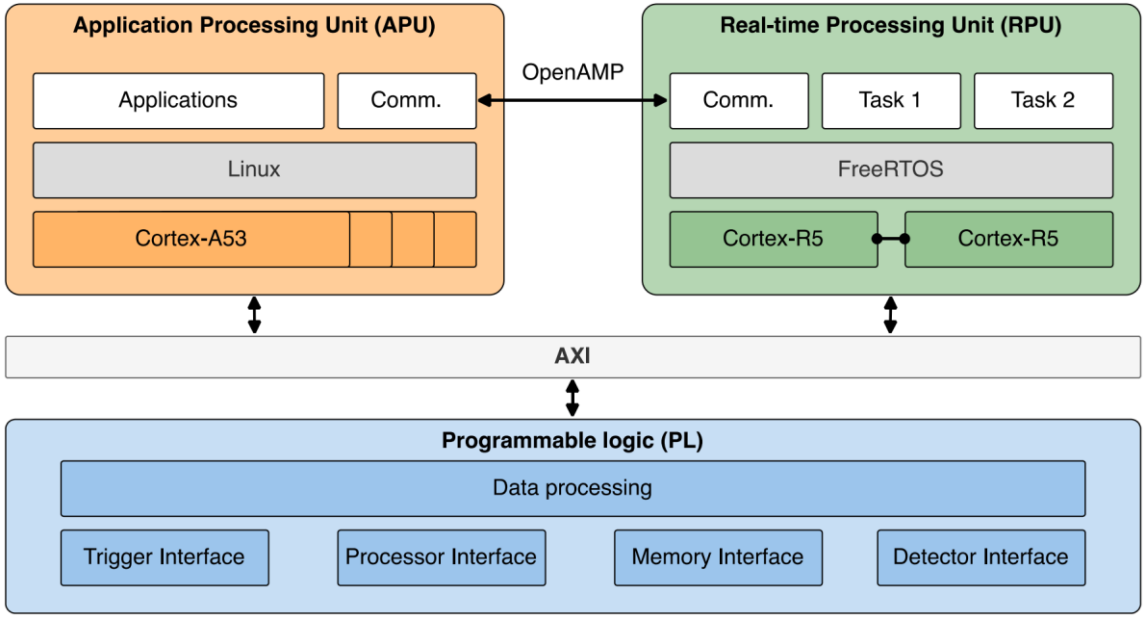
IPbus interface to external computers



REST HTTP interface to external computers



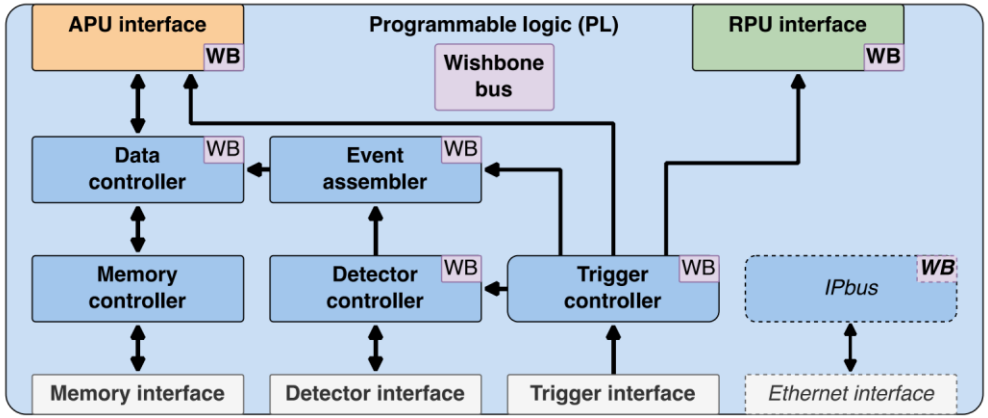
Internal view



Internal view: PL Block

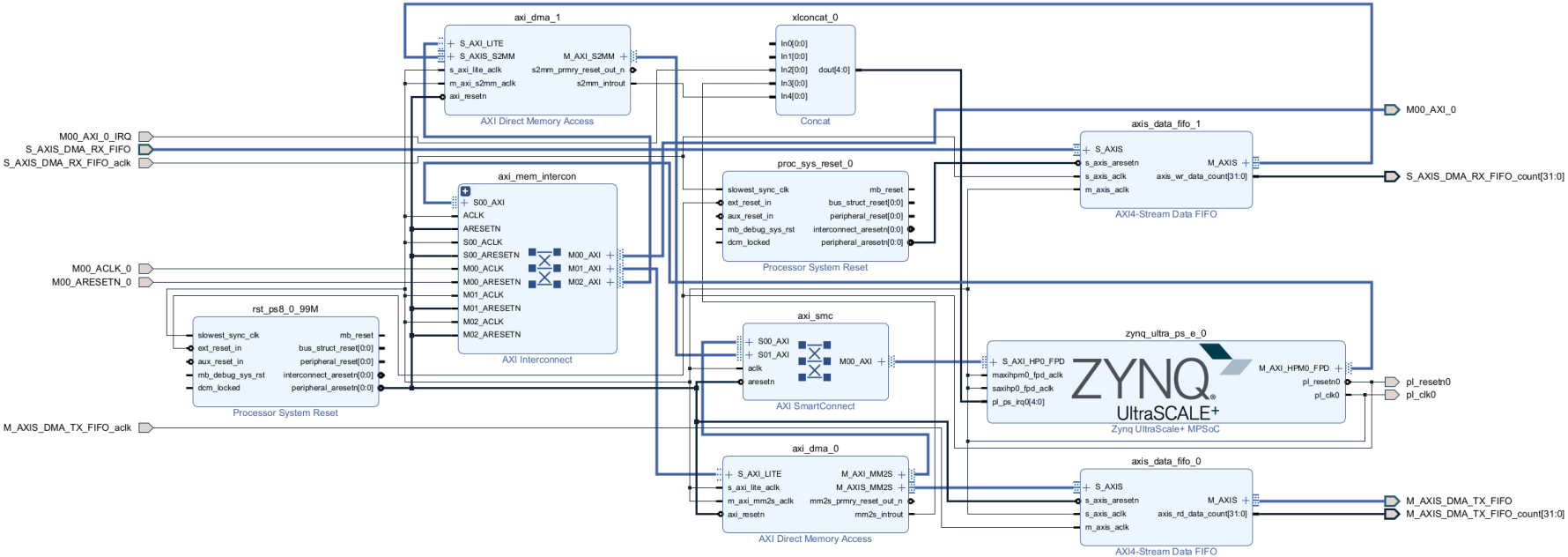
Low-level bit manipulation and data transfer:

- **Detector controller** in change of the synchronization
- **Event assembler** packages the bytes with timing information.
- **Trigger controller:** handles the generation of trigger signals and timestamps.
- **Data controller** handles the events to/from DDR4.
- **Memory controller**: DDR4 Xilinx IP block.

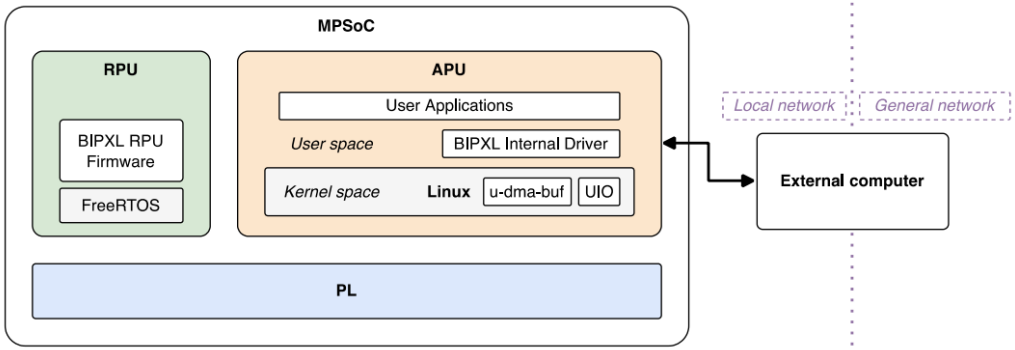


https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/bipxl-gateware

PL-APU Interface: DMA

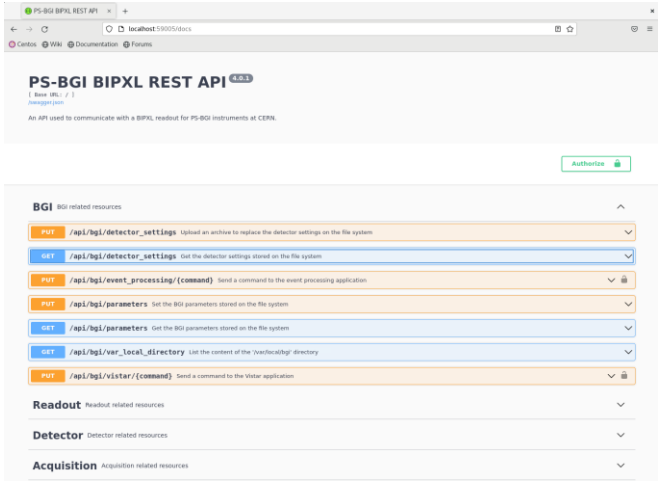


PL-APU Interface



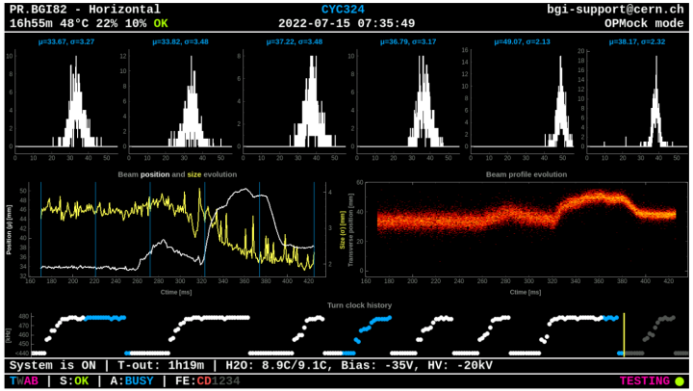
- Concepts:
  - Kernel space
  - User space
- The following drivers are used:
  - **u-dma-buf:** Creates a buffer in kernel space and exposes the physical address to user space via a file (/dev/udmabuf<n>).
  - **UIO:** userspace I/O associated with the DMA to transfer the data from/to the u-dma-buf.
- The configuration of the UIO:
  - Clear IRQs (MM2S_DMASR)
  - Set config (MM2S_DMACR)
  - Set address (MM2S_SA)
  - Set length (MM2S_LENGTH)
- Transfers starts automatically after length is set.

Internal view: User applications

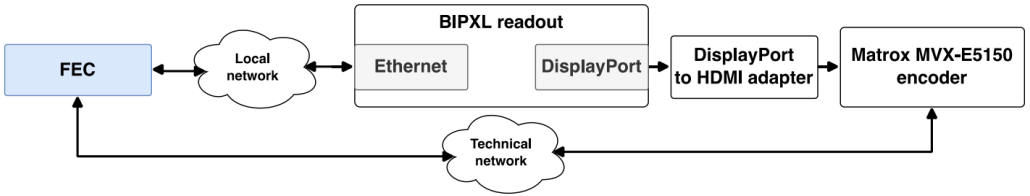


- **BIPXL Internal Driver:** abstraction between user applications above and the kernel drivers below
  - *https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/bipxl-software-internal-driver*
- **REST HTTP Server:** HTTP using Flask and Flask-RESTX frameworks
  - *https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/ps-bgi-bipxl-software-rest-server*

Internal view: User Applications

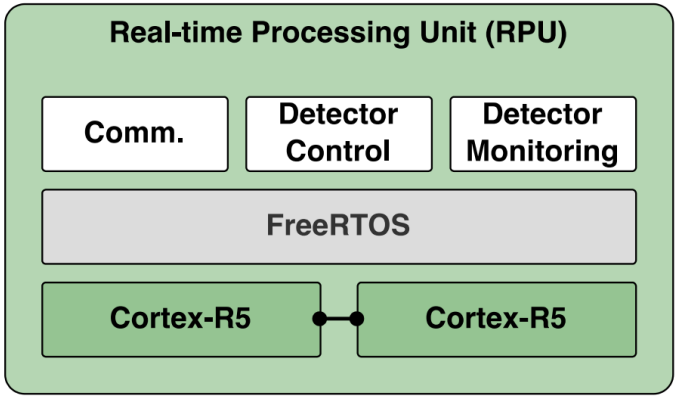


- **BIPXL Event processing:** beam profiles construction to be sent to the BGIPXL FESA class before next beam cycle.
  - *https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/ps-bgi-bipxl-software-event-processing*
- **BIPXL Software Vistar:** live display of the instrument state and beam profile acquisition.
  - *https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/ps-bgi-bipxl-software-vistar*



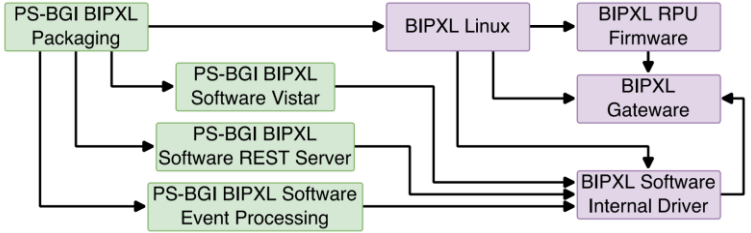
Internal view: RPU

- Detector monitoring and control (real-time critical tasks).
- Lock-step mode using **FreeRTOS**.
- Two main tasks:
  - Detector interface configuration and monitor
  - Detector control and monitoring:
    - General config data
    - Run startup sequence
    - Temperature of the sensor.
- Interface to APU: **OpenAMP** library

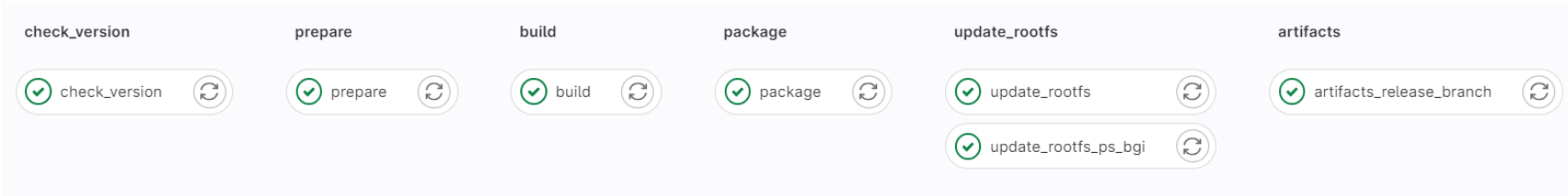


https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/bipxl-rpu-firmware

Packaging



- Packaging repository:
  - Scripts to push all the needed resources.
  - Build Petalinux3 → Gitlab runner → “bipxl-gitlab-runner”
  - Xilinx tools (version 2021.2): kernel, root file system, device tree and firmware specific for MPSoC platform.
  - Artifacts → SD Card



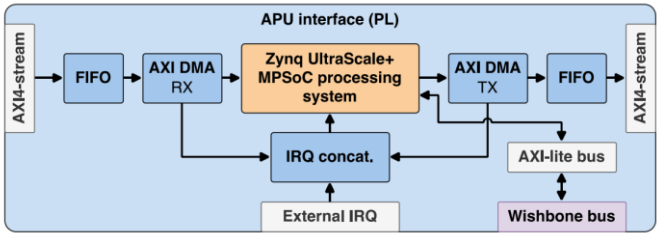
https://gitlab.cern.ch/be-bi-bgi/bipxl-readout/ps-bgi-bipxl-packaging

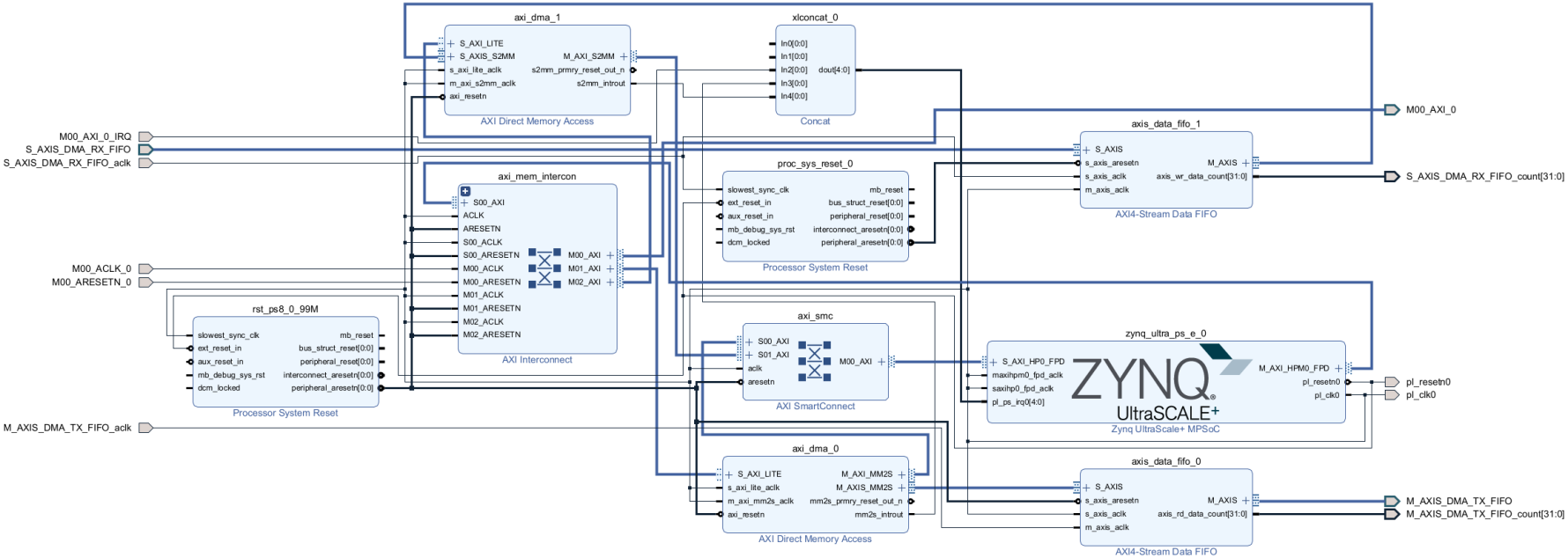
Future plans

- Installation of SPS-BGI → YETS 2023
- Instrument + readout development for LHC-BGI:
  - Timepix4:
    - 163.84 Gbps (16 Output x 10.24 Gbps)
    - LpGBT: 2.56 Gbps in downlink and 5.12/10.24 Gbps in uplink.
- SoM:
  - 4 GTH transceiver pairs, plus 13 GTH receivers.
  - SD-Card
  - Ethernet RJ45
  - Serial port
  - >4Gb PS Side DDR4
  - >1GB PL Side DDR4
  - Video port

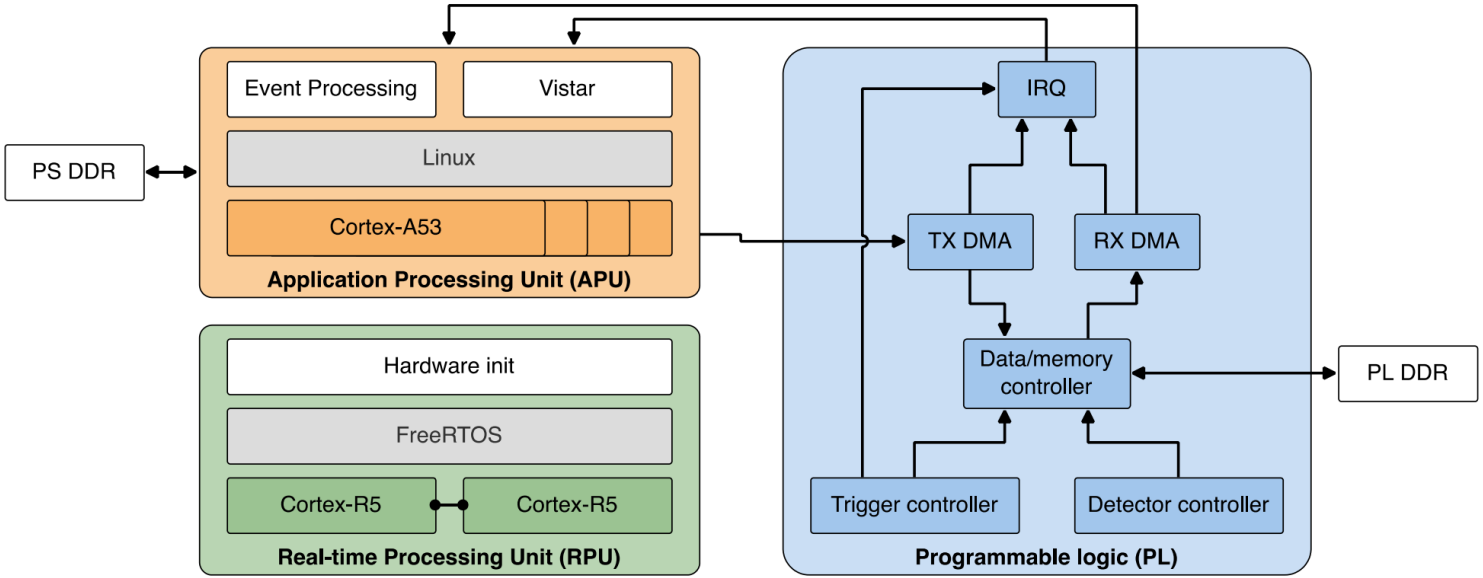
www.cern.ch

DMA


APU interface (PL)
AXI4-stream
FIFO
AXI DMA RX
Zynq UltraScale+ MPSoC processing system
AXI DMA TX
FIFO
AXI4-stream
IRQ concat.
AXI-lite bus
External IRQ
Wishbone bus


axi_dma_1
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_S2MM
s2mm_prmry_reset_out_n
s2mm_introut
AXI Direct Memory Access
xlconcat_0
In0[0:0]
In1[0:0]
In2[0:0]
In3[0:0]
In4[0:0]
dout[4:0]
Concat
M00_AXI_0_IRQ
S_AXIS_DMA_RX_FIFO
S_AXIS_DMA_RX_FIFO_aclk
M00_AXI_0
axis_data_fifo_1
S_AXIS
s_axis_aresetn
s_axis_aclk
m_axis_aclk
M_AXIS
axis_wr_data_count[31:0]
S_AXIS_DMA_RX_FIFO_count[31:0]
AXI4-Stream Data FIFO
axi_mem_intercon
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M00_AXI
M01_AXI
M02_AXI
AXI Interconnect
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
M00_ACLK_0
M00_ARESETN_0
rst_ps8_0_99M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_smc
S00_AXI
S01_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect
zynq_ultra_ps_e_0
S_AXI_HP0_FPD
maxihpm0_fpd_aclk
saxihp0_fpd_aclk
pl_ps_irq0[4:0]
M_AXI_HPM0_FPD
pl_resetn0
pl_clk0
ZYNQ
UltraSCALE+
Zynq UltraScale+ MPSoC
pl_resetn0
pl_clk0
M_AXIS_DMA_TX_FIFO_aclk
axi_dma_0
S_AXI_LITE
s_axi_lite_aclk
m_axi_mm2s_aclk
axi_resetn
M_AXI_MM2S
M_AXIS_MM2S
mm2s_prmry_reset_out_n
mm2s_introut
AXI Direct Memory Access
axis_data_fifo_0
S_AXIS
s_axis_aresetn
s_axis_aclk
m_axis_aclk
M_AXIS
axis_rd_data_count[31:0]
M_AXIS_DMA_TX_FIFO
M_AXIS_DMA_TX_FIFO_count[31:0]
AXI4-Stream Data FIFO

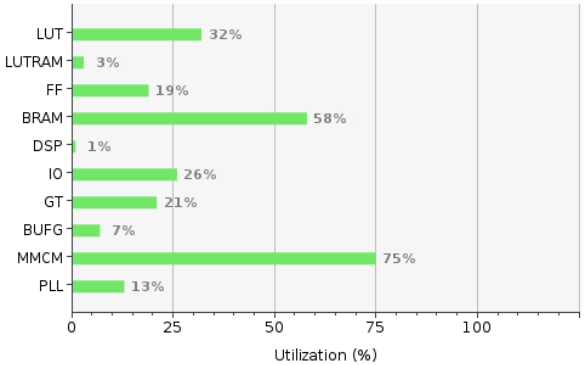
Internal view



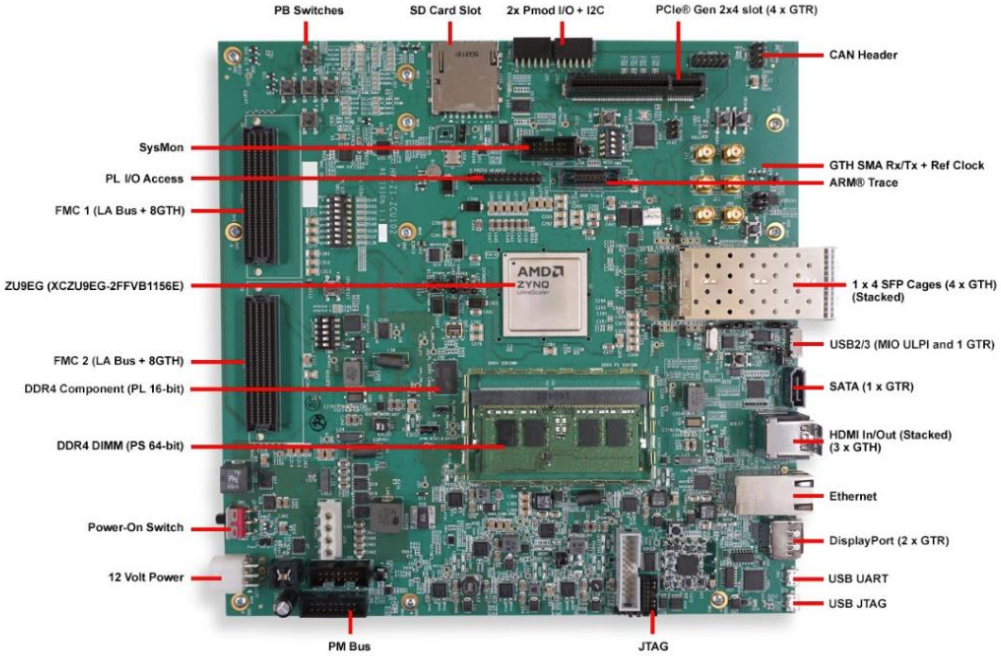
FPGA Utilization

Summary

Resource	Utilization	Available	Utilization %
LUT	87820	274080	32.04
LUTRAM	4816	144000	3.34
FF	103209	548160	18.83
BRAM	525.50	912	57.62
DSP	3	2520	0.12
IO	85	328	25.91
GT	5	24	20.83
BUFG	30	404	7.43
MMCM	3	4	75.00
PLL	1	8	12.50

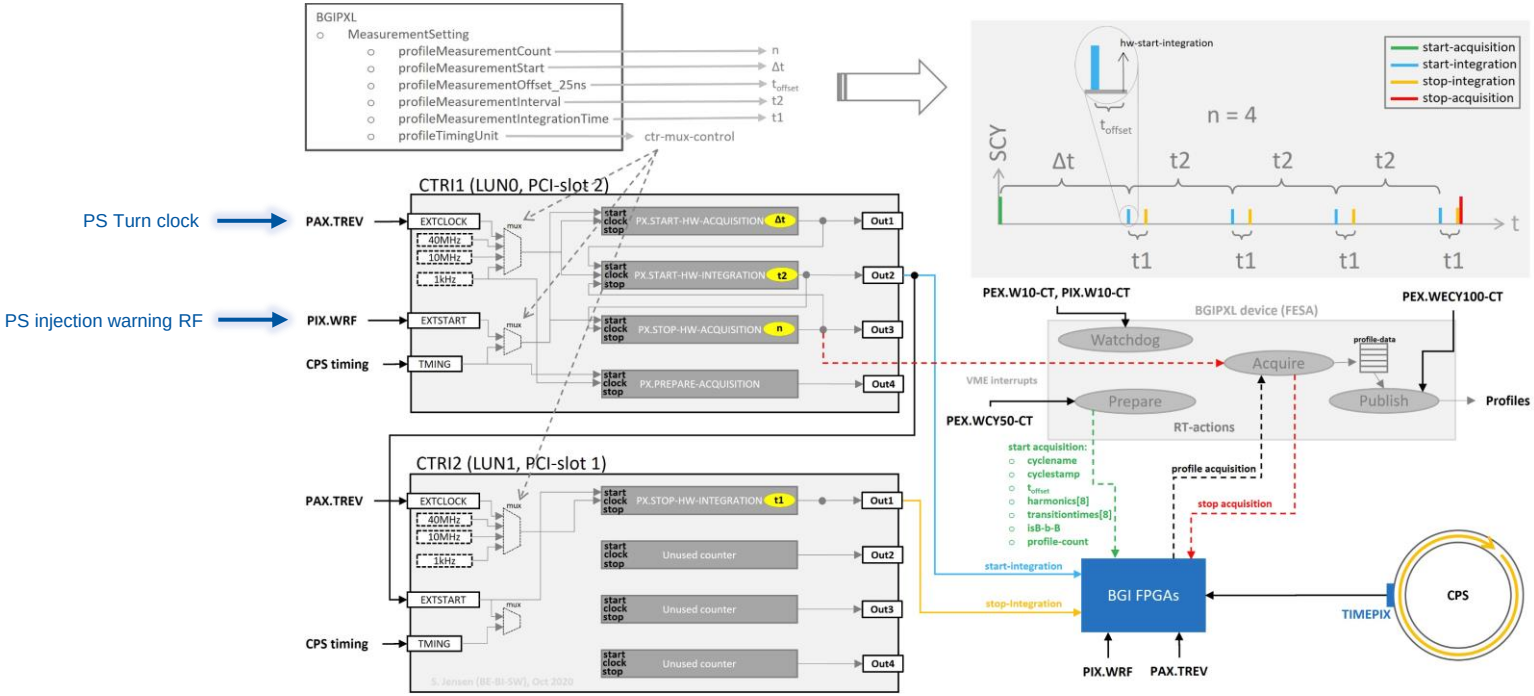


ZCU102 Evaluation Board



https://www.xilinx.com/products/boards-and-kits/ek-u1-zcu102-g.html

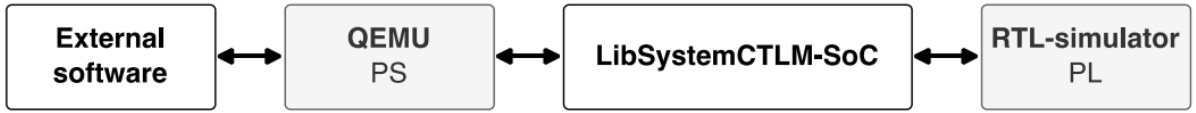
BGI Timing Setup



Steen Jensen's diagram

Co-simulation of gateware and software

- Run Petalinux with the installed software → QEMU emulator
  - No emulation of the PL or the RPU
  - To make this possible → co-simulation of the RTL + QEMU
    - LibSystemCTLM-SoC:
      - https://github.com/Xilinx/libsystemctlm-soc
      - https://indico.cern.ch/event/1090205/#7-hardwaresoftware-co-simulati



Timepix3 → Timepix4

			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	**33%**
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	**6x**
TOT energy resolution			< 2KeV	< **1Kev**	**2x**
Time resolution			1.56ns	**195.3125ps**	**8x**
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	≤163.84 Gbps (16x @10.24 Gbps)	**32x**
Target global minimum threshold			<500 e^-	<500 e^-	

https://indico.cern.ch/event/1121147/