

# From SoC to SoM: AMD and AVNET Solutions

CERN – 3<sup>rd</sup> SoC Workshop 2023

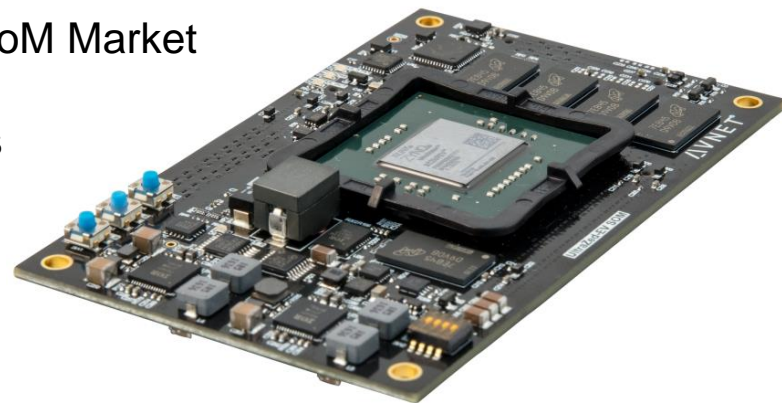
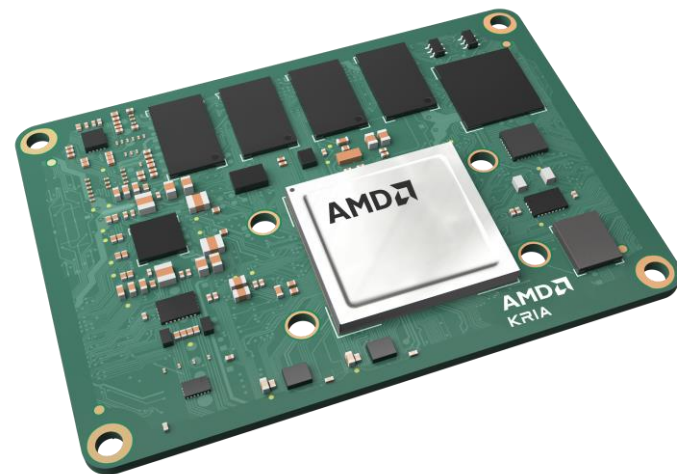
Gregory Donzel - FPGA & SoC FAE – AVNET SILICA

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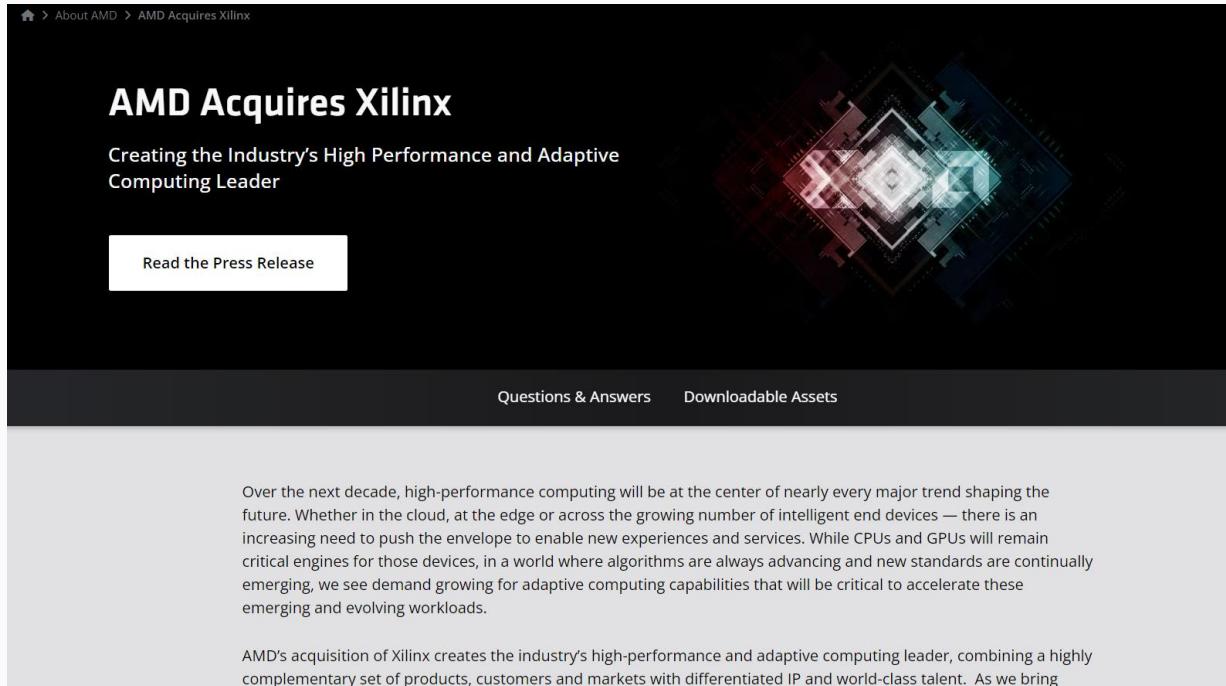


# Agenda

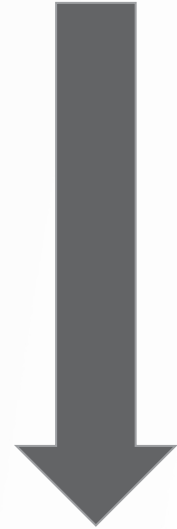
- **AMD: Versal Adaptive SoCs and Kria SoMs**
  - Versal Adaptive SoCs: Update and Roadmap
  - Kria SoMs: What's new?
- **AVNET : AMD Partner and SoM Manufacturer**
  - AVNET EMBEDDED : World leader on the SoM Market
  - AVNET SoMs :
    - Zynq US+ MPSoC/RFSoc based SoMs
    - Road to Versal...
- **Q&A**



# What happened since June 2021?...



The screenshot shows the top portion of a web page for the AMD acquisition of Xilinx. At the top left, there is a breadcrumb trail: "About AMD > AMD Acquires Xilinx". The main heading is "AMD Acquires Xilinx" in a large, bold, white font. Below it is the sub-heading "Creating the Industry's High Performance and Adaptive Computing Leader". A white button with the text "Read the Press Release" is positioned to the left. To the right of the text is a large, abstract graphic of a diamond-shaped circuit board with glowing red and blue elements. At the bottom of the page, there are two links: "Questions & Answers" and "Downloadable Assets". Below the page content, there is a paragraph of text: "Over the next decade, high-performance computing will be at the center of nearly every major trend shaping the future. Whether in the cloud, at the edge or across the growing number of intelligent end devices — there is an increasing need to push the envelope to enable new experiences and services. While CPUs and GPUs will remain critical engines for those devices, in a world where algorithms are always advancing and new standards are continually emerging, we see demand growing for adaptive computing capabilities that will be critical to accelerate these emerging and evolving workloads." Below this paragraph is another line of text: "AMD's acquisition of Xilinx creates the industry's high-performance and adaptive computing leader, combining a highly complementary set of products, customers and markets with differentiated IP and world-class talent. As we bring



## What Changes?

- XILINX = AECG (Adaptive and Embedded Computing Group)
- Committed to XILINX roadmap: More products in the Cost Optimized Portfolio



# Comprehensive Product Portfolio

	28nm	20nm	16nm	7nm
Cloud Applications				<b>AMD</b> <b>VERSAL</b> AI Core
RF Applications			<b>AMD</b> <b>ZYNQ</b> RFSoc	<b>AMD</b> <b>VERSAL</b> AI RF
Edge Applications	<b>AMD</b> <b>ZYNQ</b> 7000		<b>AMD</b> <b>ZYNQ</b> MPSoc	<b>AMD</b> <b>VERSAL</b> AI Edge
Broad Applications	<b>AMD</b> <b>VIRTEX</b> <sup>7</sup>  <b>AMD</b> <b>KINTEX</b> <sup>7</sup>  <b>AMD</b> <b>ARTIX</b> <sup>7</sup>  <b>AMD</b> <b>SPARTAN</b> <sup>7</sup>	<b>AMD</b> <b>VIRTEX</b> UltraScale  <b>AMD</b> <b>KINTEX</b> UltraScale	<b>AMD</b> <b>VIRTEX</b> UltraScale+ HBM  <b>AMD</b> <b>VIRTEX</b> UltraScale+ SSG  <b>AMD</b> <b>VIRTEX</b> UltraScale+  <b>AMD</b> <b>KINTEX</b> UltraScale+  <b>AMD</b> <b>ARTIX</b> UltraScale+  <b>AMD</b> <b>SPARTAN</b> UltraScale+	<b>AMD</b> <b>VERSAL</b> HBM  <b>AMD</b> <b>VERSAL</b> Premium  <b>AMD</b> <b>VERSAL</b> Prime

# AMD VERSAL

Adaptive SoC

Heterogeneous Acceleration

For Any Application

For Any Developer



7nm  
FinFET



# Versal™ Adaptive SoC Technology Tour



Scalar Processing Engines



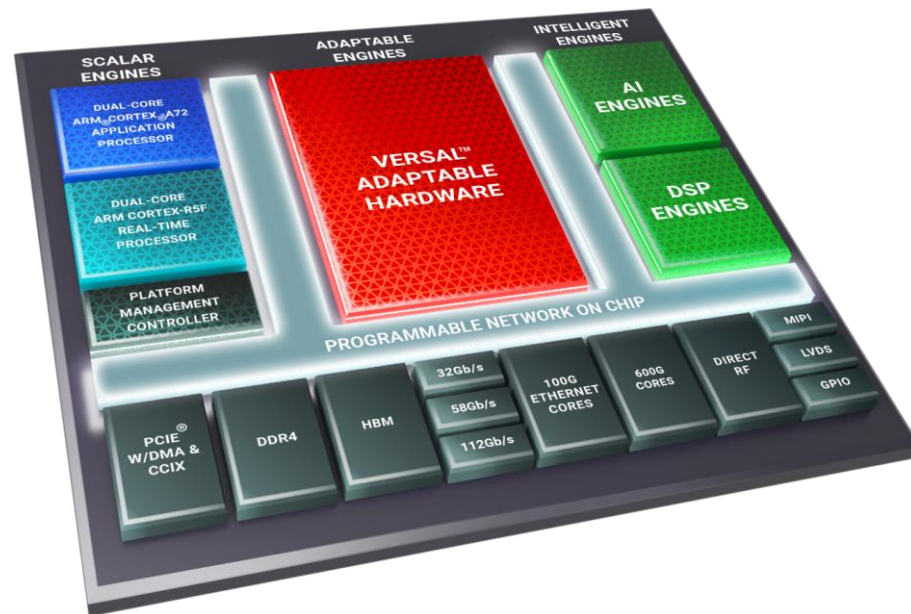
Adaptable Hardware Engines



Intelligent Engines  
SW Programmable, HW Adaptable



Breakout Integration of Advanced  
Protocol Engines





# Versal™ Architecture Overview



## Adaptable Engines

- Re-architected for faster timing closure
- Tune for power vs. performance
- Adaptable to any workload



## Intelligent Engines (DSP)

- AI Compute
- Diverse DSP Workloads



## Scalar Engines

- Platform Control
- Embedded Edge Compute



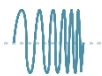
## PCIe® Gen5 & CCIX

- 2X PCIe & DMA bandwidth
- Cache-coherency



## DDR4 Memory

- 3200-DDR4, 4266-LPDDR4
- 2X bandwidth/pin



## Transceiver Leadership

- Broad range, 1G → 112G
- 58G in mainstream devices



## HBM

- 820GB/s Bandwidth
- 32GB Capacity



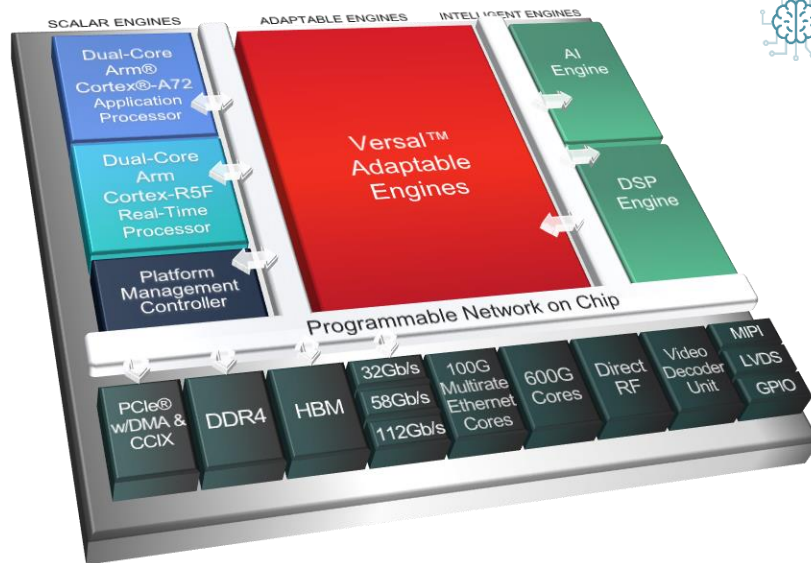
## Video Decoder Unit

- H.264/H.265 decoding
- Up to 4x 4K UHD (or 32x 1080p)



## RF

- Direct-RFADC and RF-DAC
- SD-FEC



## Programmable NoC

- Guaranteed Bandwidth
- Enables SW Programmability



## Protocol Engines

- 400G/600G cores
- Power-Optimized



## Programmable I/O

- Any interface or sensor
- Includes 3.2Gb/s MIPI

# Versal™ Roadmap

Subject to Change



**AI Core**  
AI Engine  
DSP, ML Inference



**Prime**  
Broadest Application



**Premium**  
112G Serdes  
600G Cores



**HBM**  
Memory  
Integration



**AI Edge**  
Lowest Power AI



**AI RF**  
AI DSP w/  
Integrated RF



# Versal™ Prime Series – Resources

	VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902	
Adaptable Engines	System Logic Cells (K)	329	693	1,238	981	1,968	1,139	1,575	1,969	2,233
	LUTs	150,272	316,928	565,760	448,512	899,840	520,704	719,872	900,224	1,020,928
	NoC Master / NoC Slave Ports	5	9	18	21	28	21	30	28	42
	Distributed RAM (Mb)	5	10	17	14	27	16	22	27	31
Memory	Total Block RAM (Mb)	5	18	40	34	34	21	49	47	70
	Total UltraRAM (Mb)	44	50	80	130	130	74	127	190	181
	Total PL Memory (Mb)	54	78	137	178	191	111	198	264	282
	DDR Memory Controllers	1	2	4	3	4	3	3	4	3
	DDR Bus Widths	64	128	256	192	256	192	192	256	192
Intelligent Engines	DSP Engines	464	832	1,696	1,312	1,968	1,312	1,904	3,984	2,672
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC								
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC								
	Memory	256KB On-Chip Memory w/ECC								
	Connectivity	Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)								
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	24	24	44	44	0	0	0	0
	GTYP Transceivers (32.75Gb/s)	8	0	0	0	0	32 <sup>(1)</sup>	8	28 <sup>(1)</sup>	8
	GTM Transceivers (56Gb/s)	0	0	0	0	0	0	40	16	40
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	2 x Gen5x8, CCIX	-	2 x Gen5x8, CCIX	-
	PCI Express®	1 x Gen4x8	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	1	2	2	4	4	2	6	2	6

Versal Prime Series

## Notes:

1. 16 GTYP transceivers are dedicated to the CPM for PCI Express use.

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: [www.xilinx.com](http://www.xilinx.com).

# Versal™ AI Core Series – Resources

	VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802	
Intelligent Engines	AI Engines Tiles	128	198	304	300	400	0	0
	AI Engine-ML Tiles	0	0	0	0	0	152	304
	AI Engine Data Memory (Mb)	32	50	76	75	100	76	152
	AIE-ML Shared Memory (Mb)	0	0	0	0	0	304	304
	DSP Engines	928	1,032	1,312	1,600	1,968	984	1,312
Adaptable Engines	System Logic Cells (K)	540	815	981	1,586	1,968	820	1,139
	LUTs	246,784	372,352	448,512	725,000	899,840	375,000	520,704
	NoC Master / NoC Slave Ports	10	21	21	28	28	21	21
	Distributed RAM (Mb)	8	11	14	22	27	11	16
Memory	Total Block RAM (Mb)	16	30	34	28	34	17	21
	UltraRAM (Mb)	59	110	130	91	130	63	74
	Accelerator RAM (Mb)	32	0	0	0	0	0	0
	Total PL Memory (Mb)	115	151	178	141	191	91	111
	DDR Memory Controllers	2	3	3	4	4	3	3
DDR Bus Width	128	192	192	256	256	192	192	
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
Serial Transceivers	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
	GTY Transceivers (32.75Gb/s)	0	32	0	44	44	0	0
	GTY Transceivers (32.75Gb/s)	8	0	44	0	0	32	32
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	–	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express®	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen5x4	4 x Gen5x4
	100G Multirate Ethernet MAC	1	3	4	4	4	2	2
Video Decoder Engines (VDEs)	–	–	–	–	–	2	4	
Platform Management Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug							

# Versal™ Premium Series – Resources

		VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802
Adaptable Engines	System Logic Cells (K)	833	1,186	1,575	1,969	2,233	3,763	3,738	3,837	5,558	7,352	7,326
	LUTs	380,800	542,080	719,872	900,224	1,020,928	1,720,448	1,708,672	1,753,984	2,540,672	3,360,896	3,349,120
	NoC Master / NoC Slave Ports	22	22	30	28	42	52	52	52	76	100	100
	Distributed RAM (Mb)	12	17	22	27	31	53	52	54	78	103	102
Memory	Total Block RAM (Mb)	19	26	49	47	70	89	89	89	132	174	174
	UltraRAM (Mb)	97	138	127	190	181	366	366	366	541	717	717
	Total PL Memory (Mb)	128	181	198	264	282	508	507	509	751	994	994
	DDR Memory Controllers	2	2	3	4	3	4	4	4	4	4	4
Intelligent Engines	DDR Bus Width	128	128	192	256	192	256	256	256	256	256	256
	DSP Engines	1,140	1,572	1,904	3,984	2,672	7,440	7,392	7,392	10,896	14,352	14,304
	AI Engines Tiles	-	-	-	-	-	-	472	-	-	-	472
	AI Engine Data Memory (Mb)	-	-	-	-	-	-	118	-	-	-	118
Scalar Engines	APU	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC										
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC										
	Memory	256KB On-Chip Memory w/ECC										
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)										
Serial Transceivers	GTY Transceivers (32.75Gb/s)	20	20	-	-	-	-	-	-	-	-	-
	GTYP Transceivers (32.75Gb/s)	-	-	8	28 <sup>(1)</sup>	8	28 <sup>(1)</sup>	28 <sup>(1)</sup>	68 <sup>(1)</sup>	28 <sup>(1)</sup>	28 <sup>(1)</sup>	28 <sup>(1)</sup>
	GTM Transceivers <sup>(2)</sup> (58G (112G))	24 (12)	48 (24)	64 (32)	20 (10)	96 (64)	60 (30)	60 (30)	20 (10)	100 (50)	140 (70)	140 (70)
Integrated Protocol IP	PCIe® w/DMA & CCIX (CPM4)	2 x Gen4x4	2 x Gen4x4	-	-	-	-	-	-	-	-	-
	PCIe w/DMA & CCIX (CPM5)	-	-	-	2 x Gen5x8	-	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8
	PCI Express	1 x Gen4x8	1 x Gen4x8	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	3	5	6	2	6	4	4	4	6	8	8
	600G Ethernet MAC	2	3	7	1	11	3	3	1	5	7	7
	600G Interlaken	1	2	0	0	0	1	1	0	2	3	3
Ordering Information	400G High-Speed Crypto Engine	1	1	3	1	4	2	2	2	3	4	4
	Extended <sup>(3)</sup>	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE										
	Industrial <sup>(3)</sup>	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2LSI										

# Versal™ HBM Series – Resources

			VH1522	VH1542	VH1582	VH1742	VH1782
Adaptable Engines	System Logic Cells (K)		3,837	3,837	3,837	5,631	5,631
	LUTs		1,753,984	1,753,984	1,753,984	2,574,208	2,574,208
	NoC Master / NoC Slave Ports		52	52	52	76	76
	Distributed RAM (Mb)		54	54	54	79	79
Memory	Total Block RAM (Mb)		89	89	89	132	132
	UltraRAM (Mb)		366	366	366	541	541
	Total PL Memory (Mb)		509	509	509	752	752
	HBM DRAM (GB)		8	16	32	16	32
	DDR Memory Controllers		4	4	4	4	4
	DDR Bus Width		256	256	256	256	256
Intelligent Engines	DSP Engines		7,392	7,392	7,392	10,848	10,848
Scalar Engines	APU Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	RPU Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory 256KB On-Chip Memory w/ECC						
	Connectivity Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTYP <sup>(1)</sup> 32G		68	68	68	68	68
	GTM <sup>(2)</sup> 56G (112G)		20 (10)	20 (10)	20 (10)	60 (30)	60 (30)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM5)		2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express (PLPCIe5)		8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4
	100G Multirate Ethernet MAC		4	4	4	6	6
	600G Ethernet MAC		1	1	1	3	3
	600G Interlaken		0	0	0	1	1
400G High-Speed Crypto Engines		2	2	2	3	3	
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTYP, GTM (112G)				
VSVA3697	57.5x57.5	0.92	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)		
LSVA4737	70x70	1.0		132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 60 (30)	132, 570 0, 78 68, 60 (30)

## Notes:

1. GTY transceivers operate at data rates up to 32.75Gb/s
2. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together

# Versal™ AI Edge Series – Resources

	VE2002	VE2102	VE2202	VE2302	VE2602	VE1752	VE2802
Intelligent Engines	AI Engine-ML Tiles	8	12	24	34	152	304
	AI Engine Tiles	0	0	0	0	304	0
	AIE/AIE-ML Data Memory (Mb)	4	6	12	17	76	152
	AIE-ML Shared Memory (Mb)	48	48	68	68	304	304
	DSP Engines	90	176	324	464	984	1,312
Adaptable Engines	System Logic Cells	43,750	80,080	229,688	328,720	820,313	1,139,040
	LUTs	20,000	36,608	105,000	150,272	375,000	520,704
	NoC Master / NoC Slave Ports	2	2	5	5	21	21
	Distributed RAM (Mb)	0.6	1.1	3.2	4.6	11.4	15.9
Memory	Total Block RAM (Mb)	0.8	1.7	3.8	5.4	16.7	21.1
	UltraRAM (Mb)	6.8	13.2	30.4	43.6	63.0	74.3
	Accelerator RAM (Mb)	32	32	32	32	0	0
	Total PL Memory (Mb)	40.2	48	69.4	85.6	91.1	111.3
	DDR Memory Controllers	1	1	1	1	3	3
	DDR Bus Width	64	64	64	64	192	192
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC					
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC					
	Memory	256KB On-Chip Memory w/ECC					
Serial Transceivers	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)					
	GTY Transceivers (32.75Gb/s)	0	0	0	0	44	0
Integrated Protocol IP	GTYP Transceivers (32.75Gb/s)	0	0	8	8	32	32
	CCIX & PCIe® w/DMA (CPM)	-	-	-	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®	-	-	1 x Gen4x8	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8
Video Decoder Engines (VDEs)	40G Multirate Ethernet MAC	0	0	1	1	2	2
	Video Decoder Engines (VDEs)	-	-	-	-	2	4
	Platform Mgmt Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug					

# Granular Control of Power vs. Performance

## Voltage Scaling with Speed Grade Options

FABRIC	$V_{LOW}$		$V_{MID}$		$V_{HIGH}$	
	$F_{MAX}$	Power	$F_{MAX}$	Power	$F_{MAX}$	Power
-1 Speed Grade	1x	1x	1.2x	1.3x	1.2x	1.3x
-2 Speed Grade	1.1x	1x	1.3x	1.3x	1.45x	1.6x
-3 Speed Grade	-	-	-	-	1.45x	1.6x

SerDes	$V_{LOW}$	$V_{MID}$	$V_{HIGH}$
-1 Speed Grade	26G	27G	27G
-2 Speed Grade	28G	28G	28G
-3 Speed Grade	-	-	32G

Processor (A72)	$V_{LOW}$	$V_{MID}$	$V_{HIGH}$
-1 Speed Grade	1GHz / 1.45GHz*	1.3GHz	1.45GHz
-2 Speed Grade	1.15GHz	1.35GHz	1.5GHz
-3 Speed Grade	-	-	1.7GHz

$$V_{HIGH} = .88V$$

$$V_{MID} = .80V$$

$$V_{LOW} = .70V$$

\*When  $V_{CCINT\_PS} = V_{HIGH} (.88V)$



# Getting Started with Versal Adaptive SoC Boards & Kits

## Versal™ Prime Series



**VMK180**  
General Purpose Development Kit  
(VM1802 Silicon)

*Available Now*

## Versal™ AI Core Series



**VCK190**  
AI Engine Development Kit  
(VC1902 Silicon)

*Available Now*

## Versal™ Premium Series



**VPK120**  
Essential  
Hard IP Development Kit  
(VP1202 Silicon)

*Available Now*

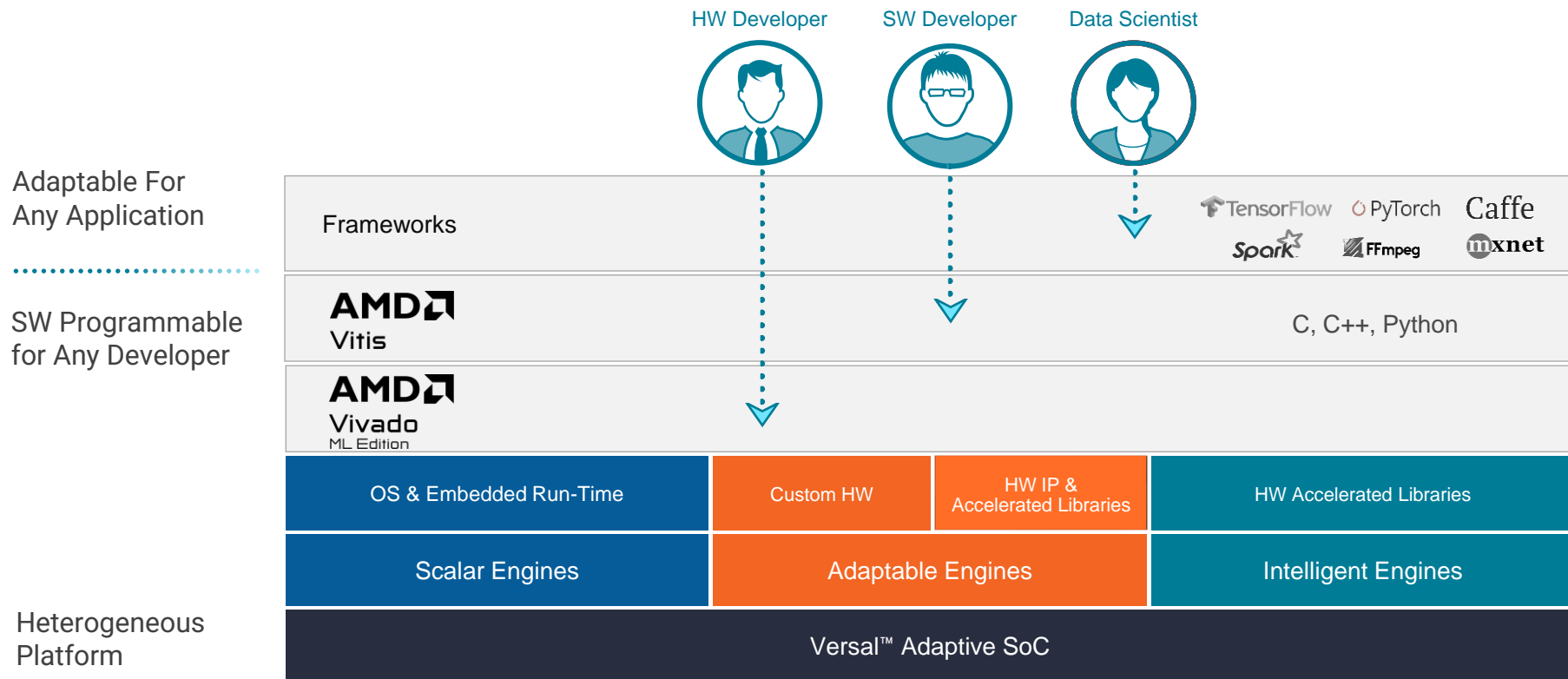
## Versal™ Premium Series



**VPK180**  
Comprehensive  
Hard IP Development Kit  
(VP1802 Silicon)

*Early Access Available Now*

# Versal™ Development Experience for All Developers



# Learning Center to Get You Started



## On-Demand Training

Recorded lectures and forums w/ experts



## Virtual Classroom

Live online training, interact w/instructors



## Live Classroom

In-person, immersive classroom environment

## Recommended Courses

[Getting Started with the Versal™ Adaptive SoC Platform](#)

[Designing with the Versal Adaptive SoC : Architecture and Methodology](#)

[Designing with the Versal Adaptive SoC : Programmable Network on Chip](#)

[Designing with the Versal Adaptive SoC : Power and Board Design](#)

[Designing with Versal AI Engine 1: Architecture and Design Flow](#)

[Designing with Versal AI Engine 2: Graph Programming with AI Engine Kernels](#)

[Designing with Versal AI Engine 3: Kernel Programming and Optimization](#)

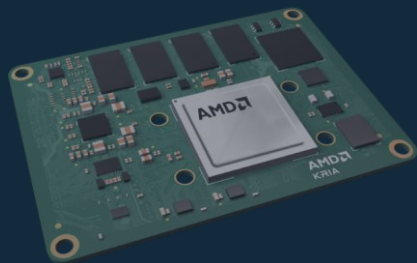
Visit [www.xilinx.com/training.html](http://www.xilinx.com/training.html)

# AMD Kria SOMs: What's new?



**AMD**   
together we advance\_

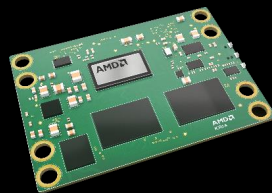
# Expanding Our Portfolio of Adaptive System-on-Modules



AVAILABLE NOW

## Kria™ K26 SOM

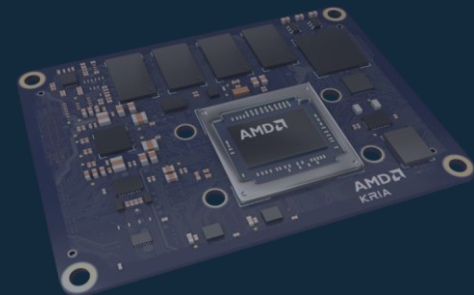
For vision AI and robotics in smart cities and smart factories



NEW: AVAILABLE NOW

## Kria K24 SOM

For electric drives and other digital signal processing-intensive applications



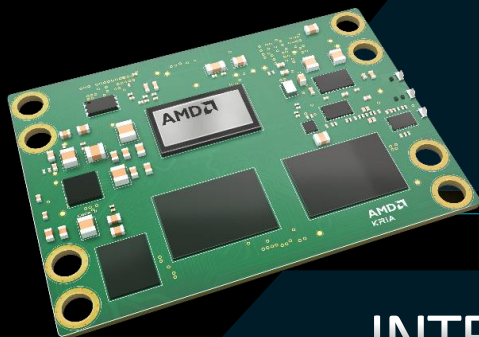
ROADMAP

## High AI Compute

High real-time compute/watt for edge AI applications

# Kria K24 SOM Overview

Based on Zynq™ UltraScale+™ MPSoC Technology



## ADAPTIVE SOC (Custom Device for Kria™ K24 SOM)

### Arm® Core

A53 Quad core  
R5F Dual core

### Ubuntu OS

Supports latest 22.04  
version

### 154K

System logic cells for  
custom acceleration

### INT8

B2304 DPU support

## INTERFACES

### 132 I/Os

Flexible for connecting multiple  
motors, sensors, and connectors

### Industrial Ethernet

4x 1G Ethernet, support  
for converged traffic<sup>1</sup>

### 4x USB

Mix of USB  
3.0 and 2.0

### 2 GB

32-bit LPDDR4  
memory (w/ ECC config<sup>2</sup>)

### Security Features

HW Root of Trust  
along with TPM 2.0<sup>3</sup>

1: TSN is enabled only through programmable logic (PL)-based Ethernet interfaces

2: ECC support only available on industrial grade SKU of K24 SOM, 32-bit LPDDR4 @ 1066 Mbps

3: HW-based security for remote attestation, measured boot, cryptographic functions



# Ruggedization for Extreme Operating Conditions Including Industrial Applications

- Built for indoor/outdoor and low/high temperature ranges
- Meets country-specific compliance and certification requirements
- Ruggedized connectors for shock resistance



## Meeting Reliability Requirements

Kria™ K24 SOM		
	C-Grade	I-Grade <sup>1</sup>
Shock	40G, 11ms	40G, 11ms
Vibration	1.9g RMS	5g RMS
Temp Range at Module TTP	0°C to 85°C	-40°C to 100°C
Humidity	85°C / 80% RH	85°C / 80% RH
Operating Life <sup>2</sup>	5 years	10 years
Availability <sup>3</sup>	10 years	10 years
Warranty (Production SOM) <sup>4</sup>	2 years	3 years

1: I-grade specs are tentative and subject to change

2: Operating Life – Suitable for deployment in a production environment

3: Availability – Time period SOM product will be available for purchase

4: Kria KD240 Drives Starter Kits are not intended for production use and come with a 90-day warranty

## Certifications

Country	Certification
US ; Canada	FCC, UL ; IC
EU	CE, ROHS 10
China	CC, ROHS 10
Vietnam	ICT
Japan ; Korea	VCCI ; KCC
Malaysia	ST CoA, SIRIM
Singapore	SPRING Safety
South Africa	SABS EMC, NRSC

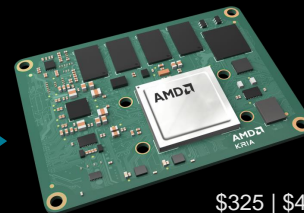
# Comparing Kria™ K24 vs. K26 SOM



\$250 | \$350  
(C-grade | I-grade)

Cost-optimized SOM for lower power, smaller form-factor & cost sensitive industrial applications

CONNECTOR COMPATIBLE



\$325 | \$450  
(C-grade | I-grade)

Mid-range SOM for Vision AI and Robotics applications requiring higher performance per watt



	K24 SOM		K26 SOM
<b>SILICON</b> (SYS LOGIC CELLS)	XCK24 InFO (154K)	▶ SILICON ▶	XCK26 (256K)
<b>SOM I/O ACCESS</b>	1x 240-Pin Connector, 1x 40-Pin Connector	▶ SOM I/O ▶	2x 240-Pin Connectors
<b>FORM FACTOR</b>	60 x 42mm	▶ 46% SMALL ▶	60 x 77mm
<b>MEMORY</b>	2GB LPDDR4 <sup>1</sup> , 32 GB	▶ DDR, eMMC ▶	4GB DDR4, 16 GB
<b>POWER</b> <sup>2</sup>	2.5W	▶ 51% LESS ▶	5.1W
<b>STARTER KITS</b>	KD240 DRIVES	▶ DEV KITS ▶	KV260 VISION AI, KR260 ROBOTICS

<sup>1</sup> ECC support available on K24 SOM I-grade

<sup>2</sup> Measured power while loading application specific bitstream on the SOM-based starter kit

# Comparing Kria™ Starter Kits



\$249

For mainstream vision AI camera & smart city applications



\$349

For high-performance industrial systems including ROS 2-based robotics applications



\$399

For deterministic motor control and DSP applications

## KV260 VISION AI

## KR260 ROBOTICS

## KD240 DRIVES

**NON-PROD SOM**

K26

K26

K24

**SOM I/O ACCESS**

1x 240-Pin Connector

2x 240-Pin Connectors

1x 240-Pin, 1x 40-Pin Connector

**NETWORK**

1x Ethernet

4x Ethernet, SFP+

3x Ethernet

**KEY INTERFACES**

MIPI Vision Sensors

SLVS-EC Vision Sensors

3-phase inverter & quadrature encoder

**EXPANSION**

1x Pmod

4x Pmod

1x Pmod

**ACCESSORIES**

Basic Accessory Pack

Sony IMX547 Camera Kits

Motor Accessory Pack

The text "AVNET : AMD Partner and SoM Manufacturer" is positioned in the bottom left corner. It is written in a white, sans-serif font against a black background. The background of the entire slide is a close-up photograph of a green printed circuit board (PCB) with various electronic components, including a large black chip and several smaller components, with a white connector strip visible in the foreground.

AVNET : AMD Partner and  
SoM Manufacturer

# / AVNET EMBEDDED : World leader on the SoM Market

**MSC HCC-CFLS**      **MSC HSD-ILDL**

**COM+HPC**



First COM-HPC® Client and Server module on the market  
 Leading next generation roadmap.  
 Innovating the future in Edge computing.

**MSC C6B-ALP**      **MSC C6C-ALP**

**COM Express**



Intel 12. Generation (products formally Alder Lake P)  
 "iCore" performance on COM Express® Basic/Compact and COM-HPC.

**MSC Q7-EL**      **MSC C6C-**

**MSC SM2S-EL**      **MSC C10M-EL**

**SMARC module**

**COM Express**



Intel Atom® Processor X Series (products formally Elkhart Lake)  
 Flexible choice of COM module standards with best in class performance and feature sets.

**MSC C6C-RYZ**      **MSC C6C-RYZ**

**COM Express**

**MSC SM2S-ZUSP**

**SMARC module**

**AMD**



AMD Ryzen™ V1000/R1000 and Zynq® UltraScale+ MPSoC  
 Industry leading SMARC® module

**NXP® i.MX 8M Plus and i.MX 93**  
 Scalable Solutions in combination with high computing power and efficient power consumption:  
 i.MX 8M Plus - for Edge based embedded vision and audio AI applications  
 i.MX 93 - performance and energy efficiency for Edge applications

**MSC SM2S-IMX8PLUS**      **MSC SM2S-IMX93**

**SMARC module**

**NXP® SMARC® Portfolio**  
 - Leading SMARC® module vendor with largest NXP® i.MX based portfolio worldwide  
 - Complete portfolio is pin and feature compatible and scalable in price and performance

**SMARC module**

# MSC SM2S-ZUSP

## AMD Zynq UltraScale+ MPSoC

- ZU2CG, ZU3CG, ZU4CG or ZU5CG, ZU2EG, ZU3EG, ZU4EG, ZU5EG, ZU4EV or ZU5EV
- Up to 8GB DDR4 SDRAM, ECC support (optional)
- Up to 2GB DDR4 SDRAM for FPGA (optional)
- Up to 64GB eMMC Flash
- SATA-III interface (6Gbps)
- Up to 2x PCI Express x2 Gen. 3
- Up to 1x USB 3.0/2.0 Host interface
- Up to 3x USB 2.0 Host interface/1x USB 2.0 Host/Device interface
- Gigabit Ethernet (single or dual)
- Wireless Module (optional)
- 1x MMC/SD/SDIO interface
- 2x CAN interface
- UART, SPI, I2C
- Rich FPGA I/O
- SMARC 2.0 Compliant
- Estimated Lifetime 2030



SMARC Module  
Zynq UltraScale+ MPSoC

AVNET<sup>™</sup> EMBEDDED / MSC



# SOMs – Zynq UltraScale+

/ULTRAZED-EG



- CG and EG families
- 103-154K LCs
- 5.3-7.6Mb Block RAM
- 240-360 DSP Slices
- Pin compatible family
- Commercial and industrial temps

/ULTRAZED-EV



- EG and EV families
- 192-504K LCs
- 4.5-11Mb Block RAM
- 728-1728 DSP Slices
- Pin compatible family
- Commercial and industrial temps

ZU2CG	◆
ZU3CG	◆
ZU2EG	◆
ZU3EG	◆
ZU4EG	◆
ZU5EG	◆
ZU7EG	◆
ZU4EV	◆
ZU5EV	◆
ZU7EV	◆

# / XRF16

Available Now

5 GHz Bandwidth  
16x 2.22 GSPS ADCs  
16x 6.554 GSPS DACs  
Xilinx RFSoc Gen2 ZU39DR

# / XRF8

Available Now

6 GHz Bandwidth  
8x 5 GSPS ADCs  
8x 10 GSPS DACs  
Xilinx RFSoc Gen3 ZU47DR

## Power Management

- Single 5.5V to 16V input
- Temp and voltage monitoring



## High Bandwidth Data Interface

- 1GbE, USB2.0 (PHYs on-board)
- 4 GTR for PCIe Gen2, SATA3, USB3
- 16 GTY for PCIe Gen3, 100 GbE, Aurora
- Up to 36 differential GPIO

## RF Clocking

- On-board ultra-low jitter RF PLLs
- External or 10 MHz TCXO reference

## Memory

- 4GB PL-DDR4 64-bit
- 4GB PS-DDR4 64-bit
- 32GB eMMC
- 128 MB QSPI Flash

# /XRF

## CarrierCard

### RF Interface

- 16 ADC
- 16 DAC
- Single-ended

### Filter Options

- FV1206 LPF or BPF
- Optional pi-pad filter

### 5.5V to 16V Power

- 6-pin custom rugged
- 2.5mm laptop supply

### System Peripherals

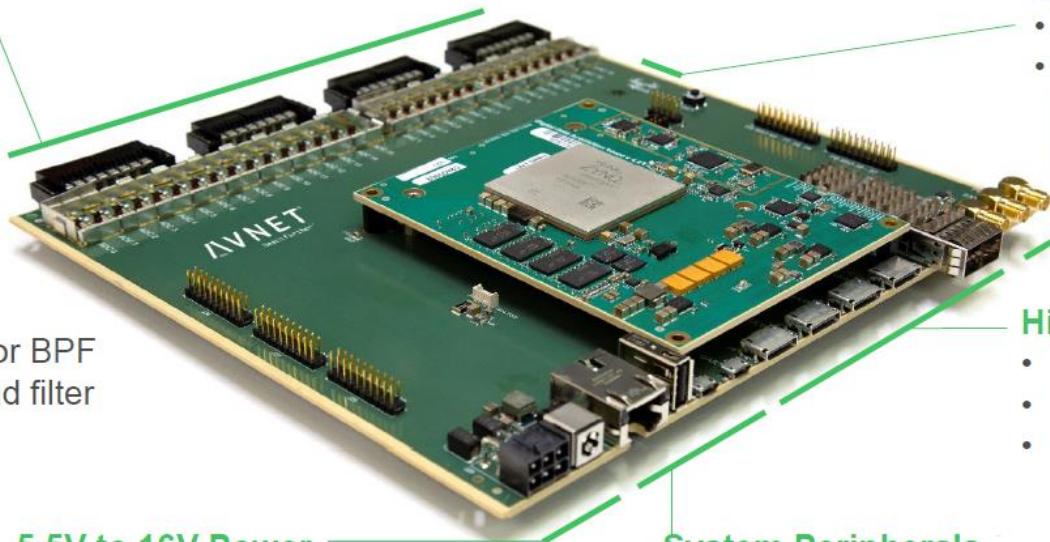
- 1 GbE
- USB, UART
- JTAG (10-pin)

### System Sync

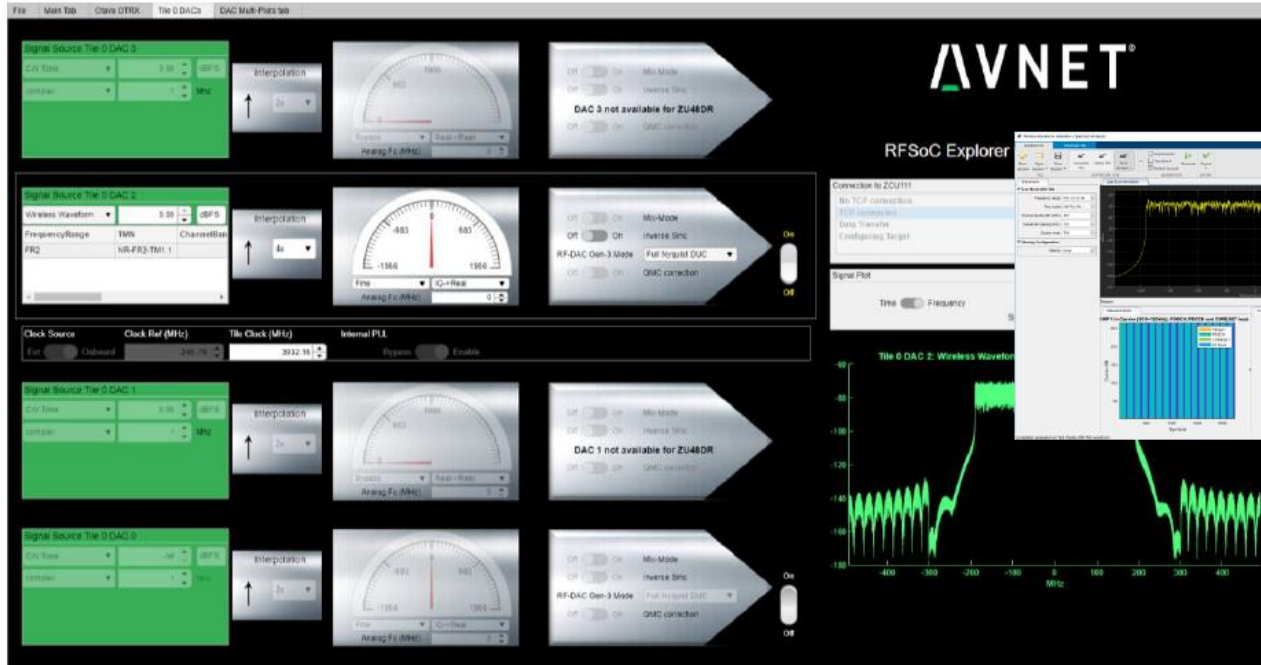
- External Ref In/Out
- Trigger In/Out

### High Speed Data Transfer

- QSFP28
- 1x PS Oculink4
- 3x PL Oculink4



# Avnet RFSoc Explorer – Native MATLAB App



5G Toolbox from MathWorks

Simulate, analyze, and test the physical layer of 5G communications systems



Create waveforms in MATLAB

Control RFSoc in MATLAB

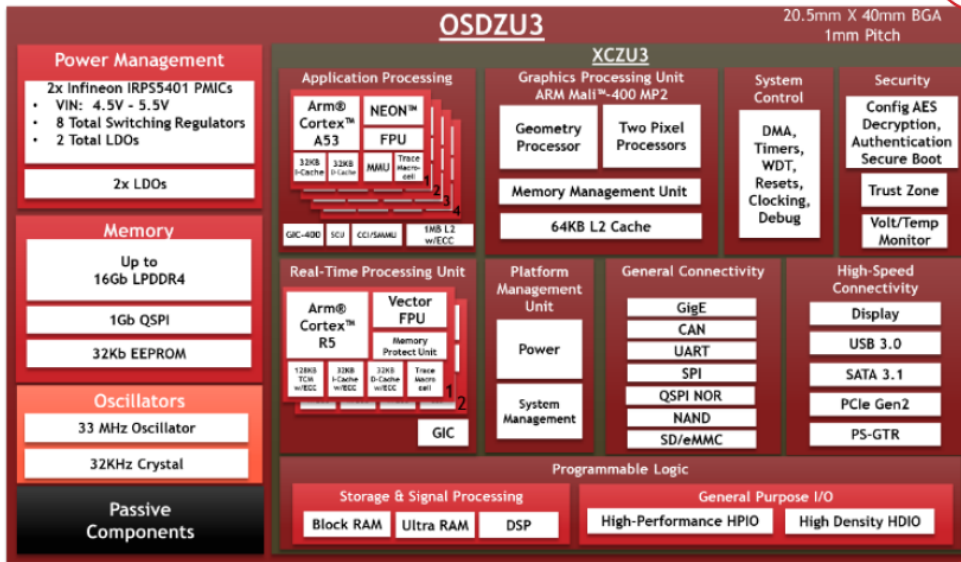
Capture & analyze in MATLAB

# Road to Versal...

Come visit us at our booth...



# OCTAVO SYSTEMS: No SoC, No SoM... SiP!!!



Integrates ZU3 MPSoC, Power Management, DDR, Oscillators, and Passives into single BGA

Access to All ZU3 I/O in the 784 pin Package

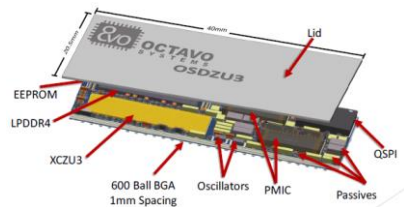
2GB LPDDR4 integrated

Single 4.5V to 5.5V Vin Generates all required power rails

Provides 2 Configurable Power rails for System Use.

Over 150 Components integrated into one 20.5mm x 40 mm package

1mm Pitch BGA allows for low-cost PCB Design Rules







**Thank You**

# Questions