

PolarFire SoC

Different and Unique SoC Solution

CERN – 3rd SoC Workshop



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

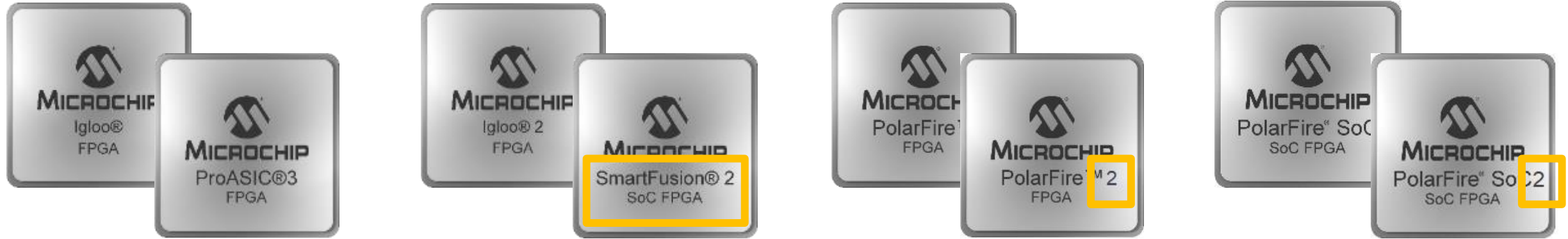
Celine Helas (MICROCHIP FAE) & Gregory Donzel (AVNET SILICA FAE)

October, 2023



SMART | CONNECTED | SECURE

Broad Range FPGA Supplier



*Smallest Packages
CPLD Replacements*

*More Resources
Low Density FPGAs*

*Cost Optimized
Mid-Range Density FPGAs*

*Quad Core RISC V
Real Time / Linux*

Up to 50% Lower Power

Proven Security

SEU Immune FPGA Configuration

Instant-on and Non-volatile



Embedded Processors on MICROCHIP FPGA's

- PolarFire® is our 1st Mid-Range FPGA family
- PolarFire® SoC offers the 1st RISC-V core complex in the programmable market

| Features | SmartFusion ProASIC3, IGLOO | SmartFusion2 IGLOO2 | PolarFire | PolarFire SoC |
|-------------------------|----------------------------------------|---------------------------------------------------------|---------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| Logic Elements | 100 - 30K | 5K - 150K | 100K - 480K | 25K - 450K |
| Transceiver Rate | -- | 1-5 Gbps | 250 Mbps-12.7 Gbps | 250 Mbps-12.7 Gbps |
| I/O Speeds | 400 Mbps LVDS | 667 Mbps DDR3 750 Mbps LVDS | 1600 Mbps DDR4 1.6 Gbps LVDS | 1600 Mbps DDR4 1.6 Gbps LVDS |
| DSP (18x18 Multipliers) | -- | 240 | 1480 | 1420 |
| Max RAM | 144 Kb | 5 Mb | 33 Mb | 32 Mb |
| Processor Option | 100 MHz ARM Cortex-M3 | Soft RISC-V Secure MCU 166 MHz ARM Cortex-M3 | Soft RISC-V Hard Crypto Co-Processor | Soft RISC-V 5x Hard RISC-V (1xE51 + 4xU54) Multicore System (625MHz) Hard Crypto Co-Processor |
| On-board Flash | Up to 512 KB code store | Up To 512 KB code store | 56 KB secure NVM | 56 KB secure NVM 128KB BootFlash |
| Family Type | CPLD Replacements Smallest Packages | Low Density FPGAs with more resources & lowest power | Mid-Range Density FPGAs Lowest Power, Cost Optimized | Open, Lowest Power, Cost Optimized, Programmable SoC |

3rd Generation 130nm

4th Generation 65nm

5th Generation 28nm

PolarFire SoC: Main Differentiators

Industry's 1st RISC V based SoC FPGA

Why RISC-V? What is it?

- Initiative of UC Berkeley in 2010 to look at what ISAs to use for their next set of projects
 - Avoid x86 and ARM solutions: both too complex, IP issues
 - Non-profit RISC-V Foundation created in 2015 to govern the ISA



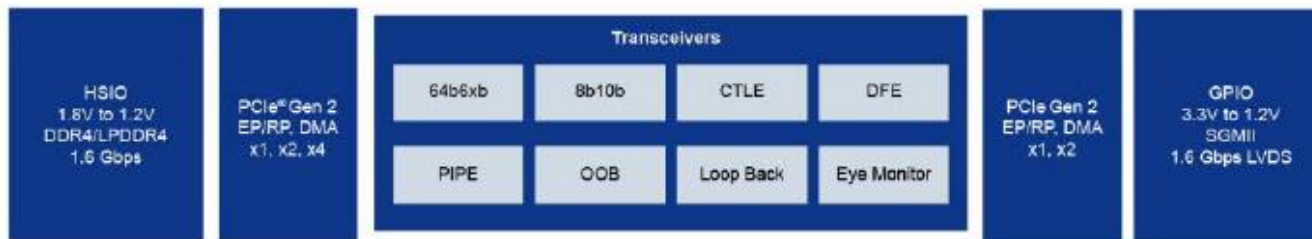
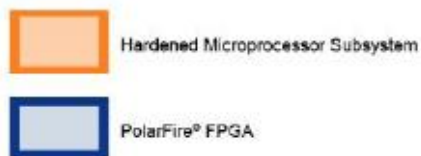
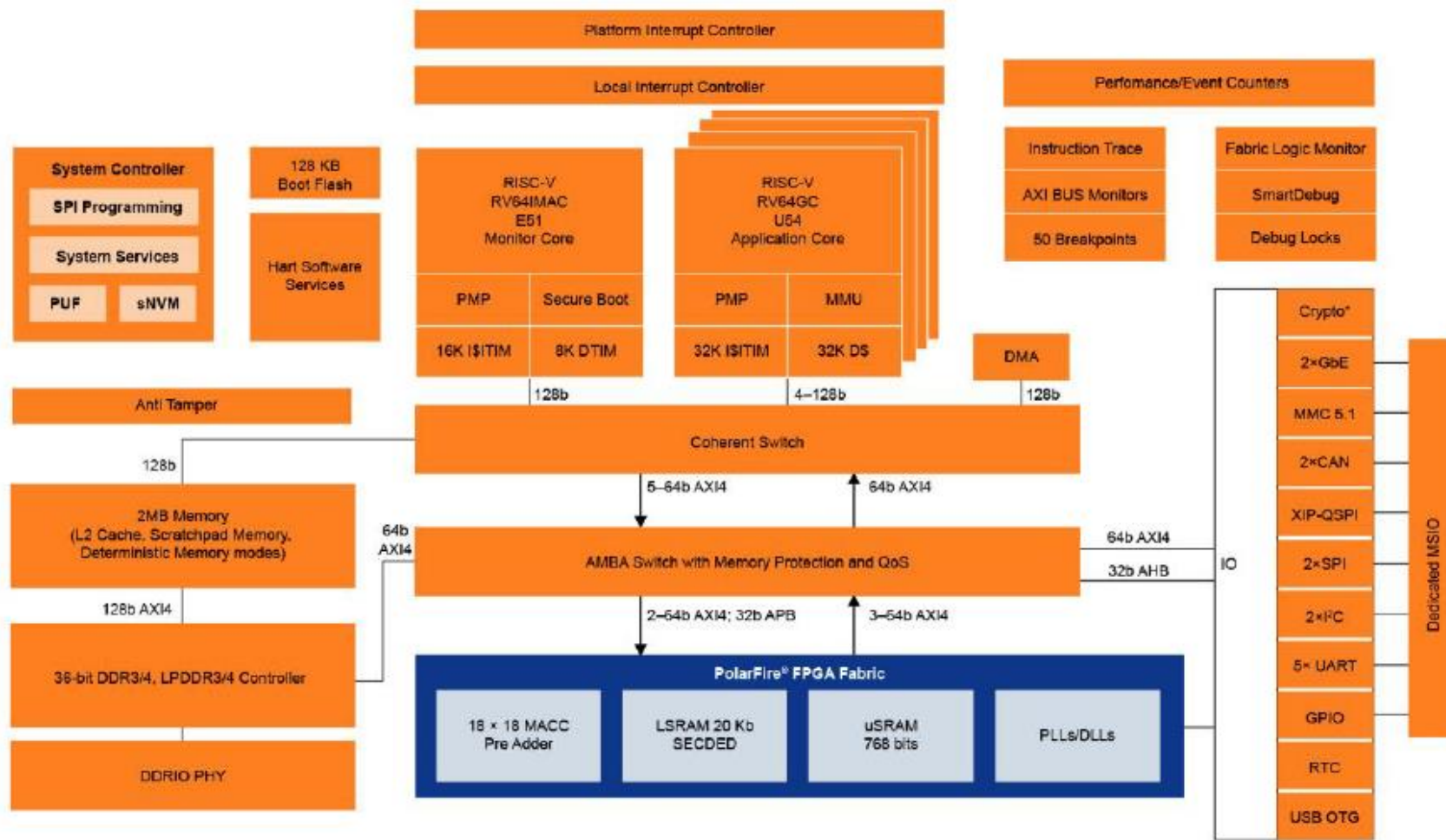
- ISA designed for
 - **Simplicity** - < 50 instructions required to run Linux. Far smaller than other commercial ISAs
 - **Longevity** - Fixed ISA for long term code portability and easy migration to an ASIC (when using Soft RISC-V = Mi-V) without negotiating a license from ARM

- **Open Source ISA**
 - Allows for RTL inspection – Trust and Certifications
 - Strong industry support - > 60 Sponsor companies.

- **A modular ISA**
 - Small standard base ISA
 - Multiple standard extensions

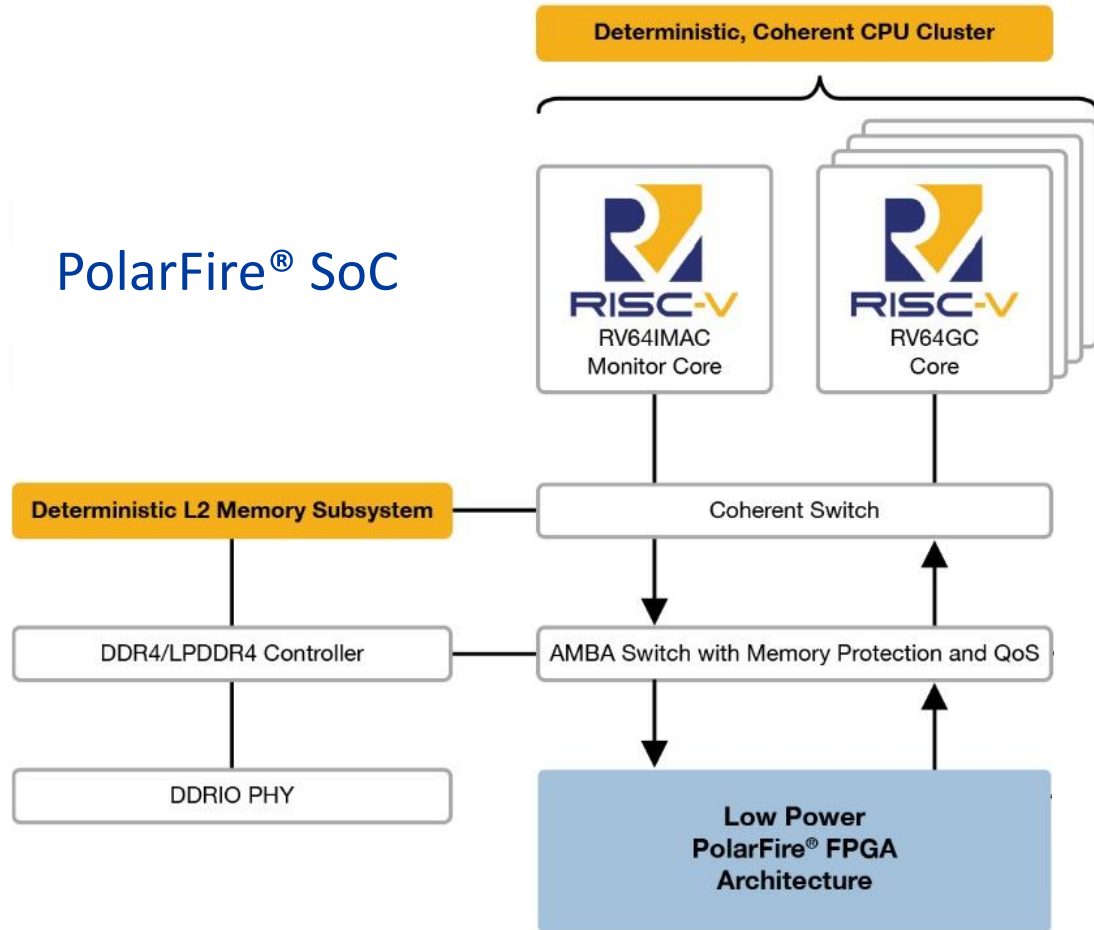


PolarFire® SoC - RISC-V Innovation Platform



*DPA-Safe Crypto co-processor supported in S devices
**SECEDED supported on all MSS memories

Enjoy Absolute Freedom to Innovate...



Asymmetric MultiProcessing (AMP)
with 2X power efficiency

Quad-core 64-bit RISC-V processors

Linux® and real-time operating systems

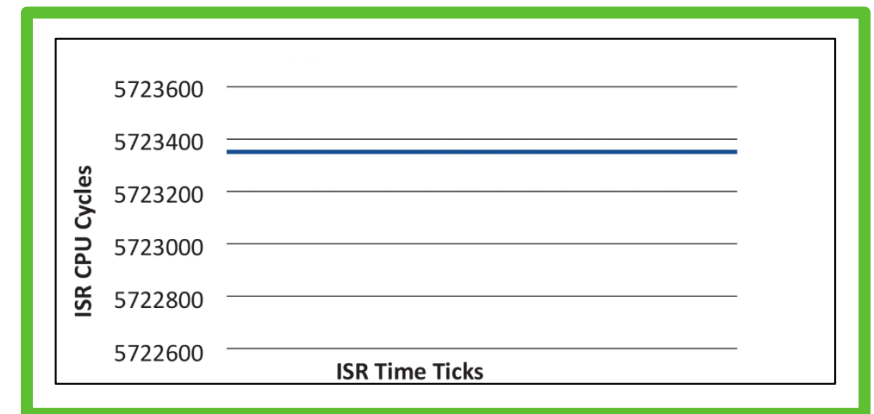
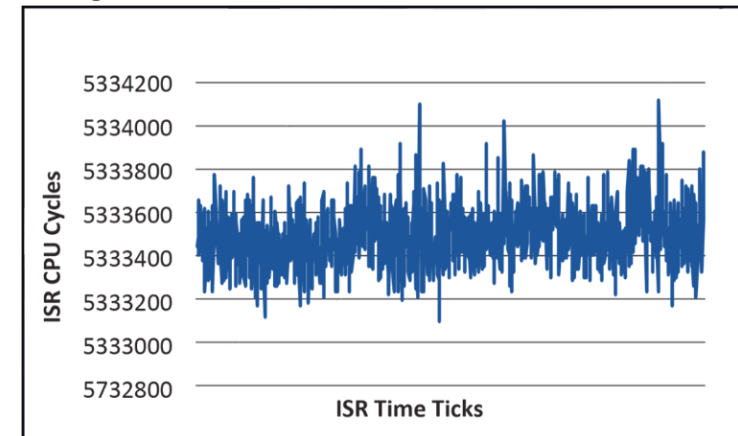
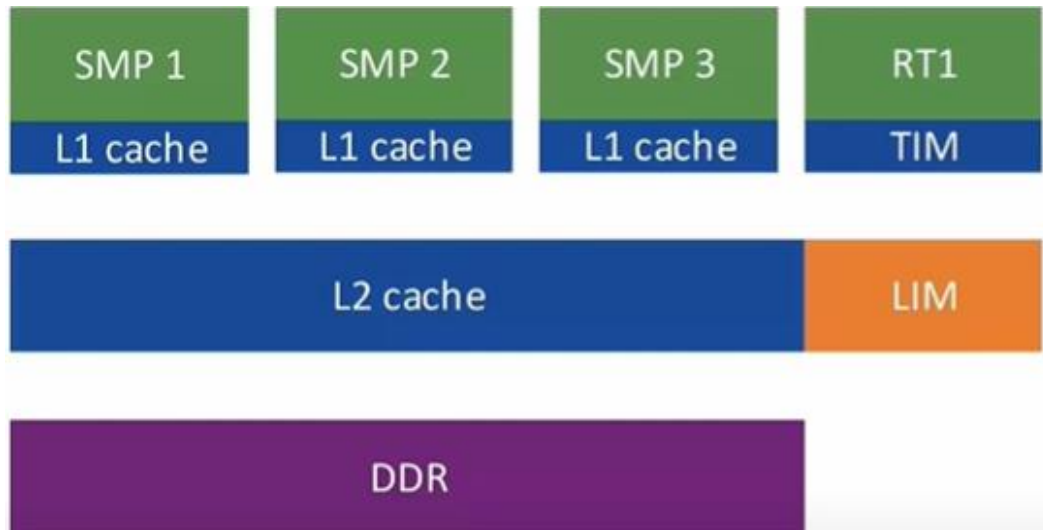
Highly flexible 2MB L2 cache

*With the most comprehensive RISC-V
development ecosystem*

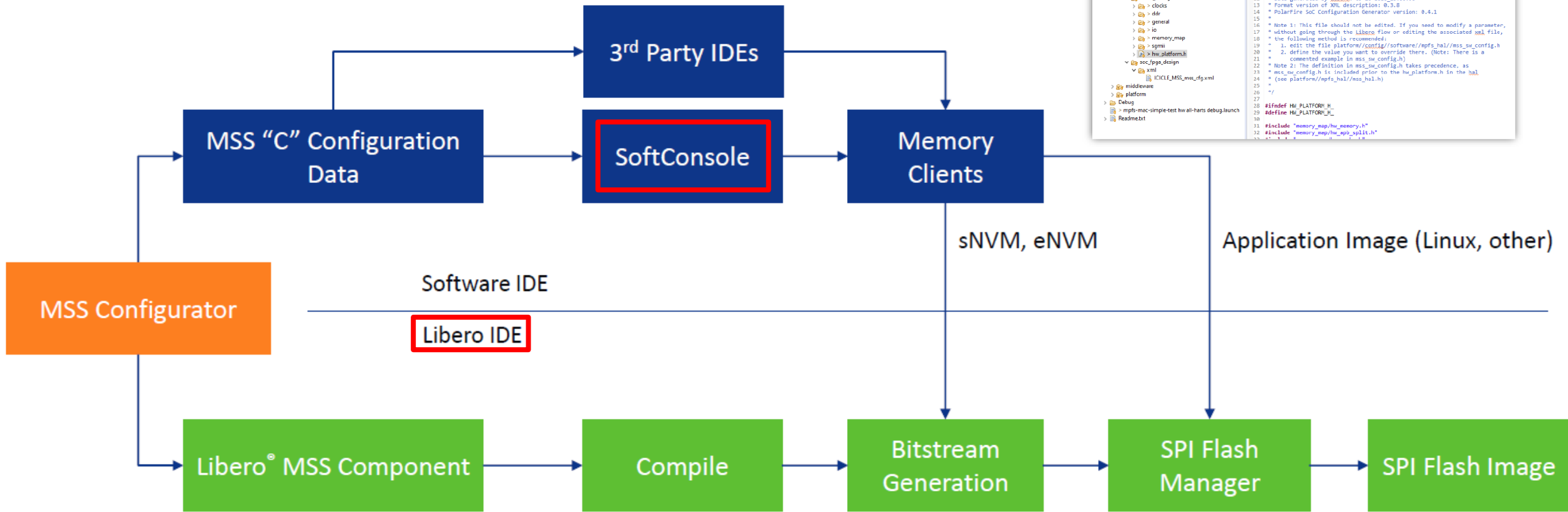
AMP is a Key Differentiator

Develop Deterministic Hard, Real-Time Systems

- Deterministic real-time systems
- L2-Loosely Integrated Memory (LIM) with branch prediction turned off
- Unique to PolarFire[®] SoC
 - Not offered by competition



Development Flow and Tools



The screenshots show the **Libero IDE** interface. The top screenshot displays the **MSS Configuration Data** table, which lists various MSS components and their configurations. The middle screenshot shows the **MSS Component** configuration, including the **Processors** and **Peripherals** sections. The bottom screenshot shows the **Bitstream Generation** process, including the **Bitstream** and **Flash** sections.

| Component | Enabled | Offset Address | Range | High Address | Enabled | Offset Address | Range | High Address |
|-----------|---------|----------------|-------|--------------|---------|----------------|-------|--------------|
| MEMORY_1 | ON | 0x00000000 | 4 KB | 0x00000004 | ON | 0x00000000 | 4 KB | 0x00000004 |
| MEMORY_2 | ON | 0x00000004 | 4 KB | 0x00000008 | ON | 0x00000004 | 4 KB | 0x00000008 |
| MEMORY_3 | ON | 0x00000008 | 4 KB | 0x0000000C | ON | 0x00000008 | 4 KB | 0x0000000C |
| MEMORY_4 | ON | 0x0000000C | 4 KB | 0x00000010 | ON | 0x0000000C | 4 KB | 0x00000010 |
| MEMORY_5 | ON | 0x00000010 | 4 KB | 0x00000014 | ON | 0x00000010 | 4 KB | 0x00000014 |
| MEMORY_6 | ON | 0x00000014 | 4 KB | 0x00000018 | ON | 0x00000014 | 4 KB | 0x00000018 |
| MEMORY_7 | ON | 0x00000018 | 4 KB | 0x0000001C | ON | 0x00000018 | 4 KB | 0x0000001C |
| MEMORY_8 | ON | 0x0000001C | 4 KB | 0x00000020 | ON | 0x0000001C | 4 KB | 0x00000020 |
| MEMORY_9 | ON | 0x00000020 | 4 KB | 0x00000024 | ON | 0x00000020 | 4 KB | 0x00000024 |
| MEMORY_10 | ON | 0x00000024 | 4 KB | 0x00000028 | ON | 0x00000024 | 4 KB | 0x00000028 |

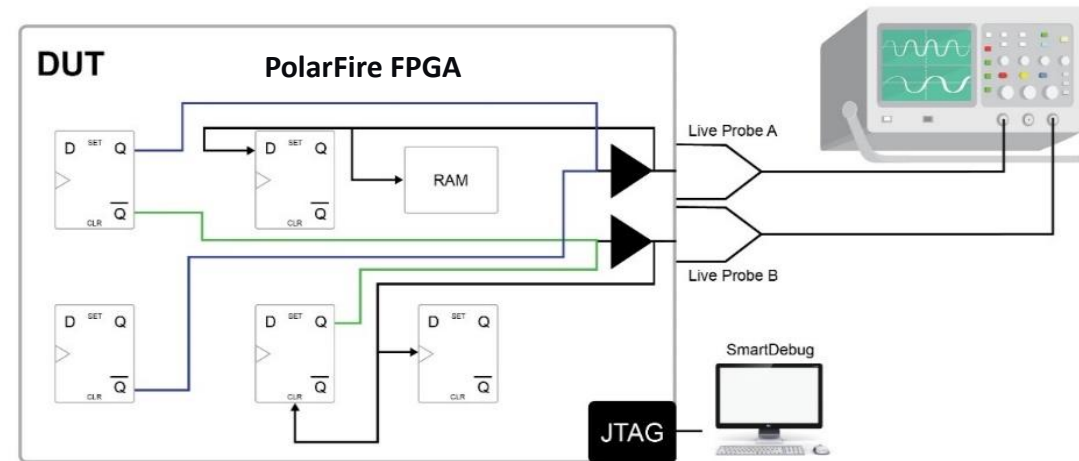
Separate flows for the embedded developer and the FPGA designer

SmartDebug – Live Probes

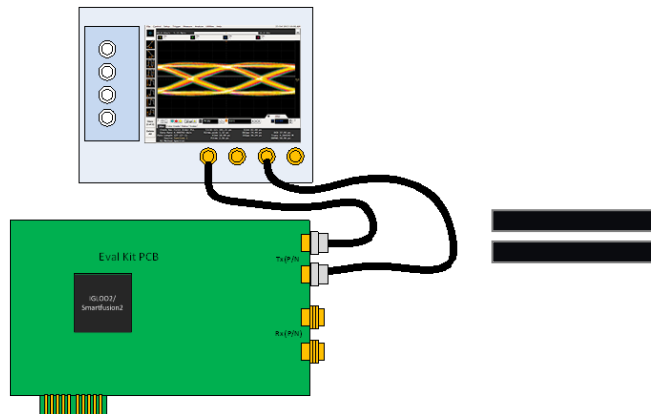
Oscilloscope Inside Your FPGA



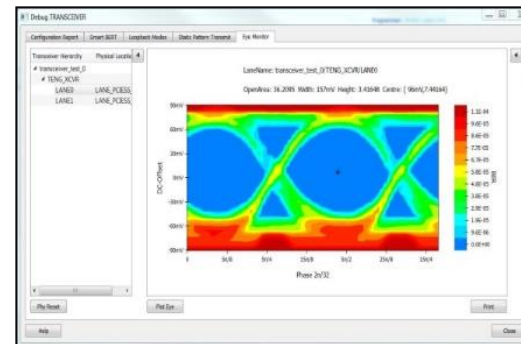
- Pick any 2 points inside the device and you can view them on an oscilloscope
- No recompiling required
- Slashes Debug Time



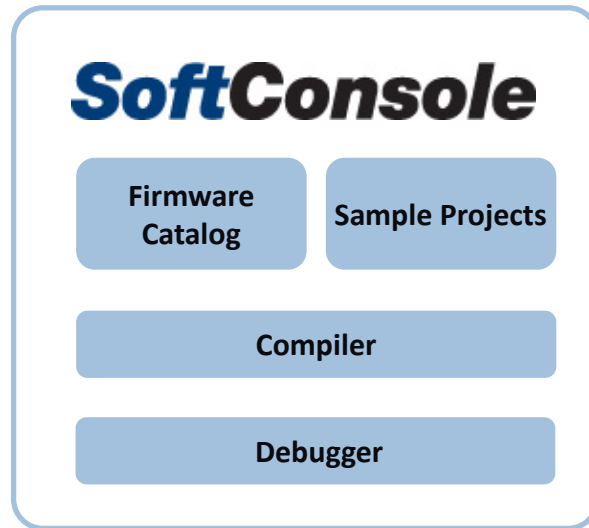
- Even SERDES Debug Available



SmartDebug Screen Shot



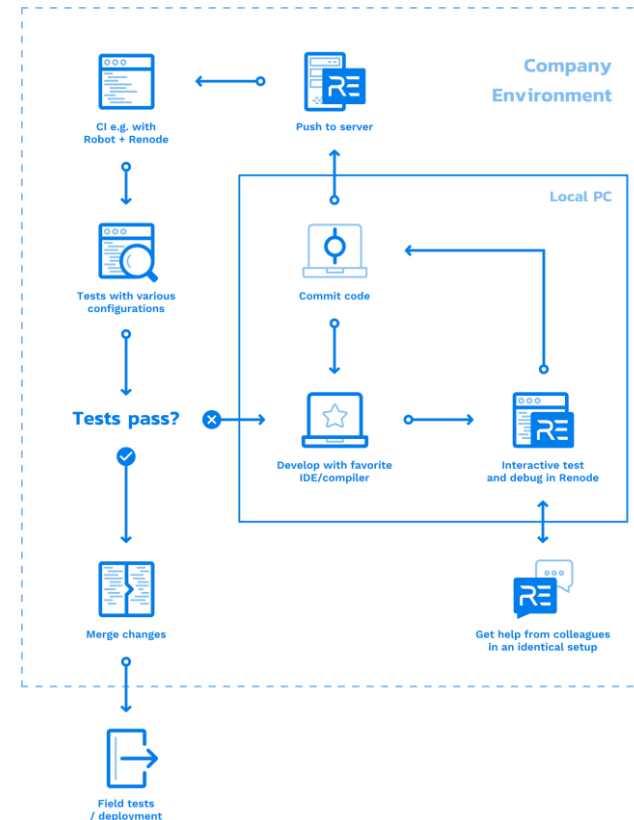
Renode Virtual development platform



Eclipse IDE Design Flow

RENODE™

- Free Rapid Software Development and Debug Capabilities Without Hardware
- 17 video tutorials on the web
 - [renode webinar series](#)



Mi-V Ecosystem Solutions



Technolution

IP / SoftCPU

Development Tools

OS / RTOS

Mi-V

Hardware

Design Services

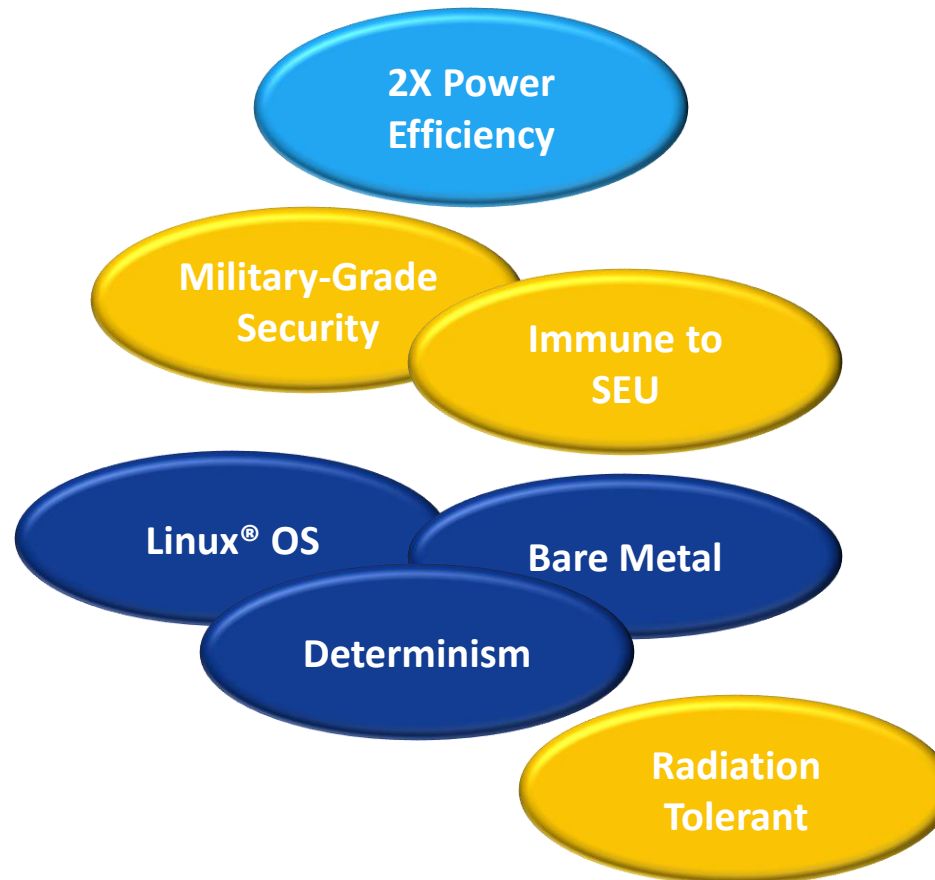
Middleware

$$\begin{bmatrix} Op \\ BL \end{bmatrix} \times \begin{bmatrix} en \\ AS \end{bmatrix}$$



New Challenges at the 'Edge'

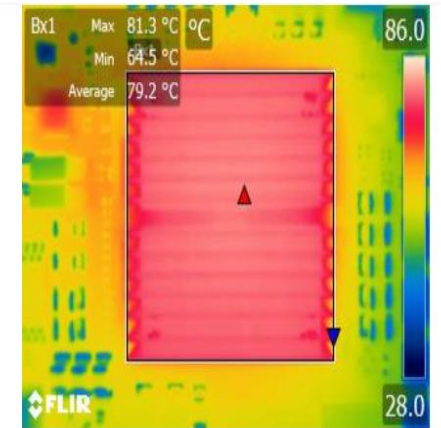
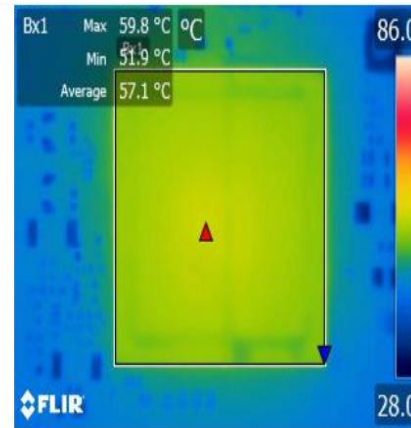
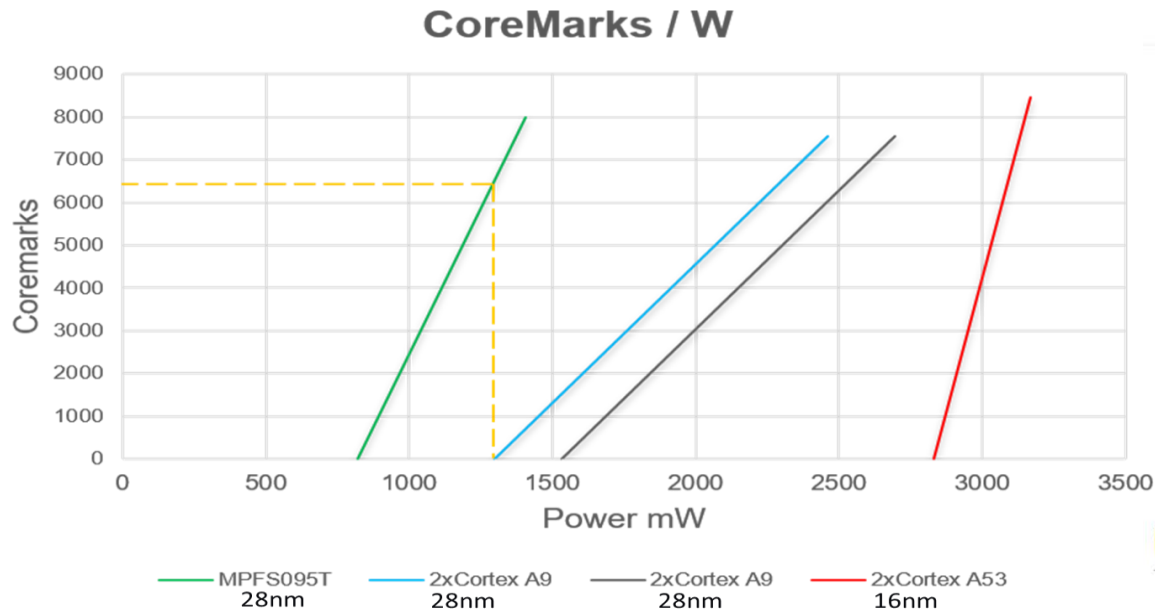
Top Five Demands of
The Intelligent Edge



Power is Money: FPGAs With Exceptional Compute and Thermal Efficiency

6500 CoreMark score of processing *before competitor gets started*

\$1.5 / W to Remove Heat
Throw out heat sinks, fans, complex chassis



10°C rise in temp doubles the FIT

Defense Grade Security, Ready for IoT

- **PolarFire SoC inherits best in class PolarFire FPGA Security**
 - DPA resistant bitstream programming
 - Anti-tamper
 - Cryptographical bound supply chain assurance
 - Physically Unclonable function
 - True random number generator
 - Side channel resistant crypto coprocessor
- **PolarFire SoC adds:**
 - + Standard secure boot and user defined Secure Boot
 - + Spectre and Meltdown immunity
 - + Physical Memory Protection
 - + SECDED on all memories MSS memories



Endurance for Any Design

Microchip FPGAs have exceptional reliability



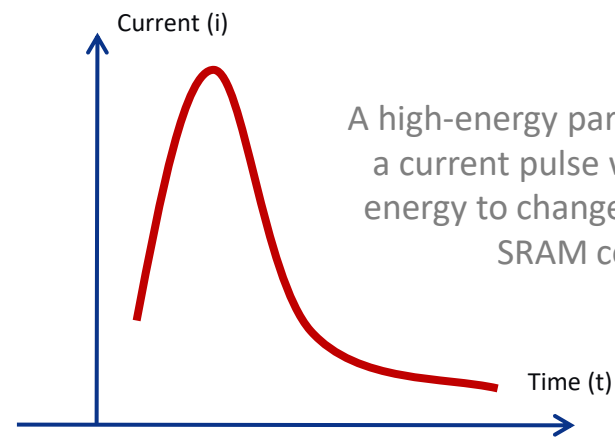
An FPGA fabric that's immune to SEU

No scrubbing required/lowers design cost

MSS memories protected via built-in SECDED

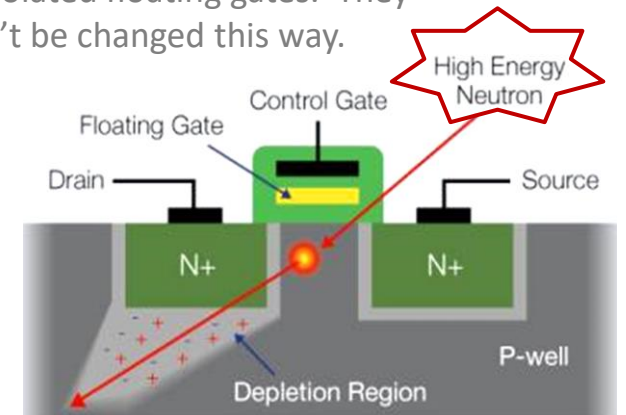
System Controller Suspend Mode

For any safety-critical application



A high-energy particle can have a current pulse with enough energy to change the state of SRAM cells!

But Microchip FPGAs store charges in oxide-isolated floating gates. They can't be changed this way.



High Reliability Screening and Qualification

- **Supported qualification standards**

- JEDEC
- JEDEC+
 - ELFR 48hr Burn-In
 - $V_{DD}+20\%$ & T_j (140C) vs Datasheet specs
- AECQ-100
- Mil Std 883 Class B
- PEMs qual on request

- **Gold bond wire options**

| Commercial | Industrial | Automotive T2/T1 | Mil Temp | Mil-Std 883 class B |
|------------------|--------------------|-----------------------|-------------------|---------------------|
| Wafer Sort | Wafer Sort | Wafer Sort | Wafer Sort | Wafer Sort |
| Package Assembly | Package Assembly | Package Assembly | Package Assembly | Package Assembly |
| Final Test +25°C | Final Test +25°C | Burn-in (Dyn, Opt.) | Final Test +25°C | Internal Visual |
| | Sample Test +100°C | Final Test +25°C | Final Test -55°C | Temp. Cycling |
| | | Final Test +125/135°C | Final Test +125°C | Const. Acceleration |
| | | | | PIND |
| | | | | Visual |
| | | | | Electrical Test |
| | | | | Dynamic Burn-in |
| | | | | Final Test +25°C |
| | | | | Final Test -55°C |
| | | | | Final Test +125°C |
| | | | | Seal |
| | | | | Group A Lot Sample |
| | | | | Group B Lot Sample |
| QC Mon. Sample | QC Mon. Sample | QC Mon. Sample | QC Mon. Sample | QC Mon. Sample |

Microchip FPGAs Immunity to Config Failures

| | | Equivalent Functional Failure Rate - FIT Rates Per Device | | | |
|--------------------------------------|-----------------|-----------------------------------------------------------|--------------|--------------------|-----------------------|
| | | Ground Level Applications | | Aviation (Typical) | Aviation (Worst Case) |
| FPGA | Technology | Sea level -NYC | 5,000' - NYC | 40,000' - NYC | 50,000' - 80°N |
| Microchip PolarFire® FPGA | 28 nm SONOS | No Failures Detected | | | |
| Microchip SmartFusion® 2 FPGA M2S050 | 65 nm Flash | No Failures Detected | | | |
| Microchip Fusion® FPGA AFS1500 | 130 nm Flash | No Failures Detected | | | |
| Microchip ProASIC® 4 FPGA A3PE600 | 130 nm Flash | No Failures Detected | | | |
| Microchip ProASIC® Plus FPGA APA1000 | 220 nm Flash | No Failures Detected | | | |
| Microchip Accelerator® FPGA AX1000 | 150 nm Antifuse | No Failures Detected | | | |
| Competitor X 3M Gate FPGA | 150 nm SRAM | 1,150 | 4,200 | 592k | 1.1M |
| Competitor X 1M Gate FPGA | 90 nm SRAM | 320 | 1,200 | 165k | 319k |
| Competitor X 24k Logic Cell FPGA | 45 nm SRAM | 1,180 | 4,300 | 608k | 1.1M |
| Competitor X 44k Logic Cell FPGA | 45 nm SRAM | 2,170 | 7,900 | 1.1M | 2.2M |
| Competitor X 75k Logic Cell FPGA | 40 nm SRAM | 2,527 | 9,200 | 1.3M | 2.5M |
| Competitor X 75k Logic Cell FPGA | 28 nm SRAM | 2,481 | 9,100 | 1.3M | 2.4M |
| Competitor I 1M Gate FPGA | 130 nm SRAM | 460 | 1,700 | 237k | 458k |
| Competitor I 1M Gate FPGA | 90 nm SRAM | 730 | 2,700 | 376k | 727k |
| Competitor I 2M Gate FPGA | 65 nm SRAM | 1,600 | 5,800 | 824k | 1.6M |
| Competitor I 25k Logic Cell FPGA | 65 nm SRAM | 580 | 2,100 | 299k | 578k |
| Competitor I 55k Logic Cell FPGA | 65 nm SRAM | 1,500 | 5,500 | 773k | 1.5M |
| Competitor I 120k Logic Cell FPGA | 65 nm SRAM | 2,900 | 10,600 | 1.5M | 2.9M |
| Competitor I 50k Logic Cell FPGA | 60 nm SRAM | 2,200 | 8,000 | 1.1M | 2.2M |

- FIT = number of errors in 10⁹ hours – Acceptable FIT rates for high-reliability applications are < 20
- Testing of Microchip FPGAs and competition at 90nm, 130nm, and 150nm performed by IROC Technologies
- Competitor X 45nm, 40nm, and 28nm based on reliability data, Competitor I 65nm and 60nm estimated at 100 Fit / Mbit

Dependable Longevity of Supply

January 26, 2022

Dear Valued Customer,

Thank you for your continued interest in Microchip/Microsemi FPGA products. The purpose of this letter is to address Microchip/Microsemi's FPGA product longevity. Below you will find a matrix of device families with data on when parts first shipped and an approximate timeframe that we expect to have wafer availability; please note that this is not a guarantee of availability.

| Device Family Name | Microsemi Part Number Starts With... | Year First Shipped | Expected Availability from 2021 |
|--------------------|--------------------------------------|--------------------|---------------------------------|
| MX | A40MX, A42MX | 1997 | 10 years |
| SX | A54SX | 1999 | 5 years |
| SXA | A54SX_A | 1999 | 10 years |
| AX | AX | 2001 | 10 years |
| eX | eX | 2001 | 10 years |
| ProAsic Plus | APA | 2001 | 10 years |
| ProAsic 3 | A3P, A3PN, A3PL | 2005 | 10 years |
| Igloo | AGL, AGLN | 2005 | 10 years |
| Igloo Plus | AGLP | 2005 | 10 years |
| Fusion | AFS | 2006 | 10 years |
| SmartFusion | A2F | 2010 | 10 years |
| SmartFusion 2 | M2S | 2013 | 15 years |
| Igloo 2 | M2GL | 2013 | 15 years |
| PolarFire | MPF | 2017 | 20 years |
| PolarFire Soc | MPFS | 2021 | 20 years |

Note: The expected supply continuity does not apply to EOL'ed products.

March 13, 2023

Dear Valued Customer,

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| SXA | A54SX_A | 1999 | 10 years |
| AX | AX | 2001 | 10 years |
| eX | eX | 2001 | 10 years |
| ProAsic Plus | APA | 2001 | 10 years |
| ProAsic 3 | A3P, A3PN, A3PL | 2005 | 10 years |
| Igloo | AGL, AGLN | 2005 | 10 years |
| Igloo Plus | AGLP | 2005 | 10 years |
| Fusion | AFS | 2006 | 10 years |
| SmartFusion | A2F | 2010 | 10 years |
| SmartFusion 2 | M2S | 2013 | 15 years |
| Igloo 2 | M2GL | 2013 | 15 years |
| PolarFire | MPF | 2017 | 20 years |
| PolarFire Soc | MPFS | 2021 | 20 years |
| RTSX-SU | RTSxxxSU | 2004 | 10 years |
| RTAX-S/SL | RTAXxxxS, RTAXxxxSL | 2004 | 15 years |
| RTAX-DSP | RTAXxxxD, RTAXxxxDL | 2011 | 15 years |
| RT ProASIC3 | RT3P | 2010 | 15 years |
| RTG4 | RT4G150 | 2015 | 15 years |
| RT PolarFire | RTPF | 2022 | 20 years |

Note: The expected supply continuity does not apply to EOL'ed products.

PolarFire SoC Family

| | Features | MPFS025T | MPFS095T | MPFS160T | MPFS250T | MPFS460T |
|---------------------------------------------------------------|------------------------------------------------|-------------------------------------|---------------------|---------------------|----------------------|----------------------|
| FPGA Fabric | K Logic Elements (4LUT + DFF) | 23 | 93 | 161 | 254 | 461 |
| | Math Blocks (18x18 MACC) | 68 | 292 | 498 | 784 | 1420 |
| | LSRAM Blocks (20k bit) | 84 | 308 | 520 | 812 | 1460 |
| | uSRAM Blocks (64x12) | 204 | 876 | 1494 | 2352 | 4260 |
| | Total RAM Mbits | 1.8 | 6.7 | 11.3 | 17.6 | 31.6 |
| | uPROM Kbits | 194 | 387 | 415 | 470 | 553 |
| | User DLL's/PLL's | 8 each | 8 each | 8 each | 8 each | 8 each |
| High Speed IO | 250 Mbps to 12.5 Gbps SERDES Lanes | 4 | 4 | 8 | 16 | 20 |
| | PCIe Gen2 End Points/Root Ports | 2 | 2 | 2 | 2 | 2 |
| Total FPGA IO | HSIO+GPIO | 108 | 276 | 312 | 372 | 468 |
| Total MSS IO | MSS IO | 136 | 136 | 136 | 136 | 136 |
| MSS DDR DB | MSS DDR Data Bus | 16 / 32 | 16 / 32 | 32 | 32 | 32 |
| Packaging Commerical & Industrial RoHS | Type/Size/Pitch | MSS IO / HSIO / GPIO / XCVRs | | | | |
| | FCSG325 (11x11, 11x14.5 ⁺ , 0.5 mm) | 102 / 32 / 48 / 2 | 102 / 32 / 48 / 2 | | | |
| | FCSG536 (16x16, 0.5 mm) | | 136 / 60 / 108 / 4 | 136 / 60 / 108 / 4 | 136 / 60 / 108 / 4 | |
| | FCVG484 (19x19, 0.8 mm) | 136 / 60 / 48 / 4 | 136 / 60 / 84 / 4 | 136 / 60 / 84 / 4 | 136 / 60 / 84 / 4 | |
| | FCVG784 (23x23, 0.8 mm) | | 136 / 144 / 132 / 4 | 136 / 144 / 168 / 8 | 136 / 144 / 180 / 8 | |
| | FCG1152 (35x35, 1.0 mm) | | | | 136 / 144 / 228 / 16 | 136 / 180 / 288 / 20 |

Extended Commercial (0°C-100°C) and Industrial (-40°C-100°C) Temperature Support for all Die Package Combinations - RoHS only

Additional Temp Grade: Military (-55°C-125°C) - Leaded packages only

⁺ FCSG325 package dimension for MPFS095T: 11x14.5, 0.5mm)



PolarFire SoC

Full temperature range offering

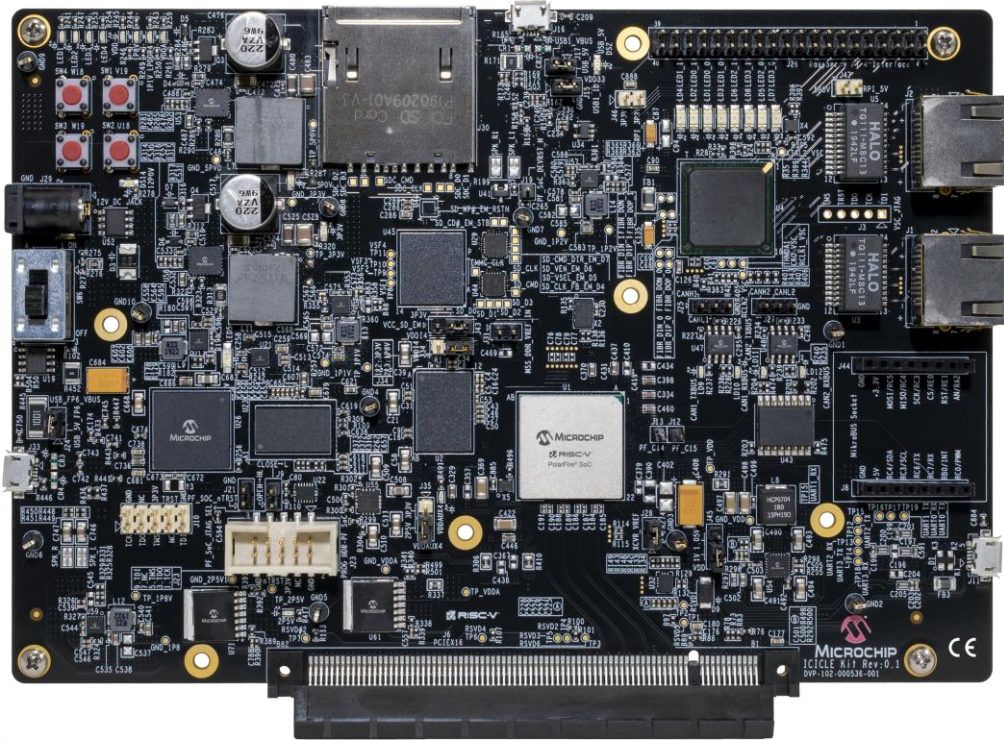
| Features | MPFS025T | MPFS095T | MPFS160T | MPFS250T | MPFS460T |
|-----------------------------------------|-------------------------------------|---------------------|---------------------|----------------------|----------------------|
| Extended Commercial / Industrial | MSS IO / HSIO / GPIO / XCVRs | | | | |
| FCSG325 ⁺ (11x11, 0.5 mm) | 102 / 32 / 48 / 2 | 102 / 32 / 48 / 2 | | | |
| FCSG536 (16x16, 0.5 mm) | | 136 / 60 / 84 / 4 | 136 / 60 / 108 / 4 | 136 / 60 / 108 / 4 | |
| FCVG484 (19x19, 0.8 mm) | 136 / 60 / 48 / 4 | 136 / 60 / 84 / 4 | 136 / 60 / 84 / 4 | 136 / 60 / 84 / 4 | |
| FCVG784 (23x23, 0.8 mm) | | 136 / 144 / 132 / 4 | 136 / 144 / 168 / 8 | 136 / 144 / 180 / 8 | |
| FCG1152 (35x35, 1.0 mm) | | | | 136 / 144 / 228 / 16 | 136 / 180 / 288 / 20 |
| Military "S" devices only | MSS IO / HSIO / GPIO / XCVRs | | | | |
| FCS25 (11x14.5, 0.5 mm) | | 102 / 32 / 48 / 2 | | | |
| FCS36 (16x16, 0.5 mm) | | | | 136 / 60 / 108 / 4 | |
| FCV484 (19x19, 0.8 mm) | | | | 136 / 60 / 84 / 4 | |
| FCV784 (23x23, 0.8 mm) | | | | 136 / 144 / 180 / 8 | |
| FC152 (35x35, 1.0 mm) | | | | 136 / 144 / 228 / 16 | 136 / 180 / 288 / 20 |
| Automotive T2 | MSS IO / HSIO / GPIO / XCVRs | | | | |
| FCSG325 ⁺ (11x11, 0.5 mm) | 102 / 32 / 48 / 2 | 102 / 32 / 48 / 2 | | | |
| FCSG536 (16x16, 0.5 mm) | | 136 / 60 / 84 / 4 | 136 / 60 / 108 / 4 | 136 / 60 / 108 / 4 | |
| FCVG484 (19x19, 0.8 mm) | 136 / 60 / 48 / 4 | 136 / 60 / 84 / 4 | 136 / 60 / 84 / 4 | 136 / 60 / 84 / 4 | |
| FCVG784 (23x23, 0.8 mm) | | 136 / 144 / 132 / 4 | 136 / 144 / 168 / 8 | 136 / 144 / 180 / 8 | |
| FCG1152 (35x35, 1.0 mm) | | | | | 136 / 180 / 288 / 20 |

⁺ FCSG325 package dimension for MPFS095T: 11x14.5, 0.5mm)

PolarFire SoC Resources

PolarFire SoC Icicle kit

Features and Collaterals



Reference designs and other collateral available [here](#)

- **PolarFire SoC (MPFS250T-FCVG484EES)** with 1× RV64IMAC core and 4× RV64GC cores by SiFive, 4× 12.7 Gbps SERDES and Secure boot
- **Memory and Storage**
 - 2 GB LPDDR4 × 32
 - 1 Gb SPI Flash
 - 8 GB eMMC Flash or SD card slot (multiplexed)
- **Interfaces**
 - 2× Gigabit Ethernet
 - Raspberry Pi-compatible 40-pin header
 - mikroBUS socket
 - PCIe® Gen 2, Micro USB 2.0 Hi-Speed OTG, 4× UART (via single micro USB), 2× CAN, SPI, I²C
- **Programming and Debugging**
 - UART via micro-USB
 - Onboard JTAG connector or embedded FlashPro6 (multiplexed)
 - 52× test points

Orderable Part Number

MPFS-ICICLE-KIT-ES

List Price

~590\$

On Github

Search for PolarFire SoC Github



PolarFire-SoC

PolarFire SoC Embedded Software

<http://www.microsemi.com/polarfiresoc>

Repositories **10** Packages People Projects

Pinned repositories

[polarfire-soc-bare-metal-library](#)

Bare metal embedded software drivers and examples for PolarFire SoC

 C  14  5

[meta-polarfire-soc-yocto-bsp](#)

PolarFire SoC yocto Board Support Package

 BitBake  10  12



[polarfire-soc-buildroot-sdk](#)

PolarFire SoC Buildroot Software Development Kit

 Makefile  13  6

[polarfire-soc-documentation](#)

PolarFire SoC Documentation

 8  5

[icicle-kit-reference-design](#)

PolarFire SoC Icicle Kit Libero reference design

 Tcl  6  1

[hart-software-services](#)

PolarFire SoC hart software services

 C  6  14

Get Started with PolarFire SoC

PolarFire® SoC
GPIOs/UIO Drivers & Yocto SDK



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

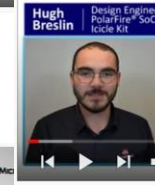
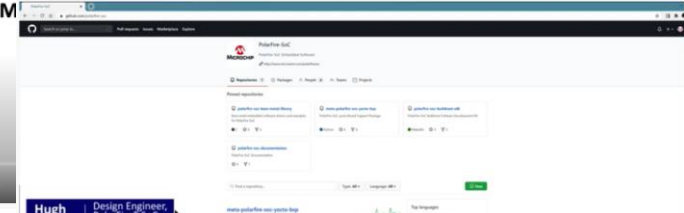
Bare Metal App Accessing



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Getting Back to Factory Defaults

- Programming the FPGA and eNVM using a provided image
- Programming the eMMC
- Generating a design and programming the FPGA
- Programming the eNVM with the HSS
- Programming the eMMC



Using the PolarFire® SoC Bare Metal Library

- Downloading the Bare Metal Library
 - Contents of the BML
- Importing projects from the BML
- Default project build configuration
- Default project debug configurations



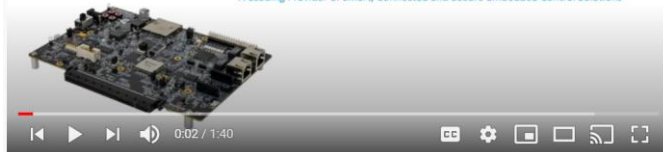
Building a Linux Yocto image



PolarFire® SoC: Running Bare Metal Application(s) from the DDR



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PolarFire® SoC Icicle Kit



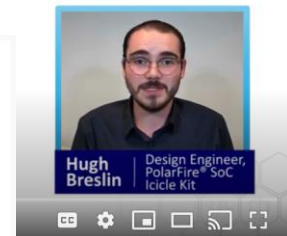
Factory MSS Configuration for the Icicle Kit

- Where to find the MSS configuration file in the reference design repository
- Opening an MSS configuration
 - Default settings



MSS Configurator Run Through

- Why use the MSS configurator?
- Installing and launching the MSS configurator
- Configuring an MSS



What is the HSS?

- Function of the HSS on system start up
- Building the HSS
 - Configuring a Windows system
- Configuring the HSS



PolarFire® SoC Summary

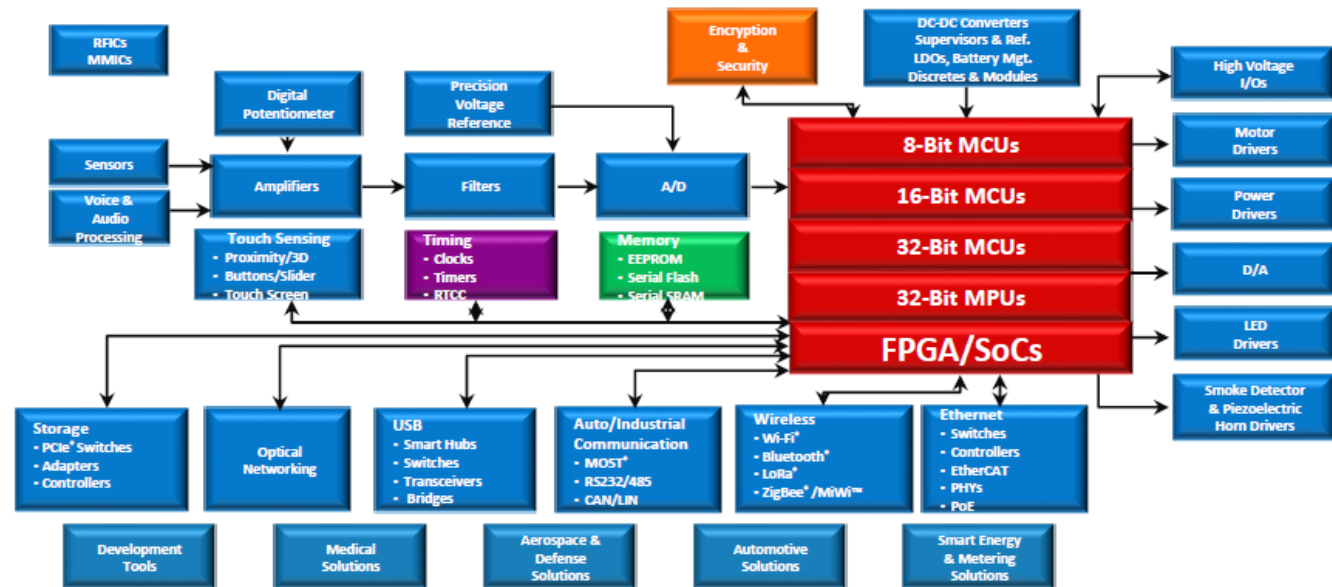
- **Polarfire® SoC-Multiprocessing**

- Linux and Real Time in a deterministic, coherent CPU cluster
- AMBA extensions into FPGA fabric for seamless communication
- Low Power
- Defense grade security/secure boot
- Exceptional reliability
- Smallest form factors – 11x11
- [Getting Started](#)

- **Longevity**

- **Microchip Total System Solutions**

- **Microchip University Virtual Classes:** www.microchip.com/mu



Thank you
