New Generation of Rad-Hard SoC FPGA

CERN SoC Workshop

Rad-hard FPGA Offering

Complete rad-hard FPGA offering and associated tools

- NX offers a complete rad-hard FPGA offering with all associated tools
- IMPULSE is the programming tools that generate any VHDL into bistream generation
- All required tools ecosystem and IPs to develop simple to complex design

NG medium

NG ultra 300

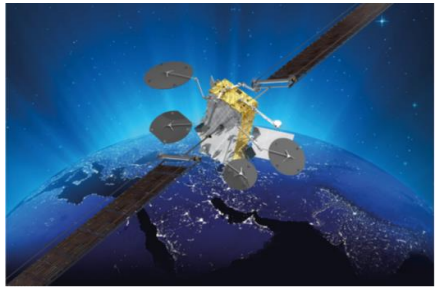
NG large

NG ultra

Key Markets

- The company is focusing on developing SoC FPGA for Hi-Rel markets
- Become quickly a clear leader on Space, Defense and Avionic market
- Focus on key market differentiators like radiation hardening, very high reliability, ITAR free etc

Space

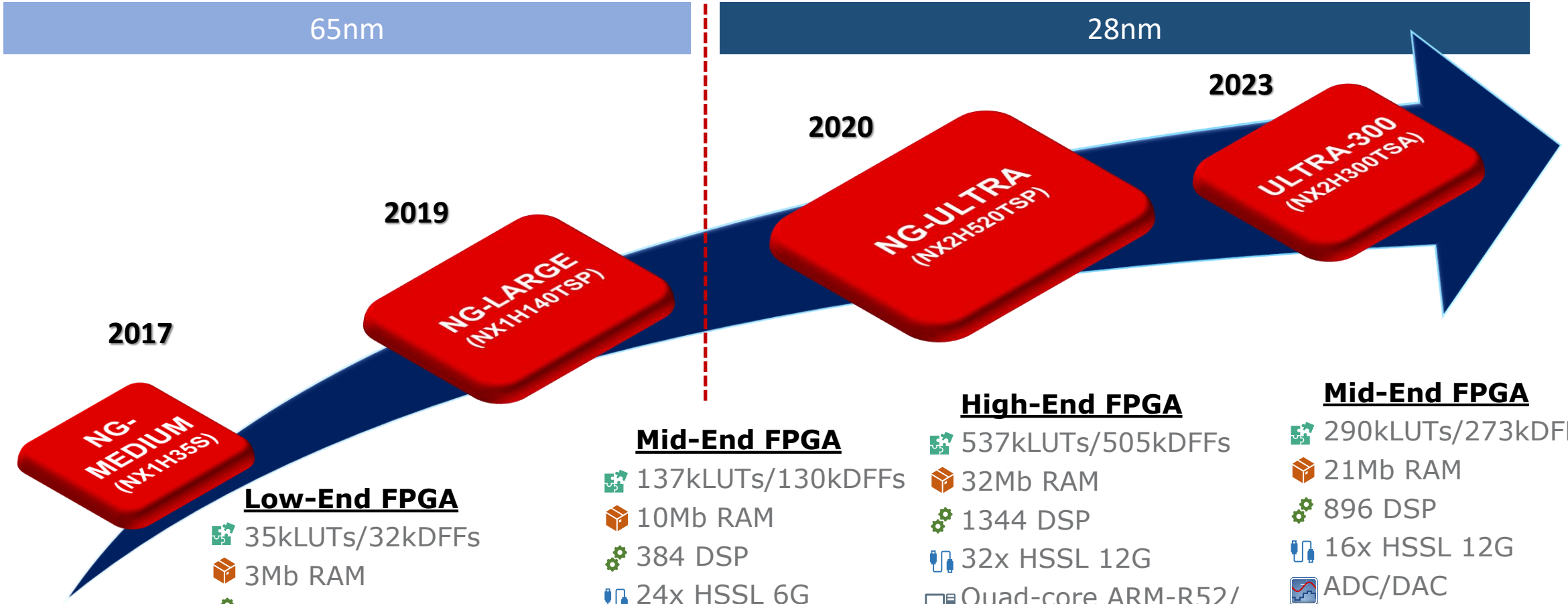


Défense

Industrial

Avionic

Rad-Hard SoC FPGA Roadmap



Low-End FPGA

- 35kLUTs/32kDFFs
- 3Mb RAM
- 112 DSP
- No HSSL
- No Hard IP Processor

Mid-End FPGA

- 137kLUTs/130kDFFs
- 10Mb RAM
- 384 DSP
- 24x HSSL 6G
- Single-core ARM-R5 (No Peripherals)

High-End FPGA

- 537kLUTs/505kDFFs
- 32Mb RAM
- 1344 DSP
- 32x HSSL 12G
- Quad-core ARM-R52/ (DAHLIA SoC)

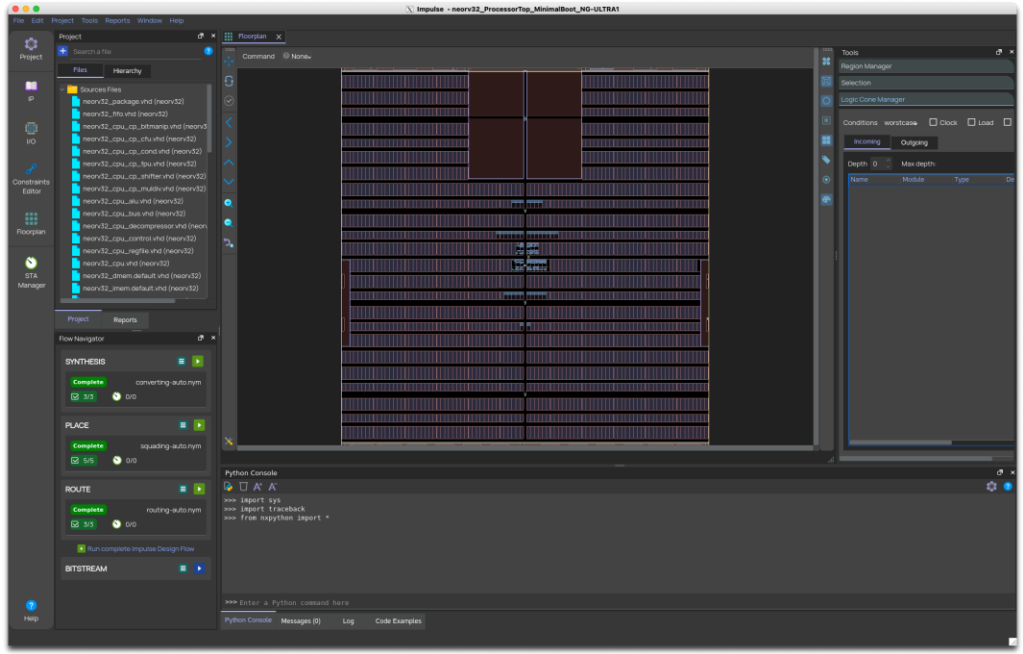
Mid-End FPGA

- 290kLUTs/273kDFFs
- 21Mb RAM
- 896 DSP
- 16x HSSL 12G
- ADC/DAC

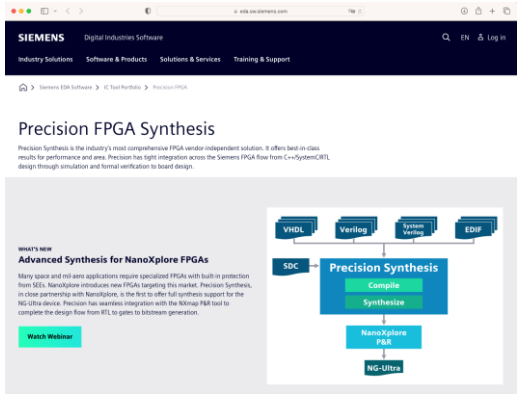
Software Tools Overview

NanoXplore's toolset: Impulse

- Performs all stages of the design, thus NanoXplore is independent from any third party tool



NanoXplore's toolset: 3rd party tools



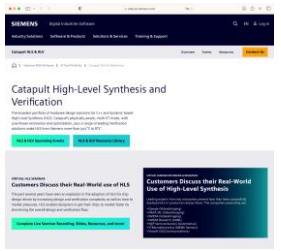
- Precision Hi-Rel (Siemens EDA): NG-ULTRA supported for Synthesis in the commercial releases

MBSE ecosystem/ HLS :

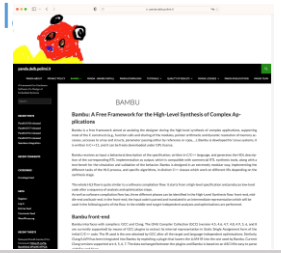
- First support available
- Further features ongoing

HDL Coder Mathworks:

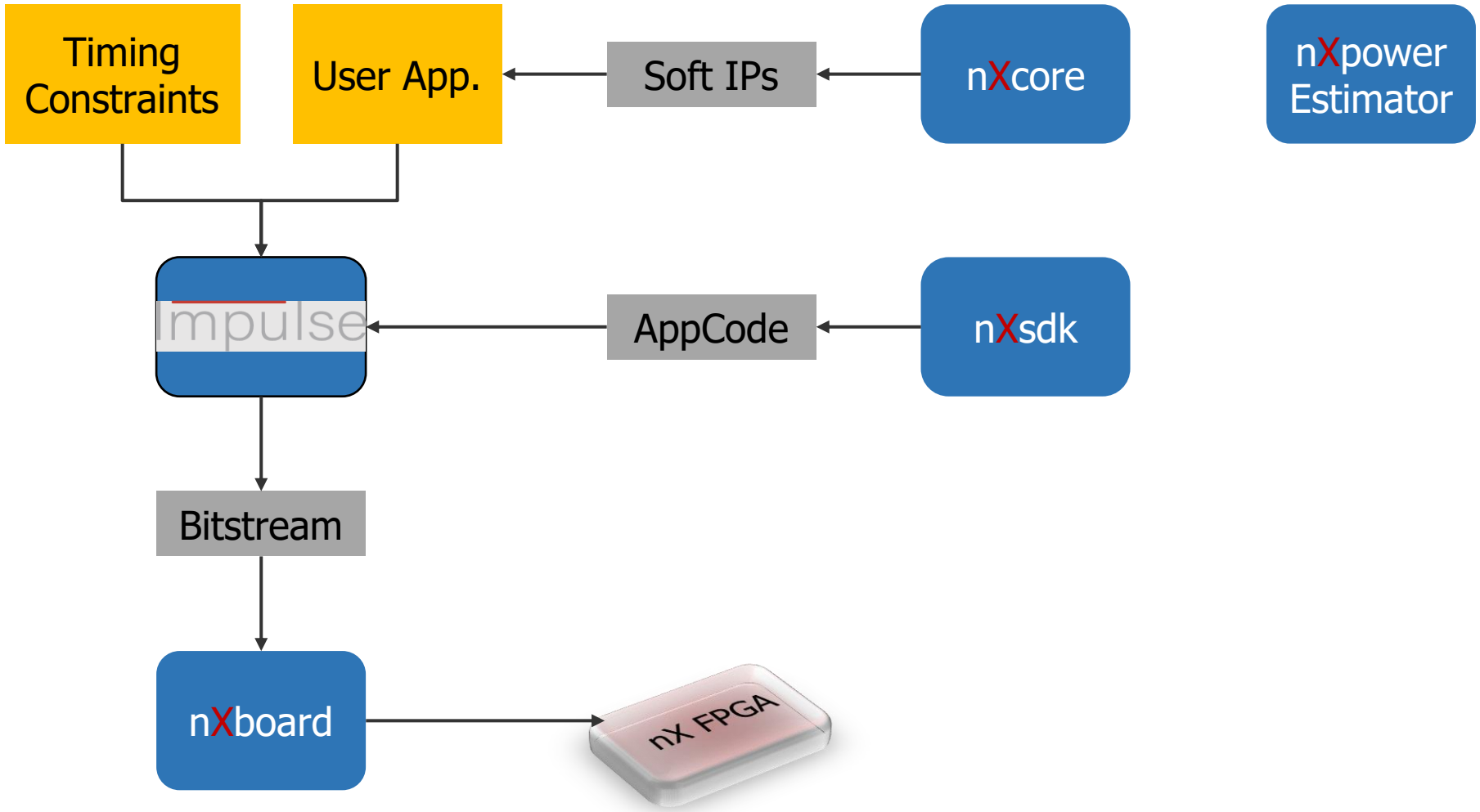
CatapultC Siemens ESA:



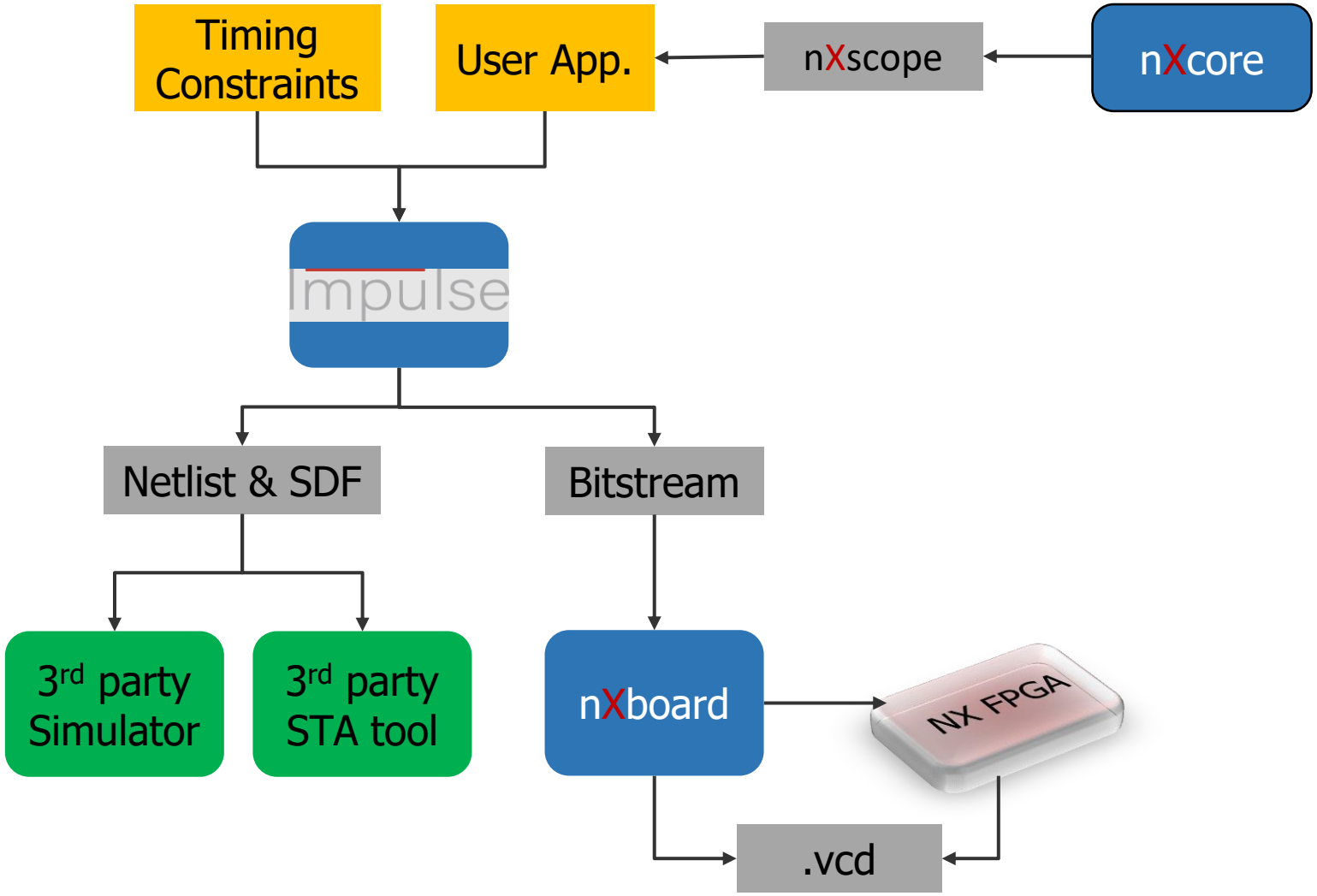
Bambu, Politecnico di Mil



Software Tools Flow



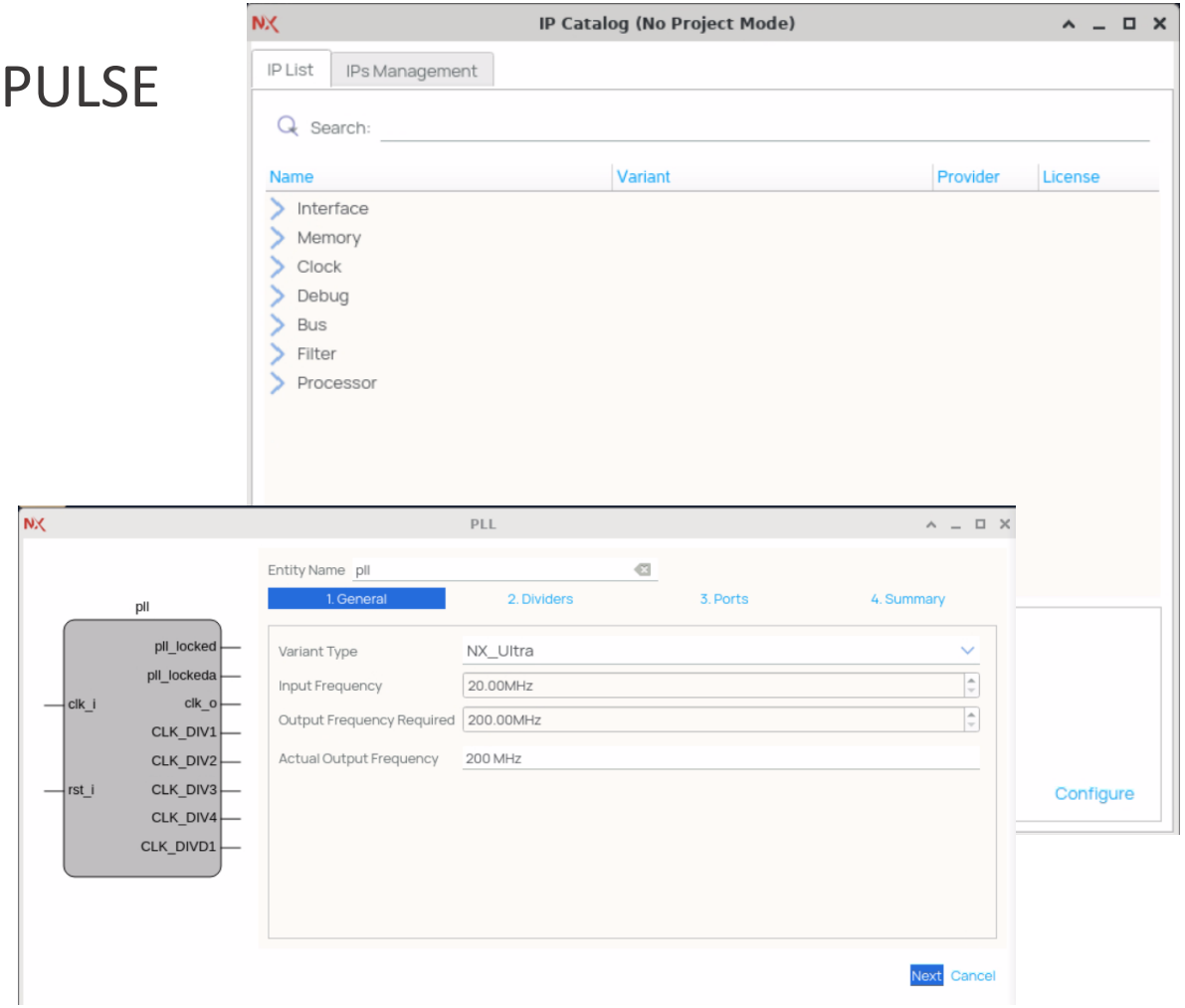
Software Tools Debugg



Software IPs

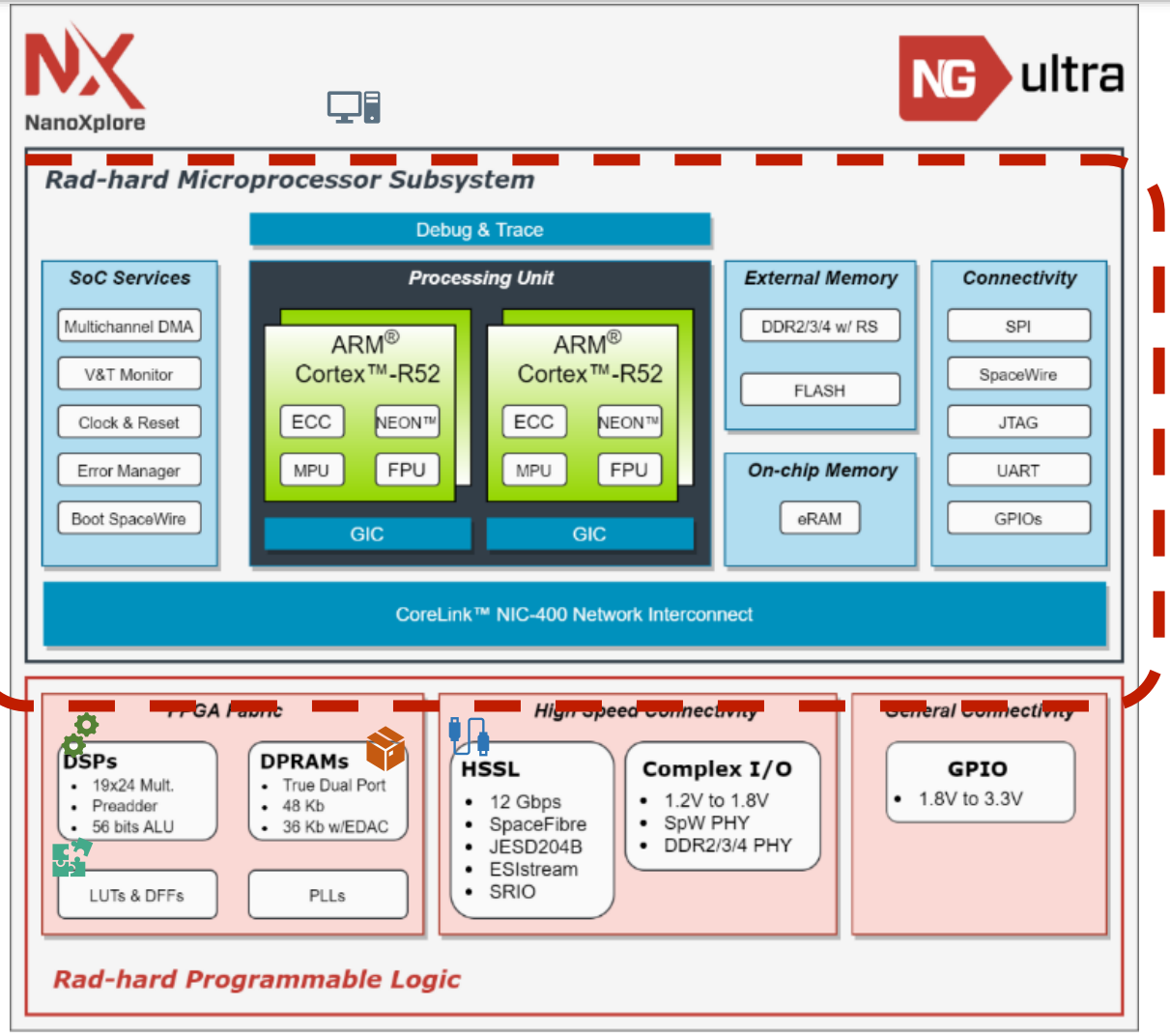
For NG-ULTRA

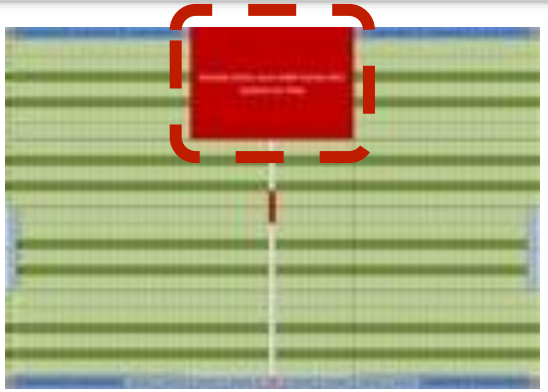
- nXcore is directly available in IMPULSE to import any available IPs
- DDR2 Controller
- Infrastructure IPs
- Filters
- Softcore
  - Leon3
  - RISC V (Q1 2024)
- HSSL protocols

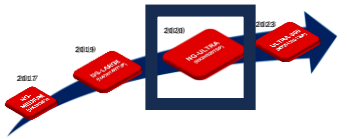


NG-ULTRA Overview

NG-ULTRA Overview



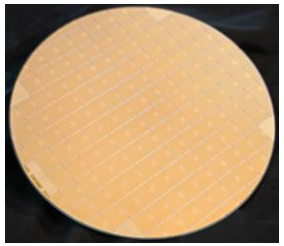




- Rad-Hardened By Design SRAM-based SoC FPGA
- Quadcore ARM R52 @ 600MHz each
- 537 KLUT density
- SpW & DDR 3&4 PHY hard-coded
- 32 HSSL @ 12 Gbps, compatible with:
  - SpaceFibre, JESD204B, ESIstream, SRIO
- BGA 1752 package

NG-ULTRA Supply Chain

life.augmented



- **Fab:** ST Crolles 28nm FD-SOI

- **Assembly flip chip**
- ST Rennes

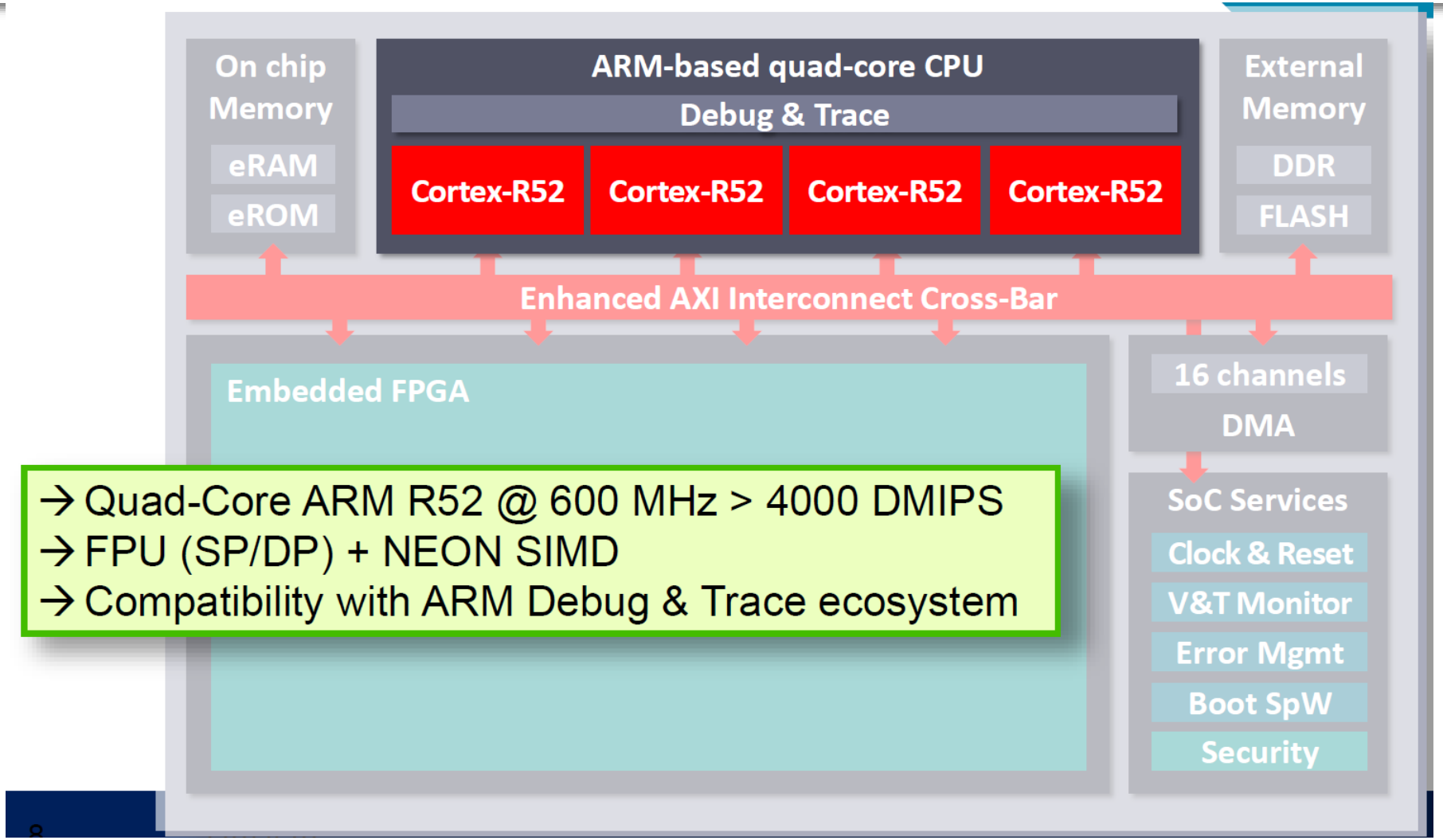
- **Testing**
- ST Grenoble

Fully European supply chain !

NG-ULTRA Overview

Device	NG-ULTRA
Capacity of modules	
Register	505 344
LUT-4	536 928
Carry	126 336
Embedded RAM	-
Core RAM Blocks (48K-bit)	672
Core RAM Bits (K = 1024)	32 256 K
Core Register File Blocks (32 x 18-bit)	2 632
Core Register File Bits	1 480 K
Embedded DSP	1 344
Clocks	50
Embedded Serial Link	
HSSL 12,5 Gbps, SERDES TX/RX (Supports several protocols including Space Fibre)	32
SpaceWire with codec 400Mbps	1
I/Os	
I/O Complex Banks	10 (34 I/Os per bank)
I/O Direct Banks	4 (24 I/Os per bank)
I/O Service Bank	1 (44 I/Os)
I/O DDR Bank	1 (204 I/Os)
I/O BScan Banks	2 (28 I/Os per bank)
User I/Os	740
I/O PHYSICAL INTERFACES	-
DDR/DDR2/DDR3	20
SpaceWire	20

NG-ULTRA Overview



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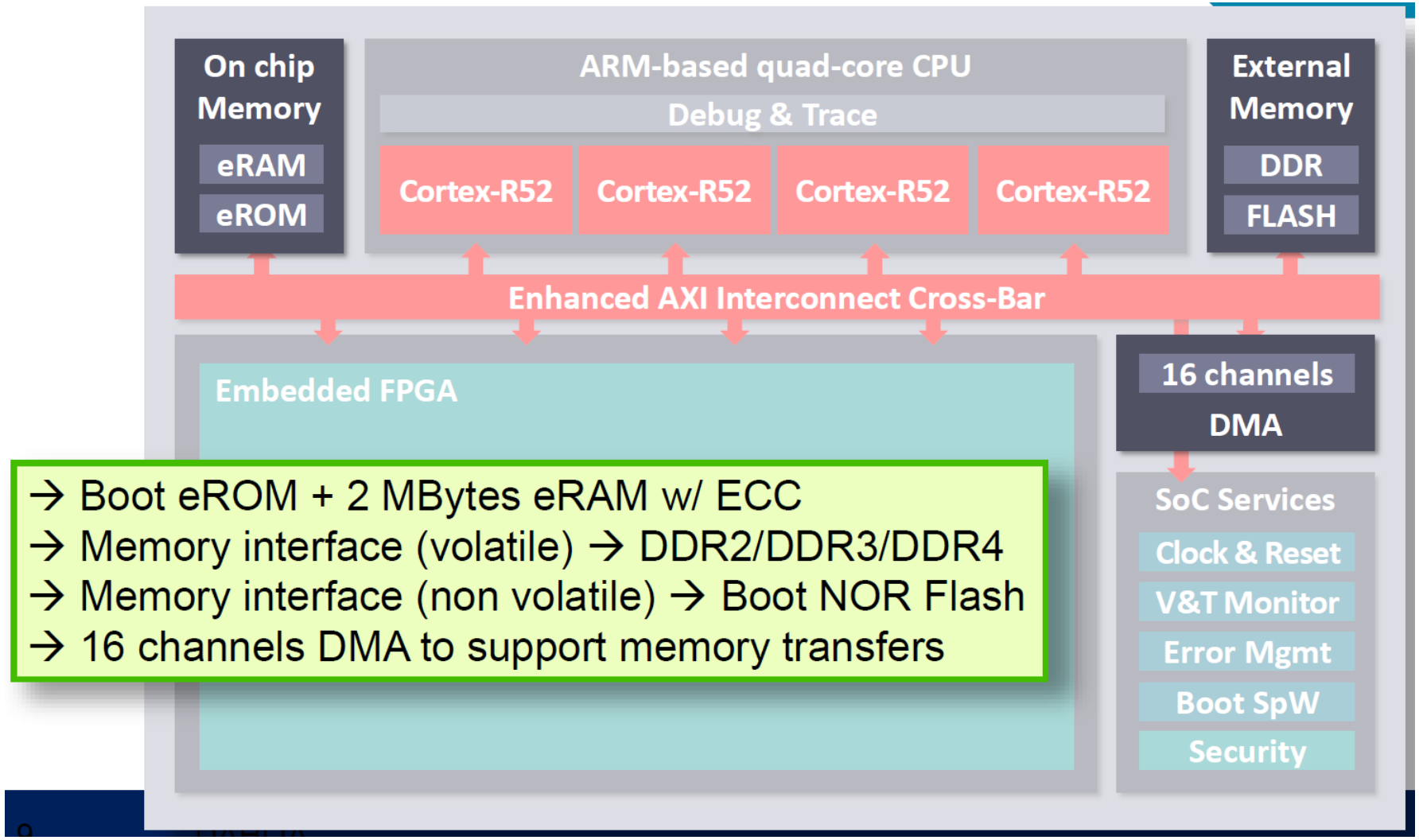
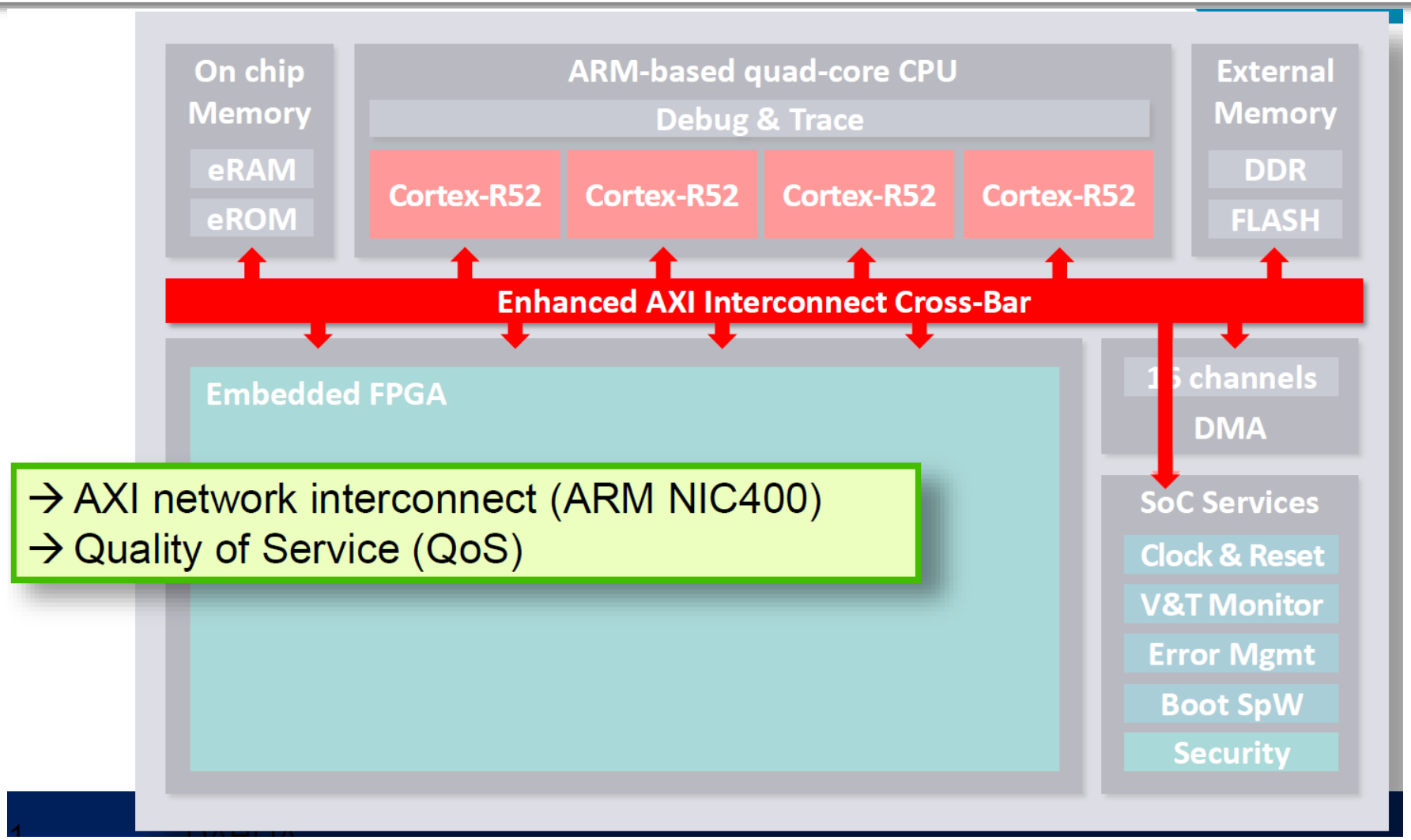


NG-ULTRA Overview



NG-ULTRA SdK

Board Support Package

- Generic build system for embedded software
  - Including Makefiles and generation instructions
  - Generic linker script
- Ready to use drivers
  - Flash, Clock & Reset, DMA, DDR, UART, eRAM, GIC…
  - ARM R52 init (crt0, handler, MPUs, stack…)
  - HAL and Helpers
- Example applications & demo

➢ Easy to use

NX Embedded Tools

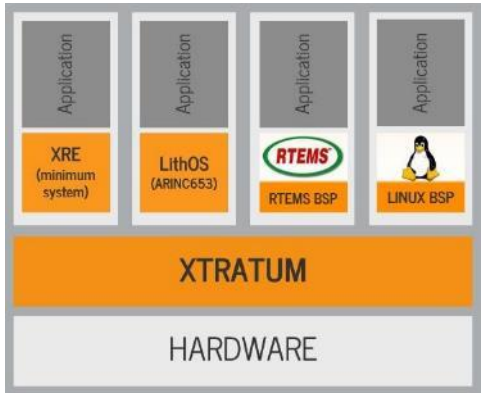
For NG-ULTRA

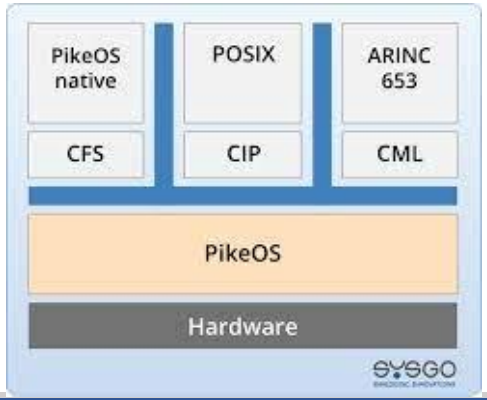
- ✓ Debugging facilities:
  - Lauterbach (debug & trace)
  - OpenOCD support
- ✓ Flash programmer
- ✓ Bitstream loader
- ✓ Memory dumper using DAP (debug access port)
- ✓ BL1 signer
- ✓ Read temperature sensor

➢ More on the way...

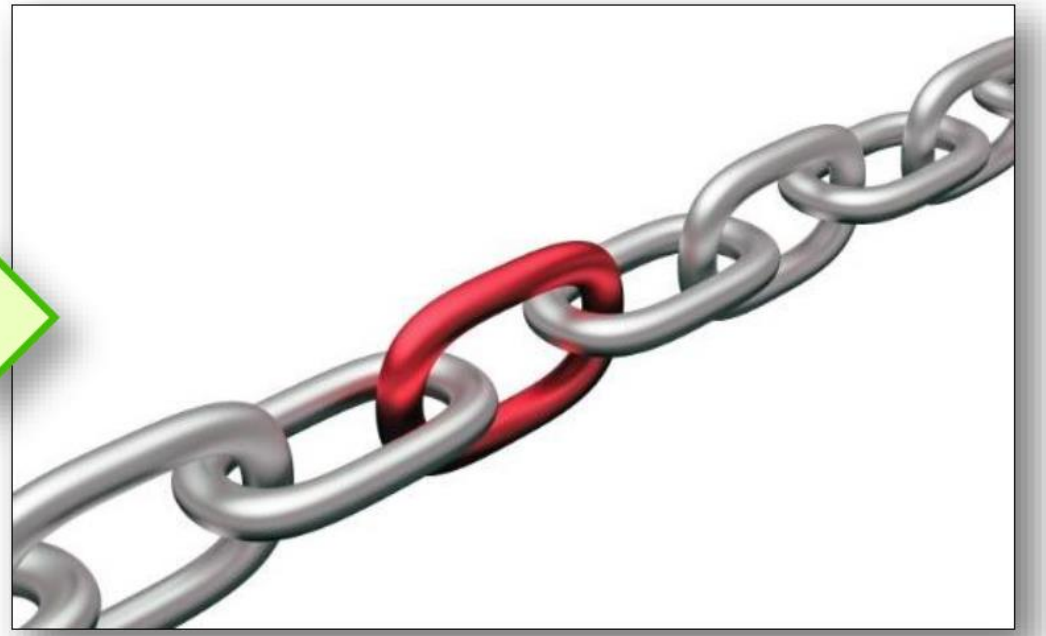
OS Supports

For NG-ULTRA





Radiation Performance – No Weakest Link (1)



Having a high performance and very robust component is not enough, because if it is associated to sensitive components (such as peripheral memories), the overall robustness will depends on the “weakest link”.
As an example, if you need to reboot each time you have an upset in a memory, this will drive the way you operate your processing module… this is an issue…

NG-Ultra solves this issue, since (1) it offers a robust Radiation Hardened By Design (RHBD) chip and (2) it provides unprecedented protection mechanisms for all of its peripheral components (Flash, DDR) allowing to use it without risk of introducing a “weakest link”.

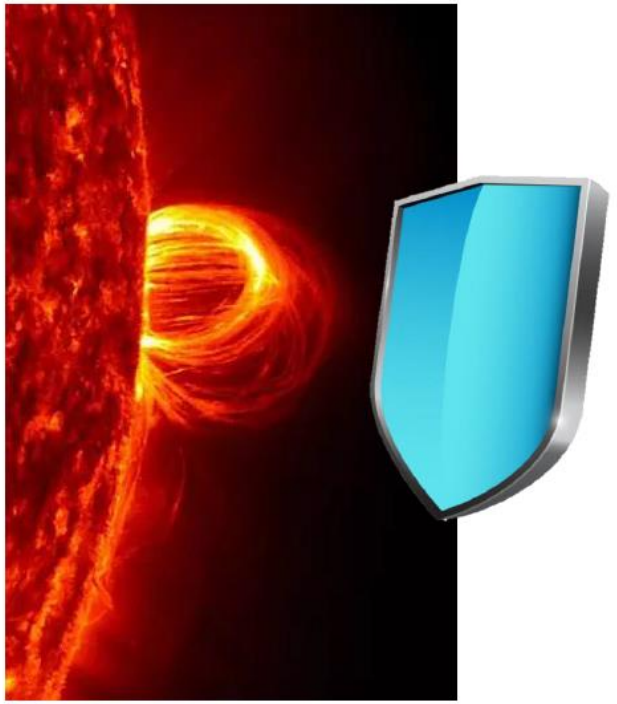
Radiation Performance – No Weakest Link (2)

NG-Ultra radiation robustness is… impressive !

- 28FDSOI technology intrinsically latch-up immune → **no SEL**
- NG-Ultra tested during 2 radiation campaigns → **no SEFI**
- Robustness confirmed (**no SEU, no SEFI**) on v1, v2 launched

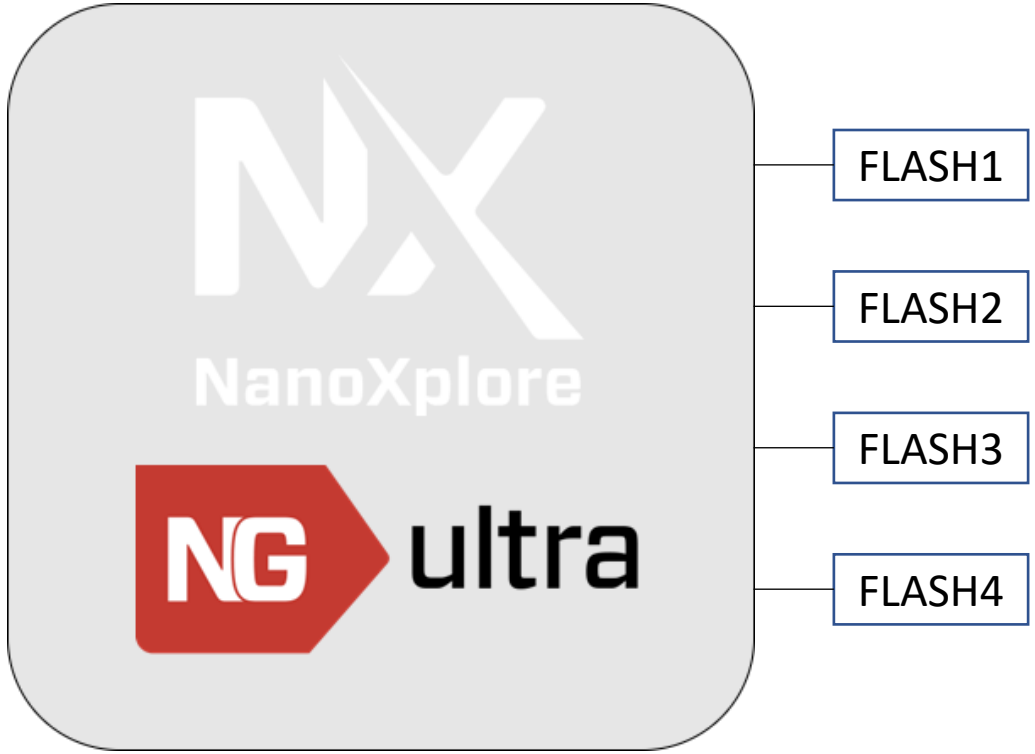
DDR memory protection → a game changer

- Supporting DDR2, DDR3 and **DDR4** / 8-bits & 16-bits devices
- Reed-Solomon for **SEU** high level of memory protection
- **Robustness against SEFI** up to the loss of two 16-bits devices



NG-ULTRA Configuration

FLASH Loading

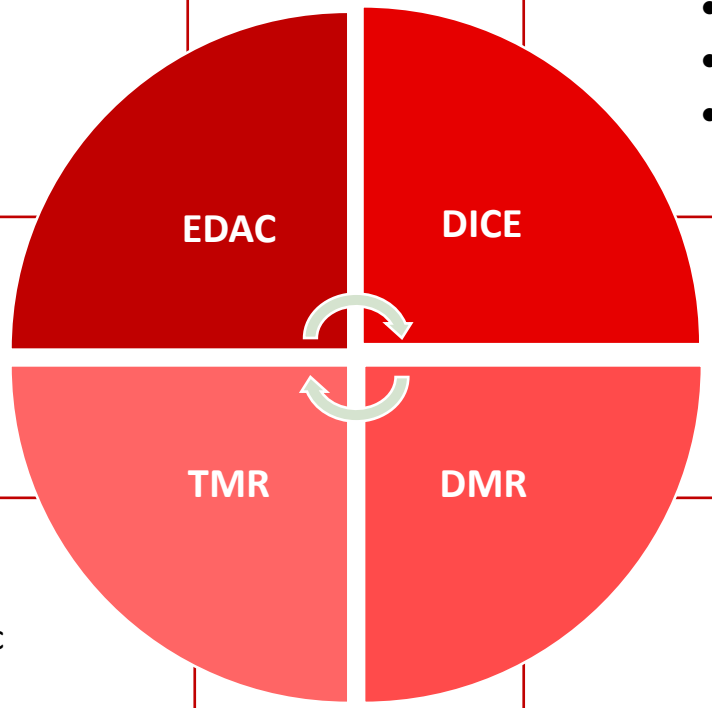


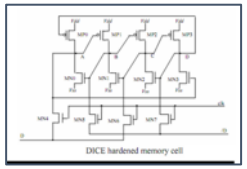
- 4 parallel SPI interfaces controlled by the boot loader
- FLASH mode:
  - SEQUENTIAL
  - TMR
- Parallel read
- NG-ULTRA performs the majority-voting
- The last memory can be used for an application purpose

28nm radiation hardening approach

- Register File
- DPRAM

- Cfg Memory
- User Register
- DFF





- Other digital: Rad Hard Logic Cells from ST 28nm

- ❿Clock Tree
- ❿Clock buffer
- ❿Matrix system

•Goal

No design mitigation techniques required by the FPGA user

Confirmed

28nm FD-SOI required less effort to develop the hardened cells compared to 65nm.

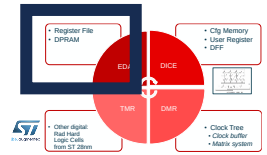
In addition, Embedded Configuration Memory Integrity Check (“**CMIC**”)

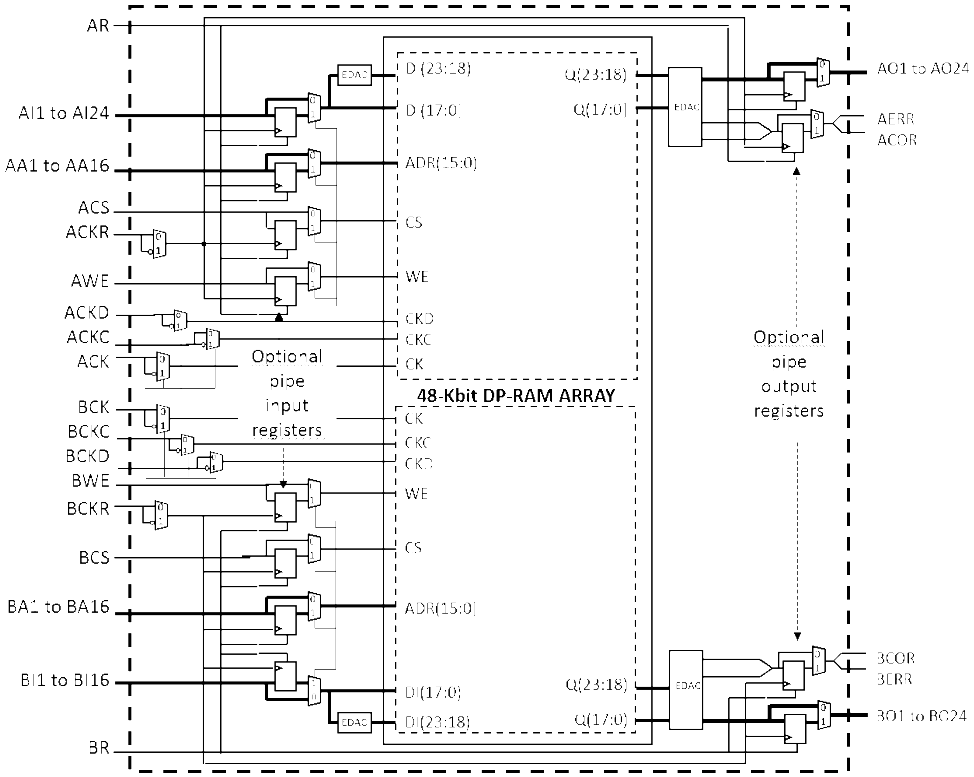
28nm radiation hardening approach: DPRAM

DPRAM Configurability:

- Optional pipe-line output register
- Initialization by bitstream
- **Embedded SECDEC EDAC**
  The ECC signature is computed during the write cycle and checked during the read cycle
- **Automatic repair mode**
  When enabled, the memory is corrected with the data/ ECC value when the correctable error is detected in the read cycle

With EDAC	Without EDAC
2048 x 1-bit	49152 x 1-bit
2048 x 2-bit	24576 x 2-bits
2048 x 6-bit	12288 x 4-bits
2048 x 9-bit	6144 x 8-bits
2048 x 18-bit	4096 x 12-bits
	2048 x 24-bits





RAM block simplify diagram

Radiation test sessions overview

NG-ULTRA FPGA Radiation test campaigns overview

2019

May Nov

- UCLouvain / HIF (BE)

DEMETER
Test chips

2020 **2021**

Dec Jun

UCLouvain / HIF (BE)

NG-ULTRA V1
1st prototypes

Parts thickness: 50, 70 µm
Tilt and roll possible

2023 **2023** **2023**

Apr Jun Sep

RADEF Jyväskylä (FI)

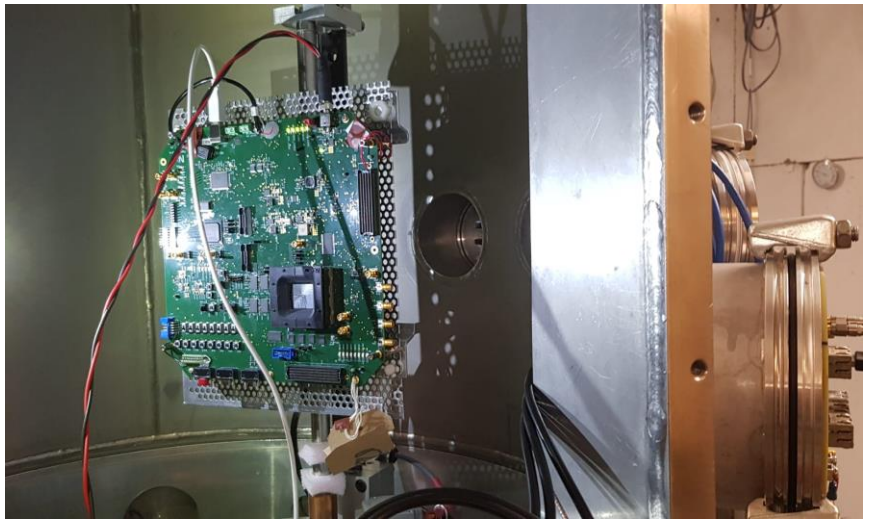
NG-ULTRA V2
final

Parts thickness: 100 µm
Tilt and roll not possible
or high energies

NG-ULTRA CMEM rad test results overview

Summary of the Configuration Memory (CMEM) test

- Test campaign: RADEF April-2023
- Number of bit in the configuration memory: **90.834.656**
- Bits Location: distributed in the whole chip
- Test Configuration:
  - Bitstream with Checkerboard (0101…..01)
  - CMIC (internal scrubber) : disabled
  - Voltage VDD_CORE -5% // nominal,
  - runs of 200 sec (shutter controlled, closed during configuration and readback)
- Number of samples: 3
- Flux: 5K ions/cm²/s
- Fluence reached : 1E+07 ions/cm²



0 errors in CMEM up to LET 62 MeV*cm²

✓Result consistent with the previous radiation test campaigns.

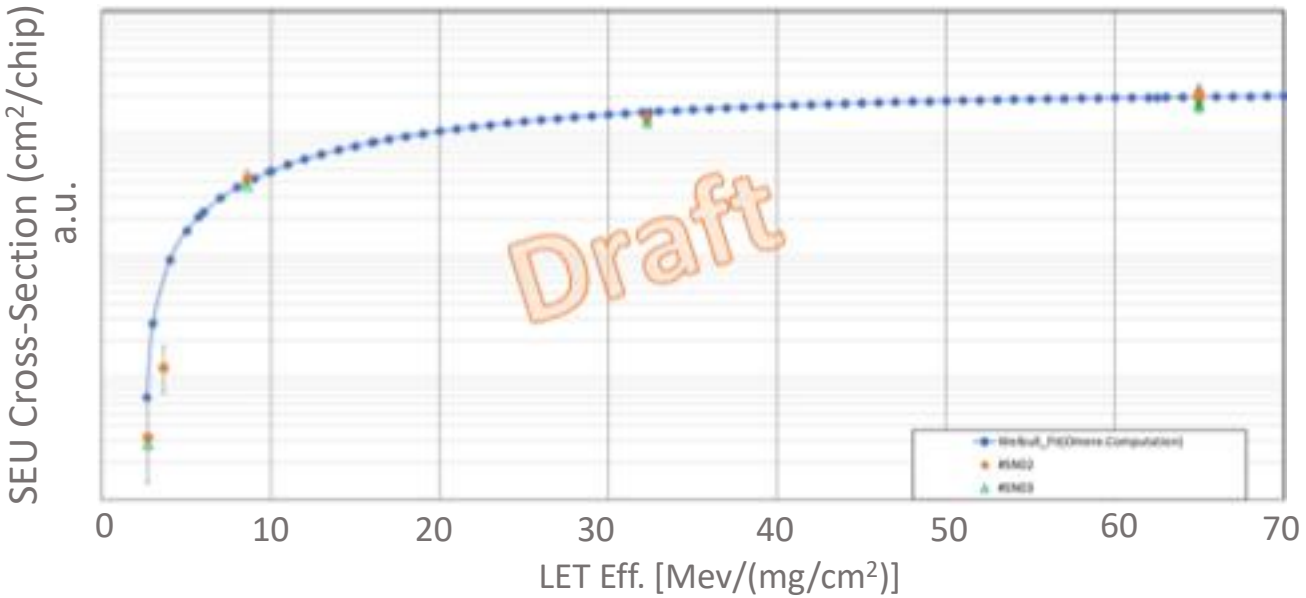
NG-ULTRA DPRAM rad test results overview

Summary of the DPRAM test

- Test campaign: RADEF April-2023
- Number of instances: **88 (672) 12%**
  4325376 bits
- Location: 2 rows of each lobe (6 / 5)
- Test Configuration:
  - **Bitstream1** : NOECC_2k x 24
  - **Bitstream2** : FAST_2k x 18
  - Voltage VDD_CORE -5% // nominal
- Number of samples: 2
- Flux: up to 15K ions/cm²/s for bitstream2
- Fluence reached : 1E+07 ions/cm²

No errors were detected using the ECC (even under flux : 15K ions/cm²/s)

Bitstream1 : NOECC_2k x 24 [3 runs]



✓ Results without ECC consistent with ST radiation data

Bitstream2 : FAST_2k x 18 [11 runs with **ECC enable**,
0 run returned error (count by ECC activation)]

NG-ULTRA DFF rad test results overview

Summary of the DFF tests

- Test campaign: RADEF April-2023
- Number of instances: **15k DFF (4%)**
- Bits Location: Lobe R3
- Test Configuration:
  - Bitstream : 15k stages, Window Shift Register (**WSR**)
  - Design frequency: 50 MHz / 80 MHz
  - Voltage VDD_CORE -5% // nominal,
- Number of samples: 2
- Flux: 10K ions/cm²/s
- Fluence reached : 1E+07 ions/cm²

0 errors detected during the campaign (up to LET 62 MeV*cm² /mg)

Radiation test next steps

- +1 more HI test session planned Q2 2024 at RADEF Jyväskylä (FI)
- +2 HI sessions planed dedicated to the SoC in 2023 at RADEF Jyväskylä (FI)
- +1 Proton test sessions being planned at PSI in 2024

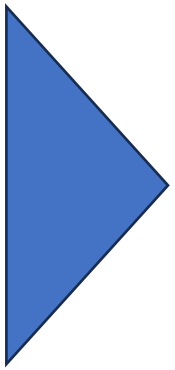
✓ **Radiation performances characterized so far are extremely strong !**

Parts available and Leadtime

- Parts available and leadtime
- Evaluation kit -> less then 1 month
- Industrial 0 to +85°c -> less than 1 month
- Military -40 to +125°c -> 1 to 3 months

Power consumption

- Illustrative power consumption of NG-ULTRA based on the following design:
- SoC 600MHz
- DFF 107k
- LUT 250k
- RAM 250
- Register file 232
- Clock 50MHz

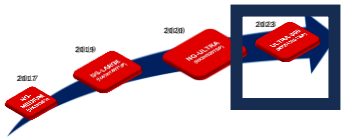


- Power consumption by rails @Tj 25°C
- 1V SoC dynamic = 1,5W
- 1V Fabric dynamic = 0,7W
- 1V Fabric static = 0,7W
- 1V8 IO = 0,1W
- 3V3 IO = 0,1W
- **Total = 3,1W**

ULTRA 300 Overview

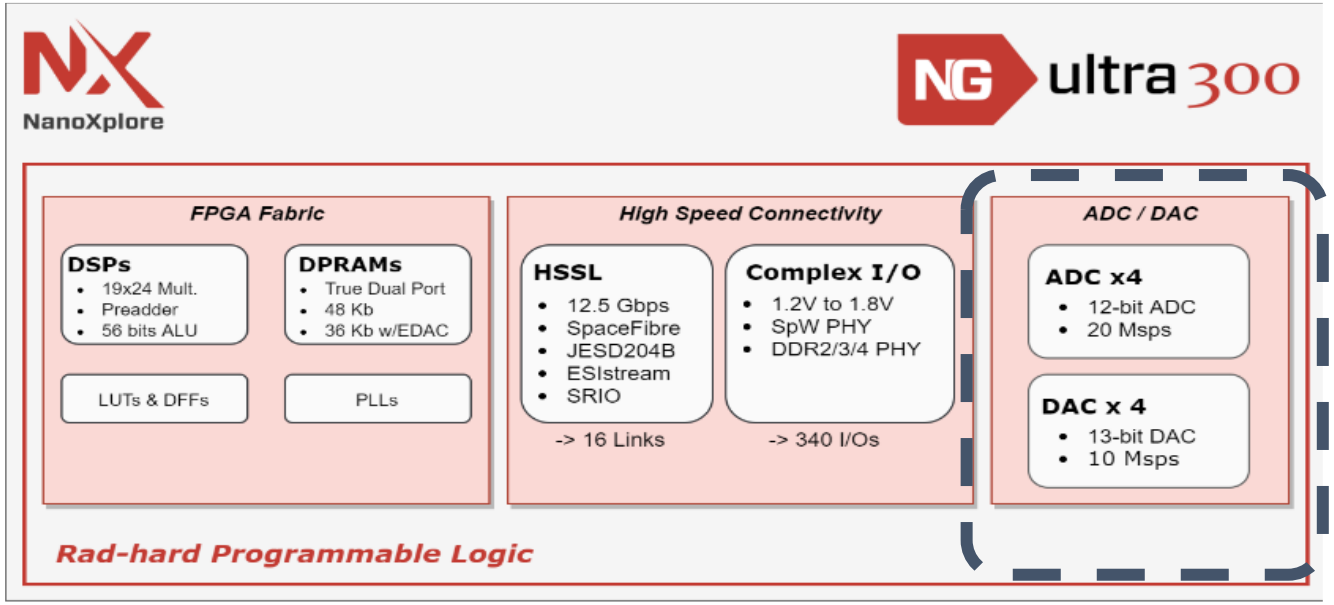
ULTRA 300 Overview

Device		Details	NX2H300TSA
Capacity - ASIC Gates	Rad Hard FPGA		**4 000 000**
Logic Modules		11x Tiles + 7CGBs	
Register		384DFF on 11rows	**273 408**
LUT-4		408LUT on 11rows	**290 496**
Carry		96CY on 11rows	**68 352**
Embedded RAM			**22Mb**
DPRAM		448BRAM * 48Kb	**21 504**
Core Register File		On 11 rows	**1 424**
Core Register File Bits		32*18bits	**807K Hardened**
Clocks / PLL			**50 / 6**
Additional Features	Rad Hard SOC		
SpaceWire PHY (8 IOBs)		2x/Complex IOBank	**20**
DDR3/4 PHY (11IOBs)		2x/Complex IOBank	**20**
DSP Blocks		From 7 rows	**896**
SpaceWire link I/F 430Mbps		CODEC	**1**
SERDES Tx/Rx 12,5Gbps (supporting several protocols such as Space Fibre)		4 Quad HSSL 12,5Gbps	**16**
Hard IP Processor core / SoC			**NO**
ADC		12-bit ADC, 10Msps	**1**
DAC		13-bit DAC, 10Msps	**1**
Design Security			**YES**
Inputs / Outputs	I/O		**547 I/Os**
Complex I/O bank		VIO 1,2 – 1,5 – 1,8V	**10 x 34 I/Os**
Simple I/O bank		VIO 1,8 – 2,5 – 3,3V	**6 x 24 I/Os + 1 x 16 I/Os**
Packages - User I/Os	PKG		
FF484 organic		27*27 mm / 1 mm	**239 I/Os (TBC)**
FF1152 organic		35*35 mm / 1 mm	**547 I/Os (TBC)**

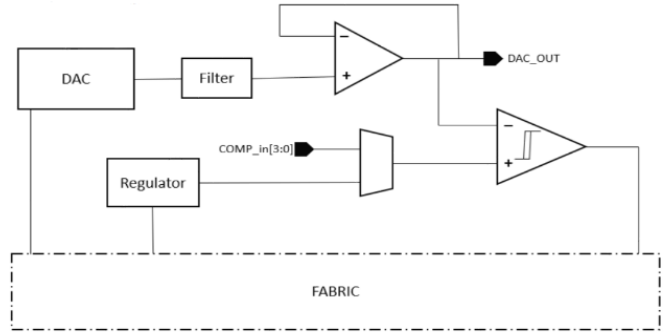


- 290 KLUT density
- 16 HSSL @ 12 Gbps, compatible with:
  - SpaceFibre, JESD204B, ESIstream, SRIO
- ADC and DAC
- BGA 484 and BGA 1152 package

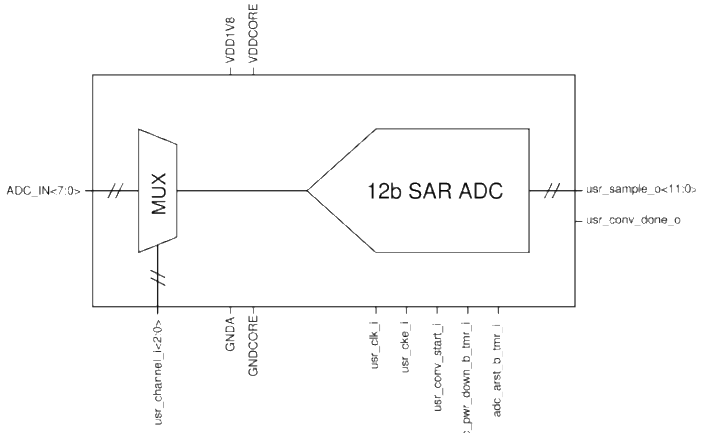
ULTRA 300 Overview



13—bit DAC, 1-10 MSPS



12—bit ADC, 1-10 MSPS up to 8 inputs



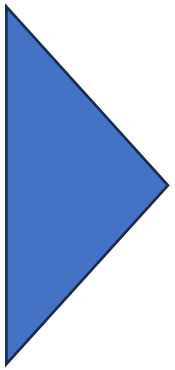
Radiation test

- 2 HI test session planned in 2024 at RADEF Jyväskylä (FI)
- +1 Proton test sessions being planned at PSI in 2024

✓ **Same blocks as NG-ULTRA -> should have the same radiation performance**

Power consomption

- Illustrative power consumption of ULTRA300 based on the following **resource intensive** design:
- DFF 107k
- LUT 250k
- RAM 250
- Register file 232
- Clock 50MHz



- Power consumption by rails @Tj 25°C
- 1V Fabric dynamic = 0,7W
- 1V Fabric static = 0,5W
- 1V8 IO = 0,1W
- 3V3 IO = 0,1W
- **Total = 1,4W**

Parts available and Leadtime

- Parts available and leadtime
- IMPULSE -> now
- Evaluation kit -> Q1 2024
- Industrial 0 to +85°c -> Q1 2024
- Military -40 to +125°c -> Q3 2024

- Any prototyping can be done on NG-ULTRA and then port on ULTRA 300

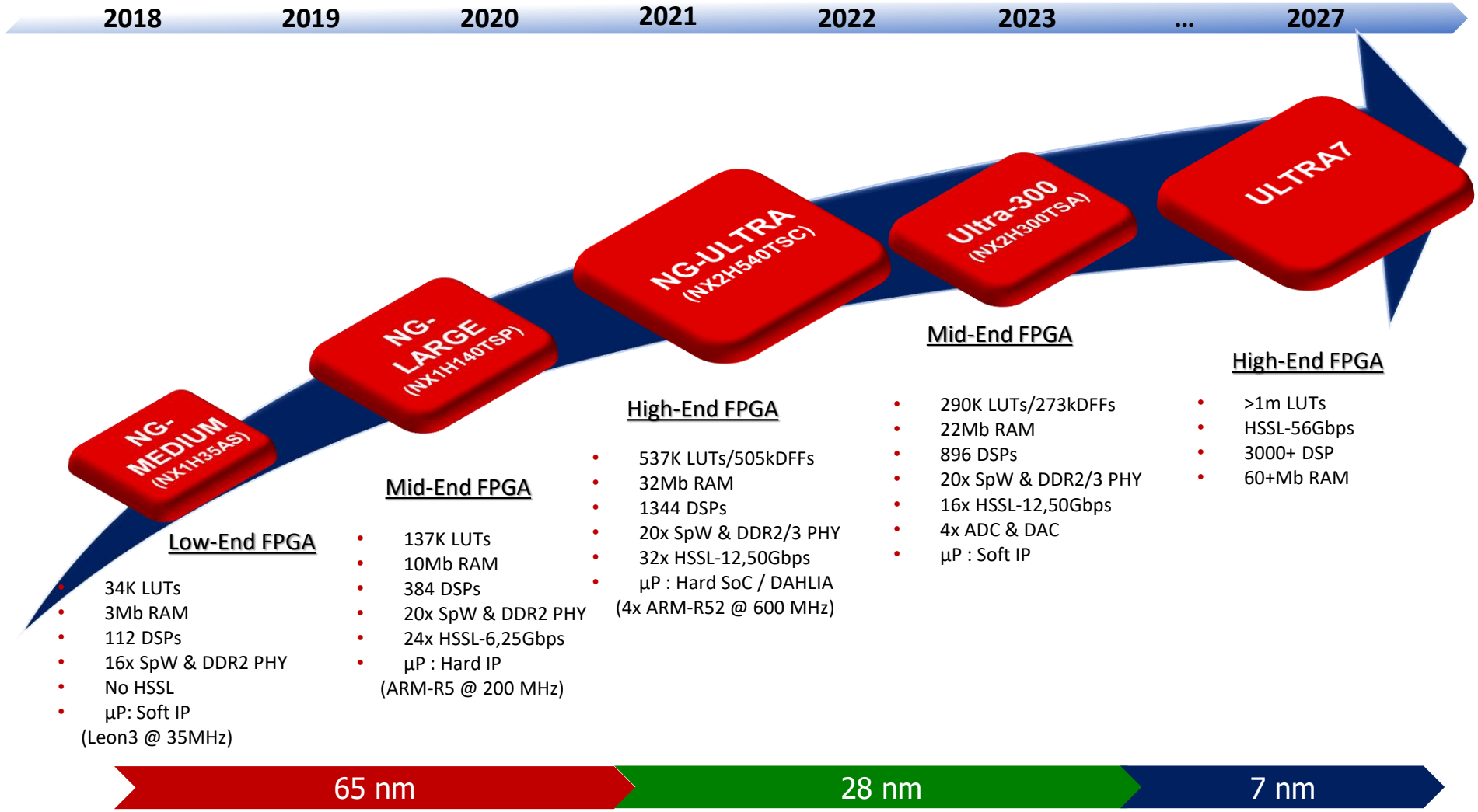
Customers

- And others to come

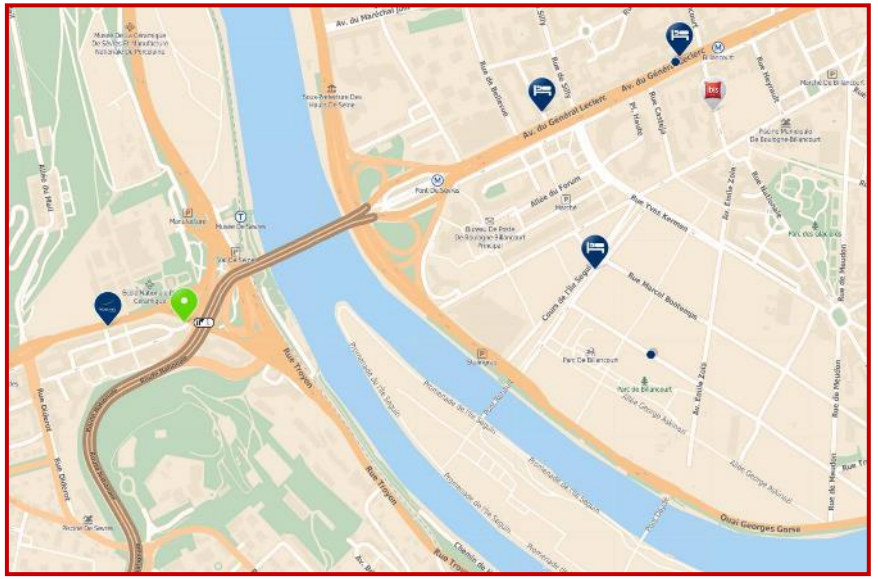
NanoXplore

Next?

Rad-Hard FPGA Roadmap



Thank you!



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