3rd CERN System-on-Chip Workshop

Report of Contributions

https://indico.cern.ch/e/1253805

Contribution ID: **1** Type: **not specified**

NanoXplore - Introducing NG-ULTRA and ULTRA300 Rad-Hard SoC FPGA for Hi-Rel CERN Application Requirements

Monday, 2 October 2023 09:40 (1 hour)

NanoXplore is introducing a state-of-the-art radiation hardened SoC FPGA portfolio offering unprecedented reliability performance. The NG-ULTRA is the first fully radiation hardened SoC FPGA in 28nm FD-SOI based on a quad core ARM R52 processor. The NG-ULTRA and ULTRA300 are the perfect candidates to address the most challenging Hi-Rel application requirements with a simple and cost-effective solution.
These components are fully based on a competitive European supply chain and already used in many Hi-Rel applications from space to ground environment.

Presenter: LEPAPE, Edouard (NanoXplore)

Session Classification: Vendor Session #1.A

Contribution ID: **3** Type: **not specified**

AMD-Xilinx (by Avnet Silica) : From SoC to SoM, AMD and AVNET Solutions

Monday, 2 October 2023 13:30 (1 hour)

XILINX became AMD about 2 years ago: the FPGA/SoC strategy has been strengthened and innovation goes on···Following 16nm technology and the Zynq US+ SoC, Versal Adaptive SoCs now complete the AMD offering with 7nm products. This presentation will go through the different Versal Adaptive SoC series with a clear status of their availability and an overview of the roadmap. In addition to SoCs, AMD released their first SoM with Kria, based on Zynq US+. This is the first member of this new AMD family : More coming soon!
As a XILINX (now AMD) partner for more than 35 years, AVNET has been collaborating and designing SoMs for more than 10 years, starting from Zynq-7000 to Zynq US+ MPSoC/RFSoC. AVNET now extends their portfolio with Versal AI Edge. This session is a great opportunity to provide a general update about the main features of AVNET SoMs : their availability, their longevity and the use of popular global standard specification in some products.

Presenter: DONZEL, Gregory (Avnet SIlica)

Session Classification: Vendor Session #1.B

Contribution ID: **4** Type: **not specified**

Microchip : PolarFire SoC A Different and Unique SoC Solution

Monday, 2 October 2023 14:30 (1 hour)

With many acquisitions over the last 10 years, MICROCHIP has become a broadline semiconductor manufacturer. After acquiring MICROSEMI (that acquired ACTEL before), MICROCHIP added FPGAs and SoCs in its portfolio. MICROCHIP has always had a good reputation for the very long longevity of their products. In addition to this key asset, they bring other significant differentiators to the FPGA/SoC market with the PolarFire SoC. This session aims at detailing them and at giving a status of the availability of these RISC-V-based SoCs.

Presenter: DONZEL, Gregory (Avnet Silica)

Session Classification: Vendor Session #1.B

Contribution ID: **5** Type: **not specified**

Enclustra - Efficient FPGA SoC-based Signal Processing (DSP) up to GS/s

Monday, 2 October 2023 15:50 (30 minutes)

Explore efficient FPGA SoC-based signal processing for Giga sample per second (GS/s) rates. Tackle traditional DSP design challenges, address sample rates surpassing clock frequencies through Parallel DSP, and emphasize bit-true design. Discover how Enclustra's fixed-point & bit-true Python & HDL libraries offer a streamlined, step-by-step design and co-simulation process, enabling high-speed, accurate signal processing.

Presenter: BRUENDLER, Oliver (Enclustra)

Session Classification: Vendor Session #1.B

Contribution ID: **6** Type: **not specified**

Trenz Electronic - Advanced Solutions

Monday, 2 October 2023 16:50 (1 hour)

For many years, Trenz has been at the forefront of specializing in the development and production of diverse modular systems, offering a wide array of benefits across numerous application domains. Our products accelerates end-device development, streamlines prototyping, and diminishes the skill demands placed on your hardware design team. One of the most important advantages is the reduction of the total financial costs invested in product development. These advantages and more are made possible through the utilization of Trenz System-on-Modules (SoMs).
Today, we invite you to delve into our world as we unfold the story of Trenz, shedding light on the comprehensive suite of services we provide to our valued clients. We will also spotlight some of our flagship products and discuss our in-house manufacturing capabilities. Additionally, we will explore our ability to customize solutions tailored to the unique requirements of our customers. Furthermore, stay tuned as we unveil our latest innovations and product releases from the past few years, like AMD Versal evaluation platform. Welcome to the world of Trenz, where innovation meets your needs.

Presenter: YUNITSKI, Vadim (Trenz Electronic)

Session Classification: Vendor Session #1.B

Contribution ID: **7** Type: **not specified**

Topic - Increase Development Efficiency and Quality using System-on-Modules with SOC Technology

Tuesday, 3 October 2023 09:30 (1 hour)

Over the years, the complexity of circuits around system-on-chips has been growing rapidly. Apart from that, the core functionality offered by the SOCs also grew exponentially. When you look at typical applications using SOCs, you see a balance between processing performance, communication bandwidth and storage capabilities. The use of system-on-modules is helping to reduce the design-in complexity of these SOCs as well as the design-in time. The focus of TOPIC in providing SOMs are related to specific application domains, life-cycle-management issues and solving typical system-level problems like load steps and thermal management. Apart from basic board design related aspects, quite some effort is spent on making the SOMs support specific functionality like lidar, radar, ultrasound, photonics as well as synchronized networked collaboration. In this context precision timing is also a relevant subject.
Please join our presentation on the strategy of TOPIC on our offered SOM solutions, illustrated by customer application examples as well as the next-generation SOM where your input is relevant.

Presenter: VAN DEN HEUVEL, Dirk (Topic)

Session Classification: Vendor Session #2.A

Contribution ID: **8** Type: **not specified**

Vendor Exhibition #2 (with coffee&tea)

Tuesday, 3 October 2023 10:30 (1h 30m)

Presenter: ALL VENDORS

Session Classification: Vendor Exhibition #2

Contribution ID: **9** Type: **not specified**

Nvidia - Optimizing Data Center Efficiency: Selected Use Cases for DPUs

Wednesday, 4 October 2023 13:30 (1 hour)

In the dynamic landscape of modern data centers, efficiency, performance, and security are paramount. NVIDIA Data Processing Units (DPUs) have emerged as game-changers in addressing these critical challenges. This presentation dives into the transformative world of NVIDIA DPUs, unveiling how these specialized hardware components are reshaping data center operations.
Throughout the presentation, we will explore the core functionalities of NVIDIA DPUs, their integration with GPUs, and their ability to accelerate networking, storage, and security tasks. We will delve into real-world use cases where DPUs have delivered tangible benefits, from reducing latency in high-speed networks to enhancing data storage capabilities. Furthermore, we will examine how NVIDIA DPUs contribute to overall data center efficiency by offloading tasks from CPUs, thus freeing up valuable compute resources for mission-critical workloads.

Presenter: Dr KALCHER, Sebastian (Nvidia)

Session Classification: Vendor Session #3

Contribution ID: **10** Type: **not specified**

Demonstrating Software Acceleration in FPGA Fabric: Deploying C/C++ Code with AMD Vitis HLS on a ZynqUS+ Platform

Tuesday, 3 October 2023 13:30 (1 hour)

Image processing algorithms as well as many other algorithms can often not be deployed on classical SoCs with the required performance.
A Sobel filter, applied to a 4k video stream, might bring embedded processors as well as normal desktop PCs to its limit.
With Vitis HLS algorithms written in C/C++ can be deployed on FPGA logic.
In this presentation a Sobel filter will be running in the FPGA fabric and benchmarked against the software variant.
The run times and the acceleration factor will be compared and discussed.

Presenter: HOEFLE, Marco (Avnet SIlica)

Session Classification: Vendor Session #2.B

Contribution ID: **11** Type: **not specified**

Introduction to Projects' Session

Tuesday, 3 October 2023 14:30 (20 minutes)

Presenter: SPIWOKS, Ralf (CERN)

Session Classification: Project Session #1

Contribution ID: **12** Type: **not specified**

The Beam Instrumentation PiXeL (BIPXL) MPSoC Readout System

Tuesday, 3 October 2023 14:50 (30 minutes)

The Beam Instrumentation group at CERN utilizes Timepix3 hybrid pixel detectors for various applications, such as measuring the transverse beam profile through the Beam Gas Ionization profile monitor (BGI) and detecting beam losses with the Beam Loss Monitor (BLM). To effectively handle events and to control and monitor these detectors, the Beam Instrumentation PiXeL (BIPXL) MPSoC Readout system has been developed based on the Zynq UltraScale+ MPSoC. This versatile platform allows the connection of one or more Timepix3 detectors, several trigger sources and one or more external computers.
This presentation will first give an overview of these types of beam profile monitors as well as an overall description of the BIPXL readout system that is now operational in the PS. After this, specific parts of the implemented architecture will be explained like the use of a REST API over HTTP for data exchanging. Lastly, we will introduce a potential system update using SoM technology.

Presenter: CABRERA CASTELLANO, Gabriela (CERN)

Session Classification: Project Session #1

Contribution ID: **13** Type: **not specified**

RFSoC-based Development for HL-LHC Beam Position Monitors

Tuesday, 3 October 2023 15:40 (30 minutes)

The future HL-LHC Beam Position Monitor (BPM) data acquisition system to be installed near the ATLAS and CMS experiments is an application with demanding digitization and signal processing requirements. The architecture under study is based on an RF System-on-Chip from Xilinx, which allows fast RF conversion and high-performance digital processing to be integrated in a single chip for multiple channels. After an introduction to the project and to the RFSoC characteristics, this talk presents the on-going developments based on this platform in the Beam Instrumentation group at CERN. Particular focus is given to the development of a high-speed 8-channel raw data acquisition system based on an evaluation board, mentioning also the strategy to integrate the setting, control and data acquisition within CERN's accelerator control system.

Presenters: DEGL'INNOCENTI, Irene (CERN); BOCCARDI, Andrea (CERN); BALCI, Elif (CERN); GONZALEZ BERGES, Manuel (CERN); KRUPA, Michal (CERN); JACKSON, Stephen (CERN)

Session Classification: Project Session #1

Contribution ID: **14** Type: **not specified**

The X2O ATCA IPMC and Control Solution: an Update

Tuesday, 3 October 2023 16:10 (30 minutes)

The presentation will discuss the latest updates of the X2O platform for the upcoming Phase-2 upgrade. The X2O platform is a modular system in ATCA standard that includes hardware, firmware and software solutions. Main updates of the X2O platform include:
Migration to the KRIA SoM (Ultrascale+ family) as a system controller and IPMC host within the power module (rev.3). Adaptations for VU13P FPGA module and 30-cage QSFP optical module. New features in KRIA SoM firmware and software such as 10G Ethernet, fast custom JTAG-DMA core, custom IPMC slaves, custom I2C master for IPMB transfers. New IPMC version that is running as an application on SoM KRIA within CentOS 8/AlmaLinux 8. Initial version of X2O board plugin as a control software solution based on SWATCH framework.
The X2O platform will be used for L1 Trigger subsystems: EMTF, OMTF, GEM, GMT and also in the DAQ upgrade of the CSC subsystem.

Presenters: GRESHILOV, Aleksei (Rice University (US)); MADORSKY, Alexander (University of Florida (US)); BACHTIS, Michail (University of California Los Angeles (US))

Session Classification: Project Session #1

Contribution ID: **15** Type: **not specified**

A SoC Development Platform Based on SoCMake Build System and SystemRDL Description

Tuesday, 3 October 2023 16:40 (30 minutes)

SoCMake is a build system for hardware designs. SoCMake covers all the segments of SoC design, eliminating the need for additional build systems within a project.
The Focus of SoCMake is on packaging hardware IP blocks in self-contained repositories that can easily be fetched and versioned with the CPM package manager. SoCMake uses CMake interface libraries to represent hardware IP blocks, using CMake linking dependencies between IP blocks can be described. SoCMake provides support for a number of EDA tools which makes it easy to run RTL simulations, synthesis, implementation, documentation generation etc.
Using CMake for a hardware build system has the advantage of inbuilt C/C++ support, making it easy to cross-compile applications for the target CPU and generate files for loading the system-on-chip memory during simulation or boot loading in real hardware.
Support for C++ also provides an easy compilation of SystemC-UVM verification environments.
As a demonstrator of a SoCMake build system 2 SoC designs are provided based on Ibex and Veer-EL2 cores.
The components of provided SoC examples are by majority automatically generated from the SystemRDL description.
Some of the generated components are:
- Interconnection and top module generator
- HAL CPP libraries
- Linker script for SoC applications
- HTML documentation of the full SoC and its IP blocks
- Peripheral IP register file with the configurable bus (APB, AXI, AVALON)
Provided are several independent peripheral IP blocks used in provided SoC examples. They are packaged with documentation and SystemC-UVM verification environment, generated from the SystemRDL description.

Presenter: PEJASINOVIC, Risto (University of Novi Sad (RS))

Session Classification: Project Session #1

Contribution ID: **16** Type: **not specified**

Towards Modern Heterogenous Code Development for SoC: Application to CROME System

Tuesday, 3 October 2023 17:10 (30 minutes)

SoC projects face the challenges of maintaining a manageable and comprehensible codebase that spans a wide range of technologies. Efficient use of resources is of paramount importance in order to enable small teams to lead such projects to success.
This presentation will discuss the modern approach used in the CROME project not only to face these challenges, but also to ensure that improved processes are enforced. Some aspects of this approach are implemented through automatization, such as continuous integration, continuous testing, but also thanks to more efficient use of documentation and peer review.
CI pipelines automate builds and tests, accelerating development cycles and enabling early bug detection, as well as straightforward build process. Utilizing tools like cocotb and GHDL, we conduct efficient hardware verification, complemented by formal verification techniques. This approach improves code reliability, minimizes regressions. Comprehensive documentation facilitates knowledge transfer and collaboration, reducing the learning curve. A well-defined project structure promotes code maintainability and scalability, fostering effective teamwork and code reuse. All of these aspects are great at face value, but they also empower newcomers to start sooner playing with the code, thanks to a lower barrier to entry.
In summary, embracing newer technologies and sticking to good practices help to achieve a maintainable and developer-friendly codebase, especially in heterogeneous systems such as the Zynq platform. These practices empower developers, simplify development, and ensure code quality.

Presenter: LAFORGE, Clyde (CERN)

Session Classification: Project Session #1

Contribution ID: **17** Type: **not specified**

Gateware and Software Architecture for the DI/OT Project

Wednesday, 4 October 2023 14:30 (30 minutes)

Distributed I/O Tier is a versatile hardware platform for custom electronics in HL-LHC applications within the Accelerators and Technology Sector. This platform exists in two variants: high-performance (non-radiation-tolerant) and radiation-tolerant. The former incorporates the System Board (a.k.a. the crate controller), featuring the Zynq Ultrascale+ MPSoC. This MPSoC runs Linux and provides various platform management services, while also leaving the majority of its resources for the users to implement application-specific logic and software services.
During the presentation we will discuss the unified gateware and software architecture for the DI/OT MPSoC. This design facilitates the coexistence of user-defined logic and software with platform management functionalities. We will introduce technical solutions for services such as crate configuration discovery, remote reprogramming of crate components and other essential services. In addition, we will share our experience in adopting a centrally supported Linux distribution for SoCs, made available through the FECOS project.

Presenters: ARIAS VAZQUEZ, Alen (CERN); GUNCIC, Bernard; AMOIRIDIS, Vasileios (CERN)

Session Classification: Project Session #2

Contribution ID: **18** Type: **not specified**

Bare-metal Programming on Zynq UltraScale+ for the FGC4 Power Converter Controller

Wednesday, 4 October 2023 15:00 (30 minutes)

The context:
The Electrical Power Converters group (SY-EPC) is currently in the process of developing the latest iteration of its power converter controller, known as FGC4. It is an embedded device, based on the DI/OT hardware platform, used to control, monitor, and diagnose power converters. The primary control algorithm runs on the system board featuring Xilinx's Zynq UltraScale+ SoC. The algorithm demands a hard real-time environment with absolute predictability in execution time to ensure stable and accurate feedback control. To meet the bandwidth requirements of upcoming power converter designs, it needs to be run on the more powerful, Cortex-A53 cores of the SoC, rather than the real-time-optimized R5 core, as the latter is simply not fast enough.
We have determined that the Linux operating system, despite extensive effort to tune it, fails to satisfy these specific constraints of determinism. However, we are aware that the remaining software components (such as the communication stack, configuration, reprogramming, etc.), can be much more effectively implemented within a standard Linux environment.
The talk:
To address this challenge, we have decided to adopt an asymmetric multiprocessing (AMP) solution. Under this approach, we allocate two out of the four A53 CPU cores to run a regular Linux kernel, while the remaining two cores are dedicated to executing bare-metal software without relying on any operating system. During our presentation we will share the research and benchmarking that lead us to selecting this particular approach. Moreover, we will delve into technical details of implementation, including: compilation of bare-metal code with Xilinx BSP, cache, MMU, and IRQ configuration, loading of the bare-metal binary, communication with the Linux application, and monitoring, reloading and protecting the system using a universal, project-independent bare-metal bootloader written specifically to implement the aforementioned features.

Presenters: ZIELINSKI, Dariusz Jakub (CERN); CEJP, Martin (CERN)

Session Classification: Project Session #2

Contribution ID: **19** Type: **not specified**

Update on SoCs in ATLAS Detector Controls: The Embedded Monitoring Processor as Example

Wednesday, 4 October 2023 15:50 (30 minutes)

SoCs are getting adopted extensively by ATLAS systems for the local control and monitoring of their back-end electronics due to their flexibility towards the hardware through the programmable logic but also the convenience provided for higher level software within the Linux platform running on the processing system. The interface to detector control back-end applications is achieved by embedding the industry standard OPC-UA protocol into the processing system, for which development and maintenance is facilitated by the OPC-UA server generation framework quasar. A prominent example is the Embedded Monitoring Processor (EMP), a common electronics platform for detector controls, exploiting the flexibility of SoCs to interface on-detector lpGBT links to the experiments controls network via dedicated quasar servers.
This contribution shortly reminds about the use of SoCs within the ATLAS DCS along with giving updates on the quasar framework. Thereafter it focuses on the EMP by presenting the current status and selected developments for this Zynq-based device.

Presenter: ECKER, Dominic (Bergische Universitaet Wuppertal (DE))

Session Classification: Project Session #2

Contribution ID: **21** Type: **not specified**

A Versatile Data Acquisition System for Silicon Pixel Detectors Prototyping (CARIBOU)

Wednesday, 4 October 2023 16:20 (30 minutes)

Caribou is a versatile data acquisition system used by multiple collaborative frameworks (CERN EP R&D, RD50, AIDAinnova) for the qualification of novel silicon pixel detector prototypes. The system is built around a common hardware, firmware and software base shared accross different projects, thereby drastically reducing the development effort and costs. The current version consists of a custom Control and Readout (CaR) board and a commercial Xilinx Zynq 7000 series Sytem-on-Chip (SoC) platform. The CaR board provides a hardware environment featuring various services such as powering,slow-control and high-speed data links that can be used by the target detector prototype. On the other hand, the SoC platform is based on a ZC706 evaluation board running a fully featured Yocto-based Linux distribution (Poky) and a custom data acquisition software (Peary). Finally, migration to a Zynq UltraScale+ architecture is ongoing with the additional objective of merging the SoC and the CaR board into a single hardware platform. This talk describes the current Caribou system architecture, its capabilities, examples of projects where it has been used, and the foreseen system upgrade.

Presenter: OTARID, Younes (CERN)

Session Classification: Project Session #2

Contribution ID: **22** Type: **not specified**

SoC Integration and Usage in the gFEX Hardware Trigger in ATLAS

Wednesday, 4 October 2023 16:50 (30 minutes)

The Global Feature Extractor (gFEX) is a hardware trigger module that has been recently installed and is in the commissioning process for Run 3 in the ATLAS experiment. The gFEX hardware design includes a Zynq Ultrascale+ SoC used for a variety of purposes. The custom Operating System (OS) used with the SoC is built using the Yocto Project integrated with Xilinx. This talk will discuss updates to the gFEX monitoring software, the status of OPC-UA integration for DCS, and plans to run TDAQ software directly on the SoC.

Presenter: DONA, Kristin (University of Chicago (US))

Session Classification: Project Session #2

Contribution ID: **23** Type: **not specified**

Tutorial #1: Building Linux Boot Files Using Templates for Multiple SoC Projects

Thursday, 5 October 2023 10:00 (1 hour)

Multiple hardware-platform projects and cooperation on common software features are two topics of interest that have emerged in the System on Chip Interest Group. Based on concrete experience of the ATLAS L1CT group with location-aware booting, we will answer the question "How can PetaLinux achieve this workflow?"by building a PetaLinux project that uses Yocto layers, patch files and device tree overlays to ensure consistency across hardware platforms and PetaLinux releases. Along the way, we will also show how these features come in together in ATLAS L1CT to accelerate the hardware and software development lifecycle as the group prepares for the important upgrades that come with the HL-LHC.

Presenter: MUSCARELLO, Giulio (Politecnico di Torino (IT))

Session Classification: Tutorials #1 and #2

Contribution ID: **25** Type: **not specified**

Tutorial #2: Using GitlabCI Parallel Builds for Mutlti-board PetaLinux Projects

Thursday, 5 October 2023 11:20 (1 hour)

This tutorial shows how to leverage GitLab CI parallel builds to optimize compilation and testing in PetaLinux projects for several boards simultaneously. Attendees will explore the advantages of enabling Continuous Integration (CI) and Continuous Deployment (CD) for Zynq SoC designs. The main focus is automating compilation, deployment of Zynq PL designs to actual boards, and booting the boards with these designs using a GitLab CI-based infrastructure. We start with the basics of Parallel Matrix in Gitlab CI. Then proceed with building the Petalinux projects, and all the necessary services around booting the board. Basic testing that the board has booted fully will be shown, however more complete testing of the software/firmware deployed with this mechanism is left to the user.

Presenter: ARUTJUNJAN, Kareen (CERN)

Session Classification: Tutorials #1 and #2

Contribution ID: **26** Type: **not specified**

Tutorial #3: Automating SoC/FPGA Firmware Testing using Kubernetes/Container-based Infrastructure

Friday, 6 October 2023 10:00 (1 hour)

This tutorial extends the CI/CD work presented in [1] and [2]. This time we solely focus on automated hardware testing utilizing Kubernetes and container-based infrastructure. First, we start describing an architecture of our testing platform and the device under test (DUT). The platform and DUT considered together combine both x86 and arm64 based hardware nodes. Then we introduce software stack which will allow us to build, deploy, and execute our tests automatically on SoC based hardware platforms. We conclude with demos on how to automatically collect, aggregate, and display tests'results within gilab CI/CD enabled project.
Hardware demonstrations will be done using low-cost KV260/KR260 development boards. If access to the hardware permits, we will extend the demo with a Versal-based board.
[1] SoC Interest Group Meeting, 23 November 2022, https://indico.cern.ch/event/1208190/
[2] 2nd System-on-Chip Workshop - CERN, 7-11 June 2021, https://indico.cern.ch/event/996093/

Presenter: HUSEJKO, Michal (Stanford University (US))

Session Classification: Tutorial #3

Contribution ID: **27** Type: **not specified**

FELIX for ATLAS Run 4 Readout: Based on a Xilinx Versal Prime ACAP Device

Thursday, 5 October 2023 13:30 (30 minutes)

For the readout of ATLAS in LHC Run 4, a prototype readout card was developed; the FLX182. The heart of the design is a Xilinx Versal Prime XCVM1802 device, a SoC with a dual core ARM Cortex-A72 application processor, as well as a Dual-core Arm Cortex-R5F real time processor.
The board contains 24 bidirectional optical links for DAQ, capable of transferring up to 25 Gb/s of data per link. Additionally 4 optical bidirectional links can either be used for 100Gb Ethernet or the LTI-TTC connection. A PCIe Gen4x16 connection is available to transfer data to the host server holding the card.
The data acquisition of FELIX happens entirely in the PL (programmable logic) of the XCVM1802, but some tasks, including flash programming and monitoring of the internal voltages and temperatures are done through the processing system. A built-in self test (BIST) application was developed as a web application running on the PetaLinux system inside the Versal Prime device. This BIST can test all the peripherals on the board, including the optical links and PCIe Gen4x16 link if external loopbacks are provided. A test report can be produced by the card as s stand-alone device as long as it has a 1Gb Ethernet connection.

Presenter: BOUKADIDA, Nayib (Nikhef National institute for subatomic physics (NL))

Session Classification: Project Session #3

Contribution ID: **28** Type: **not specified**

The Use of Xilinx Versal for the ATLAS Global Trigger

Thursday, 5 October 2023 14:00 (30 minutes)

This presentation will cover the following aspects:
- Comparison between Zynq and Versal.
- SoC implementation on Global Common Module (GCM) and its implications managing the file system and OS on multiple boards.
- Module control of FPGA over the Network on Chip (NOC).

Presenter: SANKEY, David (Science and Technology Facilities Council STFC (GB))

Session Classification: Project Session #3

Contribution ID: **29** Type: **not specified**

Split Boot v2 - Simple and Reliable Network-Based Booting for Serenity-S1 and other Boards with ZynqMPs Devices

Thursday, 5 October 2023 14:30 (30 minutes)

In preparation for the High-Luminosity upgrade of the LHC, the Serenity-S1 is designed as a multi-purpose ATCA electronics card. Like many other ATCA boards developed for the upgrade, it has a System-on-Chip from the AMD Xilinx Zynq UltraScale+ (ZUS+) family on board. In large systems with hundreds of ZUS+ devices, it is a significant challenge to keep the software on them up-to-date and in a uniform state. Although U-Boot on ZUS+ supports network boot via the Preboot Execution Environment (PXE), this is insufficient because their boot process requires application-specific information at a very early stage. After a brief update about the current state of development of the Serenity-S1, we will introduce Split Boot v2, an improved and dramatically simplified version of the already presented Split Boot, compatible with the popular Kria K26 and many other ZUS+ devices on any carrier card that provides network connectivity. The new approach relies on three phases. First, booting a generic minimal image, for instance, from the QSPI memory. Second, checking all boot-related data on the actual boot medium, for instance, the SD card, and updating the image via the network if necessary. Third, the boot mode of the ZUS+ is switched to the actual boot medium, and a soft reset is triggered. At this stage, the device boots as usual using the freshly fetched data.
Since this third stage is a regular boot of the ZUS+, PXE can be used to fetch the Kernel and NFS can be used to mount the root file system.

Presenter: FUCHS, Marvin (KIT - Karlsruhe Institute of Technology (DE))

Session Classification: Project Session #3

Contribution ID: **30** Type: **not specified**

SoC Infrastructure for the ATLAS Phase-II Level-0 Central Trigger

Thursday, 5 October 2023 15:00 (30 minutes)

For the Phase-2 upgrade of ATLAS, a new Central Trigger Processor (CTP), new Local Trigger Interfaces (LTIs), and new firmware for the Muon-CTP Interface (MUCTPI) will be developed. Already today, there is an increasing number of modules of prototypes and evaluation boards. All have a System-on-Chip (SoC) and need to be identified and booted with the right boot files, user application software and services. A common framework for consistently developing firmware and software, as well as automatically building, deploying, and testing boot files and user application software will be presented. The framework also contains development towards identifying and booting the SoCs and setting them up according to the module and their function within the experiment.

Presenter: SPIWOKS, Ralf (CERN)

Session Classification: Project Session #3

Contribution ID: **31** Type: **not specified**

CMS DAQ System Design with Zynq MPSoC for Phase-2

Thursday, 5 October 2023 15:50 (30 minutes)

This presentation will show the latest prototype of DAQ and Timing Hub (DTH) board developed by the CMS DAQ group for the Phase-2 upgrade of CMS. The board has three main functions: Provide data readout of back-end electronics with an aggregated bandwidth of 400 Gb/s over TCP/IP streams towards central DAQ; Interface to the CMS Trigger and Timing Control and Distribution System (TCDS) and distribute timing information to back-end boards; As a central HUB board, provide Gigabit Ethernet connectivity for node slots in the ATCA crate. It is equipped with a ZYNQ MPSoC SoM for configuration, control and monitoring purposes. The ZYNQ MPSoC is fully network booted, and the latest experience with the network configuration, network booting, and system shutdown is also presented.

Presenter: ZEJDL, Petr (CERN)

Session Classification: Project Session #3

Contribution ID: **32** Type: **not specified**

The CMS Barrel Muon Trigger Layer-1 Processor

Thursday, 5 October 2023 16:20 (30 minutes)

An ATCA processor was designed to instrument the first layer of the CMS Barrel Muon Trigger. The processor receives and processes DT and RPC data and produces muon track segments. The control and monitoring of the processor is taking place via a ZYNQ Ultrascale+ SoM. A Linux operating system runs on the ARM processors, providing configuration and monitoring of the board at a higher level. Interface with the outer world is achieved using Ethernet. The ZYNQ is connected with the FPGA using high speed copper serial links, allowing algorithm manipulation and high speed data movement between the two devices. Programming of the FPGA is also facilitated through the ZYNQ, as well as the communication via I2C buses with the on board peripherals. Software as well as firmware have been developed for the described functionalities.

Presenter: BESTINTZANOS, Ioannis (University of Ioannina (GR))

Session Classification: Project Session #3

Contribution ID: **33** Type: **not specified**

Xilinx Versal ACAP/SoC for Real-Time or Quasi-Real Time Data Processing

Thursday, 5 October 2023 16:50 (30 minutes)

We present a first look at utilizing the Versal AI Core Series ACAP/SoC for real-time or quasi-real time data processing applications in a high-energy physics context. We start from a demonstration of the LeNet convolutional neural network running on the Versal VCK190 using the AI Engine technology. We then discuss extending this to a more customized network architecture that is potentially capable of providing enhanced pattern recognition for collider physics applications in a real-time trigger system.

Presenter: ROSSER, Benjamin John (University of Chicago (US))

Session Classification: Project Session #3

Contribution ID: **34** Type: **not specified**

HyperFPGA: an Experimental Testbed for Future Heterogeneous Cluster Architectures

Thursday, 5 October 2023 17:20 (30 minutes)

The HyperFPGA is an open and scalable SoC-FPGA-based cluster aimed at exploring reconfigurable high-performance computing. HyperFPGA offers a flexible and programmable infrastructure that combines field-programmable gate arrays (FPGAs) with CPUs and high-speed general-purpose connectors. The flexibility of the platform extends to communication protocols at the hardware level, ideal for experimenting with novel architectures and interconnects. By leveraging on a SoM and carrier board approach, the design time is greatly reduced and the resulting platform is both future-proof and vendor independent. A Linux OS and custom driver, along with a Message Passing Interface (MPI), offer a programmable framework for firmware and task deployment. Overall, the testing of HyperFPGA using the N-Queens problem highlights the platform's ability to handle computationally intensive tasks and suggests its suitability for use in supercomputing.

Presenter: FLORIAN SAMAYOA, Werner Oswaldo (Universita e INFN Trieste (IT))

Session Classification: Project Session #3

Contribution ID: **35** Type: **not specified**

IT Support for SoC CI

Friday, 6 October 2023 13:30 (30 minutes)

Traditionally, FPGA development has been a bit like the Wild West, doing its own thing –separate from modern software practices –but recently there has been a push to incorporate CI pipelines and automated testing and building with version control. This presentation will outline some benefits of adopting CI practices in FPGA/SoC development and, most importantly, announce our plans for an IT project that will make both EDA tool images and appropriate runner infrastructure centrally available to FPGA/SoC engineers and developers.

Presenter: GENTSOS, Christos (CERN (IT-CA-GES))

Session Classification: System Session

Contribution ID: **36** Type: **not specified**

ATS - Linux for FECs and SoCs

Friday, 6 October 2023 14:00 (30 minutes)

The lowest tier in the accelerator control system uses Front-End Computers (x86_64), and in the near future will also feature SoC-based systems (aarch64). For their Operating System, the former use CentOS 7 and are configured as any other PC or server. The latter will likely demand an approach closer to those currently used for embedded systems but, after some research, we could not identify a long-term sustainable solution.
In BE-CEM, we made a synthesis of these two worlds and we are now able to offer a common solution. We realised that our Front-End Computers are more like embedded systems. We also acknowledge that future SoC-based systems will be quite powerful, allowing approaches usually adopted only for PCs and Servers. As a result, we selected Debian 12 as our reference OS and decomposed it in 4 parts: bootloader, kernel, initrd and userspace. This decomposition allowed us to have tighter control on the first three components.
This presentation will show you our journey from the selection process to the final selection and surrounding the infrastructure built around.

Presenter: VAGA, Federico (CERN)

Session Classification: System Session

Contribution ID: **37** Type: **not specified**

CERN Linux Landscape Update

Friday, 6 October 2023 14:30 (30 minutes)

The Linux landscape has shifted recently, causing a lot of confusion and nervousness in the community. This presentation will explain the recent changes and how they affect CERN and the wider HEP community, as well as providing an update on the ARM resources offered by CERN IT.

Presenter: IRIBARREN, Alex (CERN)

Session Classification: System Session

Contribution ID: **38** Type: **not specified**

Tackling Supply Chain Attacks in SoC Software with Software Bill of Material

Friday, 6 October 2023 15:00 (30 minutes)

Supply chain attacks in the context of industrial controls involve malicious actors infiltrating the network by exploiting vulnerabilities in third-party components or software used in critical systems. These attacks can compromise the integrity and reliability of industrial operations, potentially leading to disruptions, data breaches, and unauthorized control over essential infrastructure. CERN as a decentralized research facility is not immune to such threats, however standards and tools are available to help us measure our exposure to high-risk software vulnerabilities and mitigate those risks.

Presenters: COPY, Brice (CERN); DOBSON, Marc (CERN)

Session Classification: System Session

Contribution ID: **39** Type: **not specified**

ATLAS & CMS System Administration with SoCs

Friday, 6 October 2023 15:45 (30 minutes)

Presenters: SCANNICCHIO, Diana (University of California Irvine (US)); DOBSON, Marc (CERN)

Session Classification: System Session

Contribution ID: **40** Type: **not specified**

CMS Network and Booting

Friday, 6 October 2023 16:15 (20 minutes)

Presenter: DOBSON, Marc (CERN)

Session Classification: System Session

Contribution ID: **41** Type: **not specified**

ATLAS Network and Booting

Friday, 6 October 2023 16:35 (20 minutes)

Presenter: DUPONNOIS, Quentin (CERN)

Session Classification: System Session

Contribution ID: **42** Type: **not specified**

Summary and Closure

Friday, 6 October 2023 16:55 (30 minutes)

Presenter: BOUKABACHE, Hamza (CERN)

Session Classification: System Session

Contribution ID: **43** Type: **not specified**

Welcome

Monday, 2 October 2023 09:30 (10 minutes)

Presenter: SOC ORGANISING COMMITTEE

Session Classification: Vendor Session #1.A

Contribution ID: **44** Type: **not specified**

Vendor Exhibition #1 (with coffee&tea)

Monday, 2 October 2023 10:40 (1h 50m)

Presenter: ALL VENDORS

Session Classification: Vendor Exhibition #1

Contribution ID: **45** Type: **not specified**

Enclustra - FPGA SoC Solutions - Portofolio and Roadmap

Monday, 2 October 2023 16:20 (30 minutes)

This presentation presents a comprehensive overview of the Enclustra FPGA solutions ecosystem. We offer a full spectrum of Hardware solutions, from FPGA SoC modules and baseboards to development kits. On the other hand, we provide top-notch engineering services, ensuring seamless integration and customization. Finally, we pride ourselves on responsive customer support, assisting at every stage of your project. Join us to explore how our FPGA SoC solutions empower innovation and streamline your development journey today and tomorrow.

Presenter: JOKAR, Samir (Enclustra)

Session Classification: Vendor Session #1.B

Contribution ID: **46** Type: **not specified**

Update of the ATLAS Online SW DAQ-to-SoC Communication Prototype

Wednesday, 4 October 2023 17:20 (30 minutes)

We are presenting an update of the prototype implementation of the DAQ to SoC communication library, provided by ATLAS DAQ Online Software group. The presented solution is lightweight, based on the HTTP protocol and Nginx software implementation of HTTP server and allows to organize command exchange between ATLAS Run Control framework and SoC controlled subsystems, typically during operations of SoC in the scope of a data-taking session.

Presenter: KAZAROV, Andrei (University of Johannesburg (SA))

Session Classification: Project Session #2