

# TWEPP 2023 Topical Workshop on Electronics for Particle Physics

Sunday, 1 October 2023 - Friday, 6 October 2023

Geremeas, Sardinia, Italy



# **Book of Abstracts**

# Contents

ATLAS LAr Calorimeter Commissioning for LHC Run-3 . . . . .	1
Development of the Continuous Readout Digitising Imager Array Detector . . . . .	1
Prototyping during pre-production: the re-design of ATLAS ITk strip tracker powerboards for the end-cap . . . . .	3
The quality control programme for ITk strip tracker module assembly . . . . .	4
How the discovery of Cold Noise delayed the production of ATLAS ITk strip tracker mod- ules by a year . . . . .	5
Demonstration of the digital readout chain in the NvDEx experiment . . . . .	6
CMS Outer Tracker Phase-2 Upgrade on-module powering . . . . .	7
RD53A Quad Modules Production and QC for the ATLAS Inner Tracker Outer Barrel (OB) Demonstrator. . . . .	8
Silicon photonic, planar coupled, 4-channel WDM transmitter . . . . .	9
HEPS-BPIX40: the upgrade of the hybrid pixel detector for the High Energy Photon Source . . . . .	10
System level tests of large-scale multi-module prototype structures of the ATLAS ITk pixel detector . . . . .	11
Hybrid designs and kick-off production experience for the CMS Phase-2 Upgrade . . . .	11
A high time resolution and dynamic range monolithic pixel detector-ASIC for Micro Vertex Detector in PANDA experiment . . . . .	12
Fault Tolerance Evaluation Study of a RISC-V Microprocessor for HEP Applications . . .	13
A Charge-integration Pixel Detector Readout Chip Features High Frame Rate with in-pixel ADCs. . . . .	14
Prototype electronics for the silicon pad layers of the future Forward Calorimeter (FoCal) of the ALICE experiment at the LHC . . . . .	15
Development of monolithic pixel sensor prototypes for the CEPC vertex detector . . . .	16
ALICE ITS3: a bent stitched MAPS-based vertex detector . . . . .	17

Software mitigation scheme to increase availability under the radiation of microcontroller-based design for LHC accelerator environment . . . . .	18
SET sensitivity study of a VCRO-based PLL for HL-LHC ATLAS HGTD . . . . .	19
A Low-Power Gated-Vernier Ring Oscillator TDC for Cryogenic Detectors . . . . .	20
A High Time Resolution Monolithic Active Pixel Sensor with Node-Based, Data Driven and Parallel Readout for Vertex Detector in particle physics Experiments . . . . .	21
The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results . . . . .	22
The Prototype Design of PEB - a Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade . . . . .	23
Front-End RDMA Over Converged Ethernet, real-time firmware simulation . . . . .	24
An FPGA-based Front-end Module Emulator for the High Granularity Timing Detector Readout Module . . . . .	25
Verification Environment for ALTIROC ASIC of the ATLAS High Granularity Timing Detector . . . . .	26
Commissioning of the Test System for the Phase-2 Upgrade of the CMS Outer Tracker . . . . .	27
Test Result of the New ASD2 Chips for Phase-II Upgrade of the ATLAS MDT Chambers at HL-LHC . . . . .	28
3D-integrated pixel circuit for a low power and small pitch SOI sensor . . . . .	29
An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs . . . . .	30
Design and implementation of Neural Network based conditions for the CMS Level-1 Global Trigger upgrade for the HL-LHC . . . . .	31
Adaptability and efficiency of the CMS Level-1 Global Trigger firmware implementation for Phase-2 . . . . .	32
A Custom Discrete Amplifier-Shaper-Discriminator Circuit for the Drift Chambers of the R3B Experiment at GSI . . . . .	33
CMS ECAL VFE design, production and testing . . . . .	34
HGTD PEB DC/DC Power Block in Low Temperature and Magnetic Field Operation . . . . .	35
Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology . . . . .	36
Design and First Experience of the Prototype Pixel Layers for the ALICE FoCal . . . . .	37
Best Practices in Design Verification of ASICs for High Energy Physics Experiments . . . . .	38
A high frequency radiation hardened DC/DC-converter with low volume air core inductor . . . . .	39

The optimization, design and performance of the FBCM23 ASIC for the upgraded CMS beam monitoring system . . . . .	40
A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs. . . . .	41
Cryogenic Charge Readout Electronics for the ProtoDUNE-II Program and DUNE . . . .	42
SiC based beam monitoring system for particle rates from kHz to GHz . . . . .	43
Universal test system for boards hosting bPOL12V DC-DC converters. . . . .	44
Testing and characterisation of the prototype readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker . . . . .	45
CMS Level-1 trigger Data Scouting firmware prototyping for LHC Run-3 and CMS Phase-2 . . . . .	46
40MHz trigger-less readout of the CMS Drift Tube muon detector . . . . .	47
System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC	47
CMS HGCALElectronics Vertical Integration System Tests . . . . .	48
Design of a very low power 12 bits 40 MS/s ADC based on a time-interleaved SAR architecture . . . . .	49
Ionizing Radiation Influence on 28-nm MOS Transistor's Low-Frequency Noise Characteristics . . . . .	50
The CMOS Pseudo-Thyristor: A Zero-Static Current Circuit for Pixelized Detector Front-End Stage . . . . .	51
SiGe integrated chip readout for fast timing . . . . .	52
NEW GENERATION B-FIELD AND RAD-TOLERANT DC/DC POWER CONVERTER FOR ON-DETECTOR OPERATION . . . . .	53
A demonstrator for a real-time AI-FPGA-based triggering system for sPHENIX at RHIC .	54
Single Event Effects characterization of a commercial 28 nm CMOS technology . . . . .	55
The End-of-Substructure (EoS) card for the ATLAS Strip Tracker Upgrade –from Design to Production . . . . .	56
Performance profiling and design choices of an RDMA implementation using FPGA devices . . . . .	57
FLX-182, the hardware platform for ATLAS readout during High Luminosity LHC . . . .	58
Status of the MDT Trigger Processor for the ATLAS Level-0 Muon Trigger at the HL-LHC	59
Upgrade of the ATLAS Level-0 TGC Endcap Muon Trigger . . . . .	60
A full-function Global Common Module (GCM) prototype for ATLAS Phase-II upgrade .	61
The phase-1 upgrade of the ATLAS level-1 calorimeter trigger . . . . .	62

Reliability of Power Conversion Card for CMS MTD-BTL . . . . .	63
The Trigger & Data Acquisition interface module of the Tile Calorimeter for the ATLAS Phase- II Upgrade . . . . .	64
Performance of a novel charge sensor on the ion detection for the development of a high-pressure avalancheless ion TPC . . . . .	65
Reliability Run and Data Analysis of the Accelerated Aging of Present and Future Electrolytic Capacitors Installed in the Protection Systems of Superconducting Magnets of the Large Hadron Collider at CERN . . . . .	66
Design of the OBELIX monolithic CMOS pixel sensor for an upgrade of the Belle II vertex detector . . . . .	67
Development of the data transmission architecture of the stitched sensor prototype towards the ALICE ITS3 upgrade . . . . .	68
28 nm front-end channels for the readout of pixel sensors in future high-rate applications	68
CMS ECAL Upgrade Front End card. Design and performance. . . . .	69
Model and analysis of the data readout architecture for the ITS3 ALICE Inner Tracker System . . . . .	70
Radiation Tolerance Tests for SFP+ Transceivers . . . . .	71
A readout system based on SiPM for the dRICH detector at the EIC . . . . .	72
A prototype 4D-tracking demonstrator based on the TimeSPOT developments. . . . .	73
Data acquisition system of the PANDA Micro-Vertex Detector (MVD) . . . . .	74
Prototype of a 10.24Gbps Data Serializer and Wireline Transmitter for the readout of the ALICE ITS3 detector. . . . .	75
Performance of H2GCROC3, the readout ASIC of SiPMs for the back hadronic sections of the CMS High Granularity Calorimeter. . . . .	76
A Radiation Hardened IP Development Programme for 28nm CMOS Technology . . . . .	77
Digital processing and BLMASIC control prototype for the Beam Loss Monitor system in the SPS at CERN. . . . .	78
Integrating lpGBT into the Common Readout Units (CRU) of the ALICE Experiment . . . . .	79
NAPA-P1: NANOSECOND TIMING PIXEL FOR LARGE AREA SENSORS . . . . .	80
SAQRADC: An on-demand, low-power, minimal footprint, 10-bit resolution charge-redistribution ADC with internal clock generation . . . . .	81
An FPGA-based Data Aggregator for ATLAS ITK Pixel DCS System . . . . .	82
Electrical / piezo-resistive effects in bend AlpiDe - Monolithic Active Pixel (MAP) sensors . . . . .	83
Performance of the COLUTA ADC ASIC for the ATLAS HL-LHC Liquid Argon Calorimeter Readout . . . . .	84

Characteristics and total ionizing dose response of 22nm Fully Depleted Silicon-on-Insulator .....	85
Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers .....	86
Development of FABulous: An Embedded FPGA Framework in 28nm CMOS .....	87
CRATEBO: A High-speed, Radiation-Tolerant and Versatile Testing Platform for FPGA Ra- diation Qualification for High-Energy Particle Accelerator applications .....	87
The LHCb VELO Upgrade II: design and development of the readout electronics .....	88
On-beam system test of the new readout electronics for the CMS Electromagnetic Calorime- ter upgrade .....	89
32-channels mixed-signal processor for the tracking system of the GAPS dark matter ex- periment .....	90
Two HVCMOS active pixel ASIC designs for the Measuring GCR and SEP with a combined dynamic range of >80dB .....	91
Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3 .....	92
SystemC framework for architecture modelling of electronic systems in future particle de- tectors .....	93
FastRICH: a readout ASIC with precise time stamping for the LHCb RICH detector .....	94
The status of the Back-end card for the JUNO experiment .....	95
Design and Characterization of a precision tunable time delay integrated circuit. ....	96
DC Power Circuit Evaluation for the Development of the Barrel Calorimeter Processor V2	97
Integration of EDWARD readout architecture in full-field fluorescence imaging detector	98
Mu2e calorimeter readout electronics: design, characterisation, and radiation hardness ..	99
The Analog Front End for FastRICH: an ASIC for the LHCb RICH Detector Upgrade .....	100
MIMOSIS2 validations using Cadence Protium platform and its Black Box flow .....	101
Magnetic resilience studies for power supplies .....	102
CERN Radiation Hardness Assurance: Challenges and Solutions for Large-Scale Distributed System Exposed to High-Energy Particle Accelerator Environments .....	102
Multi-Channel Radiation-Tolerant Humidity Monitoring System for the CMS Inner Cold Sub-detectors .....	103
Radiation test of commercial of the shelf (COTS) optical transceivers in the frame of the beam position monitor (BPM) consolidation project for the Large Hadron Collider (LHC) .....	104
Test Bench of a 100G Radiation Hardened Link for Future Particle Accelerators .....	105

Chips for calibration of the ATLAS LAr calorimeter . . . . .	106
Prototype measurement results in a 65nm technology and TCAD simulations towards more radiation tolerant monolithic pixel sensors . . . . .	107
Test and performance of the LiTE-DTU ASIC for the HL-LHC upgrade of the CMS ECAL barrel . . . . .	108
Novel developments on the OpenIPMC project . . . . .	109
Digital duty cycle correction system for clock paths in radiation-tolerant high-speed wire- line transmitters . . . . .	110
In-pixel AI for lossy data compression at source for X-ray detectors . . . . .	111
Method for extracting the single event upset cross section from error counts in triplicated error-correction code registers . . . . .	112
Dual use driver for high speed links transmitters in the future high energy physics experi- ments . . . . .	113
Characterization of the ATLAS Liquid Argon Front-End ASIC ALFE2 for the HL-LHC up- grade . . . . .	114
SciFi Front-End Electronics: Calibration and Results on detector performance . . . . .	115
Design and characterization of RD53C production chips for ATLAS and CMS pixel upgrades at HL-LHC . . . . .	116
Tri-axis 5 $\mu$ m hexagon pixel-strip matrix combining 3*852 current comparator in a 180nm node . . . . .	117
The CMS HGCALE trigger data receiver . . . . .	118
Real time data processing with FPGAs at LHCb . . . . .	119
Overview of the production and qualification tests of the lpGBT . . . . .	120
Digital on Top methodology for Monolithic Active Pixel Sensor, feedback from MIMOSIS sensors for CBM Micro-Vertex Detector . . . . .	121
Lab measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype detector with a large breakdown voltage . . . . .	122
Electronics Upgrade for the HADES MDC Drift Chambers . . . . .	123
Design and measurements of SMAUG1, a prototype ASIC for voltage measurement using noise distribution . . . . .	124
Time and Clock Distribution Over a Hierarchy of Deterministic Optical Links . . . . .	125
High-speed front-end electronics and digitisation system for the Crilin calorimeter with enhanced timing performance . . . . .	126
Towards Single-Event Upset detection in Hardware Secure RISC-V processors . . . . .	127



The development of a laser system for use in the timing performance measurements of CMS HGCAL silicon modules . . . . .	128
Proof of principle for a novel PET detector . . . . .	129
Constant Fraction Discriminator for NA62 experiment at CERN . . . . .	130
A prototype readout system for the beam monitor at the CSR external-target experiment	131
Design of the ASIC readout scheme for the JUNO-TAO experiment . . . . .	132
Development of a multi-purpose DAQ system for Timepix4-based detectors. . . . .	133
AstroPix: A novel HV-CMOS pixel sensor for space-based experiments . . . . .	134
Development and performance of a pixel chip for the readout of GEM detectors for high- rate particle tracking . . . . .	135
A common readout unit for multichannel array detectors at HIRFL-CSR . . . . .	136
Compact Silicon Photonic Mach-Zehnder Modulators for High-Energy Physics . . . . .	137
Radiation Tolerance of the MUX64 for the High Granularity Timing Detector of ATLAS	138
Beam test of a baseline vertex detector for the CEPC . . . . .	139
Implementation and performance comparison of MMC firmware on RISC-V and ARM- based MCUs . . . . .	140
Real-time Signal Processing and Data Acquisition for the Electric Field Detector (EFD-02) on the CSES-02 satellite . . . . .	141
Commissioning of the Upstream Tracker for the LHCb upgrade . . . . .	142
Evaluating the RFSoc as a Software-Defined Radio Readout System for Magnetic Microcalorime- ters . . . . .	142
A novel Front-End for Monolithic Active Pixel Detectors ASICs . . . . .	143
First test results for ECON-T and ECON-D ASICs for CMS HGCAL . . . . .	144
Development of quad-channel high resolution digital picoammeter for beam diagnostics	146
Testing a Neural Network for Anomaly Detection in the CMS Global Trigger test crate during Run 3 . . . . .	147
Front End Board for Large Area SiPM Detector . . . . .	148
RD50-MPW: A monolithic High Voltage CMOS pixel chip with high granularity and high radiation tolerance . . . . .	148
From 3D to 5D tracking: SMX ASIC-based Double-Sided Micro-Strip detectors for compre- hensive space, time, and energy measurements . . . . .	149
Characterization of the BigRock 28 nm Fast Timing Analog Front End . . . . .	150
Design Updates for HPSoc: A very high Channel Density Waveform Digitizer with sub- 10ps resolution . . . . .	151

Design updates for AARDVARCv4: Waveform Sampling System On Chip with Picosecond Timing Resolution . . . . .	152
Outer Barrel services chain characterization for the ATLAS ITk Pixel Detector . . . . .	153
MightyPix at the LHCb Mighty Tracker –Verification of an HV-CMOS pixel chip’s digital readout . . . . .	154
The OBDT-theta board: time digitization for the theta view of Drift Tubes chambers. . .	155
Design and implementation of the Hybrid Detector for Microdosimetry (HDM): Challenges in readout architecture and experimental results . . . . .	156
Time-Delay-Based Analog Front-End for Monitored Drift Tubes in 65 nm CMOS with < 200 ns Baseline Recovery Time and Coherent Time-over-Threshold . . . . .	157
FPGA Firmware design with High Level Synthesis: Methodology, gains, and pitfalls . . .	158
Design and performance of the front-end electronics of the charged particle detectors of PADME experiment . . . . .	159
The Optosystem: validation and testing of the high-speed optical-to-electrical conversion system for the readout of the ATLAS ITk Pixel upgrade . . . . .	160
Lessons from integrating CMS Phase-2 back-end electronics and first results from Serenity-S1, a production optimised ATCA blade. . . . .	161
A low crosstalk 768-channel of 14-bit analog to digital converters for high resolution array of detectors. . . . .	162
The first full size full functionality ETROC2 (16x16) prototype for CMS MTD Endcap Timing Layer (ETL) upgrade . . . . .	163
GaN based DC-DC converters for high energy physics applications . . . . .	164
Design, production and irradiation results of the new advanced front end electronics of CMS iRPC . . . . .	165
Accelerators overview, outlook, differences, why do we need the different concepts, FCC/e+/muon..., impact on detector R&D and electronics . . . . .	165
Advancing fusion energy: Meeting the challenges of diagnostics and electronics for the ITER project . . . . .	166
Introduction . . . . .	166
lpGBT calibration . . . . .	166
VTRx+ production ramp up challenges and status . . . . .	167
VL+ optical fibre plant preproduction status and production plans . . . . .	167
The Design and Packaging Challenges of a High Density 25G Optical Engine . . . . .	167
Opening . . . . .	167
Introduction . . . . .	167

The search for gravitational waves from LIGO/Virgo/KAGRA detectors to Einstein Telescope: recent results and new frontiers of gravitational wave instruments and astronomy . . . . .	167
Sardinia cultural heritage: the nuraghi and nuragic civilization . . . . .	168
Welcome . . . . .	168
EUROPRACTICE IC services and foundry news . . . . .	168
EUROPRACTICE EDA tools for the HEP community . . . . .	169
CERN ASIC support and Foundry services news . . . . .	169
Open discussion . . . . .	169
Experience with RFSoc for Beam Instrumentation applications . . . . .	169
RFSoc used as a readout for Magnetic Microcalorimeters . . . . .	169
TBC . . . . .	169
Discussion . . . . .	170
Associazione "Sardegna verso l'UNESCO" . . . . .	170



**System Design, Description and Operation / 2****ATLAS LAr Calorimeter Commissioning for LHC Run-3**

**Author:** LAr speaker committee<sup>None</sup>

**Corresponding Authors:** florent.bernon@cern.ch, larspeak@cern.ch

To cope with the increase of the LHC instantaneous luminosity, new trigger readout electronics were installed on the ATLAS Liquid Argon Calorimeters.

On the detector, 124 new electronic boards digitise 10 times more signals than the legacy system. Downstream, large FPGAs are processing up to 20 Tbps of data to compute the deposited energies. Moreover, a new control and monitoring infrastructure has been developed.

This contribution will present the challenges of the commissioning, the first steps in operation, and the milestones still to be completed towards the operation of both the legacy and the new trigger readout for LHC Run-3.

**Summary (500 words):**

The Liquid Argon Calorimeters are employed by ATLAS for all electromagnetic calorimetry in the pseudo-rapidity region  $|\eta| < 3.2$ , and for hadronic and forward calorimetry in the region from  $|\eta| = 1.5$  to  $|\eta| = 4.9$ . They also provide inputs to the first level of the ATLAS trigger. After successful period of data taking during the LHC Run-2 between 2015 and 2018 the ATLAS detector entered into the a long period of shutdown. In 2022 the LHC will restart and the Run-3 period should see an increase of luminosity and pile-up up to 80 interaction per bunch crossing.

To cope with this harsher conditions, a new trigger readout path has been installed during the long shutdown. This new path should improve significantly the triggering performances on electromagnetic objects. This will be achieved by increasing the granularity of the objects available at trigger level by up to a factor of ten.

The installation of this new trigger readout chain required also the update of the legacy system. More than 1500 boards of the precision readout have been extracted from the ATLAS pit, refurbished and re-installed. The legacy analog trigger readout that will remain during the LHC Run-3 as a backup of the new digital trigger system has also been updated.

For the new system 124 new on-detector boards have been added. Those boards that are operating in a radiative environment are digitizing the calorimeter trigger signals at 40MHz. The digital signal is sent to the off-detector system and processed online to provide the measured energy value for each unit of readout. In total up to 31Tbps are analyzed by the processing system and more than 62Tbps are generated for downstream reconstruction. To minimize the triggering latency the processing system had to be installed underground. The limited available space imposed a very compact hardware structure. To achieve a compact system, large FPGAs with high throughput have been mounted on ATCA mezzanines cards. In total no more than 3 ATCA shelves are used to process the signal from approximately 34000 channels.

Given that modern technologies have been used compared to the previous system, all the monitoring and control infrastructure is being adapted and commissioned as well.

This contribution will present the challenges of the installation, the commissioning and the milestones still to be completed towards the full operation of both the legacy and the new readout paths for the LHC Run-3.

**Tuesday posters session / 6****Development of the Continuous Readout Digitising Imager Array Detector**

**Authors:** Alexander Klujev<sup>1</sup>; Cornelia Wunderer<sup>2</sup>; David Pennicard<sup>None</sup>; Hans Krueger<sup>3</sup>; Sabine Lange<sup>4</sup>; Torsten Laurus<sup>5</sup>; Ulrich Trunk<sup>6</sup>; alessandro marras<sup>None</sup>; heinz graafsma<sup>2</sup>

<sup>1</sup> *Deutsches Elektronen-Synchrotron*

<sup>2</sup> *DESY*

<sup>3</sup> *University of Bonn*

<sup>4</sup> *Desy*

<sup>5</sup> *Deutsches Elektronen-Synchrotron DESY*

<sup>6</sup> *Physikalisches Institut*

**Corresponding Author:** alessandro.marras@desy.de

The CoRDIA project aims to develop an X-ray imager capable of continuous operation in excess of 100 kframe/s. The goal is to provide a suitable instrument for Photon Science experiments at diffraction-limited Synchrotron Rings and Free Electron Lasers considering Continuous Wave operation.

Individual circuit blocks (adaptive-gain amplifier, analog-to-digital converter) were produced using a 65nm process and characterized, confirming expected performances.

A prototype has been designed, assembling said blocks in a pipelined, modular structure that can be replicated in a 2D pixel array.

Manufacturing is expected in spring 2023. Design architecture, expected performances and first test results will be reported.

#### **Summary (500 words):**

The upgrade of Synchrotron Rings toward the diffraction limit demands an upgrade of X-ray imagers to faster, continuous operation. Such devices are also needed to exploit the potential of high repetition-rate Free Electron Lasers considering Continuous Wave operation.

The CoRDIA (Continuous Readout Digitising Imager Array) detector aims at providing a hybrid detector capable of photon discrimination at 12 keV (also compatible with high-Z sensors for higher energies), a substantial full well, a compact pixel size (~100um), and continuous readout capability at a frame rate of ~150 kHz.

A first prototype including circuit blocks (analog front-end, analog-to-digital converter) has been manufactured in TSMC65nm technology, confirming expected performances [1].

A second prototype has now been designed, with the goal of signal-processing images in a pipeline fashion (so that one image is acquired at the same time the former one is digitized and streamed out), while at the same time arraying the circuits in a modular “superpixel” structure can be replicated in a 2D matrix in the readout ASIC.

The design (Figure) integrates the ADCs and the silicon area reserved for transmission drivers within the pixel array area (along with the analog front-end circuits), rather than relegating them to a periphery outside of the array (that would result in blind regions in a multi-chip assembly). The bump-bond pads interfacing to the sensor are redistributed to a uniform 2D array to facilitate bonding.

The circuits in the analog Front-End are designed using a standard-cell template for easiness of reuse, Place&Routing, and compatibility with existing digital designs, while trying to implement some RD53 recommendations to mitigate the impact of ionizing radiation. The Front-End includes an adaptive-gain circuit to extend the dynamic range, inspired by the AGIPD detector [2].

The Front-End to ADC interface consists in two sets of Sample/Hold cells that allow parallel charge integration of an image (at 150kHz), while charge integrated during the former image is sequentially passed to a Successive Approximation Register (11bit) digitizer (at 2.5MS/s), serving the 16 pixels included in the “superpixel” modular structure. Both circuits have proven to work within expected performances as insulated units; the purpose of the second CoRDIA prototype is to verify their operation as a circuital chain.

The superpixels are arranged in a mirrored double-column fashion around the common silicon area reserved for the output driver. Rather than develop a new high-speed driver, we decided to adopt the PCS-GWT solution developed by NIKEF for Timepix4 [3]. The drivers are not yet implemented in the second CoRDIA prototype, but Place&Route estimations suggest the area reserved is more than enough for the purpose, even reserving some space for TSV landing pads.

The prototype has been submitted for manufacturing at the end of 2022, and it is foreseen to be tested in spring 2023. Test results will be reported.

- [1] A Marras et al Journal of Physics: Conference Series 2380 (2022) 012093  
[2] X.Shi et al NIM-A Vol 624, Iss 2, 11 December 2010, Pages 387-391  
[3] X. Llopart et al 2022 JINST 17 C01044

**Power, Grounding and Shielding / 7**

## **Prototyping during pre-production: the re-design of ATLAS ITk strip tracker powerboards for the end-cap**

**Author:** Dennis Sperlich<sup>1</sup>

**Co-author:** Luise Poley<sup>2</sup>

<sup>1</sup> *Albert Ludwigs Universitaet Freiburg (DE)*

<sup>2</sup> *Simon Fraser University (CA)*

**Corresponding Author:** dennis.sperlich@cern.ch

For the construction of the future ATLAS strip tracker end-caps, six geometries of silicon strip detector modules were designed. Each module comprises one or two silicon strip sensors and several flexes holding the required readout electronics, designed to match the geometry of each module. Due to the large number of designs, two module geometries using two sensors per ring module were prototyped for the first time in 2022, and showed excessively high noise. This contribution presents an overview of the follow-up investigation to diagnose the issue, the subsequent powerboard re-design and results from the first prototypes in 2023.

### **Summary (500 words):**

Modules for the ATLAS ITk strip tracker are designed to meet several strict design criteria: a noise occupancy of < 1% and efficiency of at least 99% and a signal-to-noise ratio of at least 10:1 at the expected end-of-life fluence and dose. For the assembly of ITk strip tracker end-caps, six different module geometries were developed in order to provide sufficient coverage for tracking. The three module types located on smaller radii comprise one sensor (diced to maximise usable area of a 6" wafer) each, the module geometries located on outer radii require the combination of two sensors each.

Due to the high cost of prototyping especially sensor geometries, out of the six sensor shapes, only the innermost one was prototyped during the R&D phase. Dual sensor modules could only be prototyped as an approximate version using the existing sensor shape and an early development version of the powerboard. Using these combinations of prototype geometries, there was no strong evidence for excess noise during the R&D phase.

When the first prototype modules of all module geometries were assembled in 2022, the module types located at the outermost radii (R4 and R5) showed a noise excess far above the design specifications (up to twice the allowed maximum), making the approved design unusable for the production phase scheduled to begin within 12 months. Over the course of three months, an extensive investigation into the source of the excess noise was conducted by systematically modifying the test setup and module geometry. This process was made more complicated by the limited quantities of available parts: only two modules of each geometry (R4 and R5) were available world-wide to perform all necessary tests and modifications during this investigation. The tests included additional shielding, modified grounding and referencing and SMD component replacements.

Eventually, the powerboard, a kapton flex designed to control and monitor voltage and current for the module, was identified as the source of the noise. With the identification of the input filter as the noise source, a systematic weakness in all four powerboard designs was discovered. Improving the filtering was found to recover the module noise performance close to expectations.

With a pressing need for a re-design to produce a module within required specifications, several powerboard variations of the same geometry were designed and produced in parallel and became available for assembly into modules in 2023. Each design variant was assembled into at least two modules and their noise performance tested for comparison, leading to a design selection and first R4 and R5 module

prototypes within specification, as well as a good understanding of the underlying issue.

**Thursday posters session / 8**

## **The quality control programme for ITk strip tracker module assembly**

**Authors:** Abraham Tishelman-Charny<sup>1</sup>; Luise Poley<sup>2</sup>

<sup>1</sup> *Brookhaven National Laboratory (US)*

<sup>2</sup> *Simon Fraser University (CA)*

**Corresponding Authors:** [abraham.tishelman.charny@cern.ch](mailto:abraham.tishelman.charny@cern.ch), [anne-luise.poley@cern.ch](mailto:anne-luise.poley@cern.ch)

The assembly of the ATLAS Inner Tracker requires the construction of 19,000 silicon strip sensor detector modules in eight different geometries. Modules will be assembled and tested at 31 institutes on four continents, from sensors, readout chips and flexes. In order to adhere to the module specifications defined for sufficient tracking performance, a rigorous programme of quality control and assurance was established to cover components at every stage of assembly. This contribution presents an overview of the QA/QC programme for ITk strip tracker modules, results from the pre-production phase (5% of the production volume) and proposed adjustments for production.

### **Summary (500 words):**

Modules for the future ATLAS strip tracker are assembled in a series of steps which are identical for all modules:

- 1) reception tests of SMD populated flexes  
requiring visual inspection and wire bonding tests
- 2) assembling readout chips to hybrid flexes using UV cure glue  
requiring visual inspection, weighing to determine the amount of used glue and metrology to determine correct positioning and heights
- 3) electrically connecting readout chips and flexes using wedge bond wirebonding  
followed by full electrical characterisation and burn-in
- 4) reception tests of silicon strip sensors  
requiring visual inspection and an electrical test to determine leakage current and breakdown voltage
- 5) attaching a high voltage connection to the back of the sensor  
requiring visual inspection and electrical sensor testing
- 6) reception tests of powerboard flexes  
consisting of visual inspection and full electrical characterisation tests
- 7) assembly of hybrids and powerboards to sensor using an epoxy glue  
requiring visual inspection, weighing to determine glue weight, metrology to determine the sensor bow and to check component positions and height
- 8) electrically connecting readout chips and sensor strips using wedge bond wirebonding  
followed by a full electrical characterisation and tests alternating between warm and cold temperatures

At each step of the assembly process, one or more QC steps are performed to ensure compliance of each assembled component with all mechanical and electrical requirements. Additional quality assurance tests are performed to ensure the sufficient quality of all components to be used for module assembly. 31 institutes worldwide participate in the overall module assembly effort, performing either the full assembly chain or part of it, sharing the effort with other institutes, in which case additional tests are performed as reception tests of each component transported between institutes.

In order to ensure comparability of test results between institutes using different measurement setups and machines, a common set of procedures, documents and database structures was developed. All institutes were checked for adherence to common procedures as part of an overall site qualification process and results were compared throughout pre-production (5% of the overall production volume).



Several issues were identified during pre-production based on the available data:

- high noise of end-cap modules comprising two sensors
- glue build-up on assembly tooling leading to component heights outside of specification
- low inter-strip isolation between sensor strip implants leading to increased noise

For other characteristics, the data available from pre-production was sufficient to relax the requirements for production regarding e.g. positioning and height precision and electrical performance, which was made possible by the availability of data in a common format, uploaded to the common production database.

Prototyping and pre-production of modules were used to exercise the entire QC programme designed to catch potential, still unknown issues, with the goal to re-evaluate their necessity for a robust QC programme during production. We believe this collection of data to be of interest to the particle physics community due to its size and ability to re-evaluate which aspects of QC will be considered necessary going forward.

Invited / 9

## How the discovery of Cold Noise delayed the production of ATLAS ITk strip tracker modules by a year

Author: Luise Poley<sup>1</sup>

<sup>1</sup> *Simon Fraser University (CA)*

Corresponding Authors: [matthew.glenn.kurth@cern.ch](mailto:matthew.glenn.kurth@cern.ch), [george.dyckes@cern.ch](mailto:george.dyckes@cern.ch), [anne-luise.poley@cern.ch](mailto:anne-luise.poley@cern.ch)

The construction of the ATLAS strip tracker barrel will require the assembly of 12,000 barrel detector modules over the course of 3.5 years. In 2022, during the module pre-production phase, modules were found to display clusters of noisy channels outside required specifications when tested at operating temperatures (-40 °C), called “Cold Noise”. Extensive investigations into the cause and mechanism of Cold Noise interrupted pre-production and occupied most barrel module assembly sites. This contribution presents an overview of the year-long investigations into Cold Noise, the final identification of the underlying mechanism and necessary changes for the transition to production.

### Summary (500 words):

Silicon strip sensor modules for the strip tracker barrel consist of a silicon strip sensor, one polyimide flex board controlling and monitoring voltage and current (“powerboard”) and one or two kapton flexes with ten readout chips each (“hybrids”). For sufficient tracking performance, modules are required to have a noise occupancy < 1%, a hit efficiency > 99%, less than 2% bad channels and a signal-to-noise ratio of at least 10:1 at the end of life.

In 2022, pre-production barrel modules tested at operating temperature (-40°C) displayed clusters of very noisy channels, exceeding the specifications for acceptable module performance. Cold Noise was observed starting at temperatures between -20°C and -40°C, was observed to worsen or, occasionally, improve with repeated cycles; modules with nominally the same characteristics showed Cold Noise to different extent; some areas of modules were more likely to display Cold Noise than others. The statistical occurrence of Cold Noise complicated investigations into the underlying issue, as modifications required the assembly of several modules in order to test their impact on module performance.

Over the course of the next twelve months, pre-production was halted, so that the limited number of pre-production components was available for investigations into the cause and mechanism of Cold Noise. In a project-wide effort, experts from all involved institutes investigated all aspects of modules that were potential causes of Cold Noise, which revealed individual parts of the overall cause:

- different glues with nominally identical properties led to different amounts of Cold Noise
- increasing the glue layer thickness reduced the observed amount of Cold Noise
- increasing the current drawn by the powerboard increased the extent of Cold Noise

- bypassing the powerboard for module operation (i.e. powering hybrids directly) eliminated Cold Noise
- adding mechanical stiffeners to the powerboard reduced Cold Noise
- adding various options for additional shielding did not impact Cold Noise
- Cold Noise is only observed for module channels located above a glue layer between hybrid and sensor
- the occurrence of Cold Noise shows a phase relationship with the switching frequency of the on-board DC-DC-converter's switching frequency
- inducing vibrations to the powerboard through a transducer produced a similar module noise pattern as Cold Noise.

In 2023, two major observations were made:

Laser vibrometer measurements on SMD components mounted on powerboards revealed that several capacitors showed vibration at about 2 MHz with an amplitude of about 1 nm. These vibrations can couple into the silicon sensor through piezo-electric effects in the glue layer.

Cold Noise measurements of end-cap modules showed no Cold Noise in the production version of end-cap modules, despite utilising a nominally comparable component design that varied mostly in geometry.

The combination of both results provided enough information for a re-evaluation of the existing barrel module powerboard design and its adjustment for an improved noise performance.

For a more complete overview of the performed tests and results, please see the attached overview.

**Thursday posters session / 12**

## **Demonstration of the digital readout chain in the NvDEx experiment**

**Authors:** Lei Lang<sup>1</sup>; Kai Chen<sup>1</sup>

<sup>1</sup> *Central China Normal University*

**Corresponding Authors:** chenkai@ccnu.edu.cn, leilang@mails.ccnu.edu.cn

NvDEx is a proposed experiment to hunt for the neutrinoless double beta decay of  $^{82}\text{Se}$ , with a high pressure  $\text{SeF}_6$  gaseous TPC. The readout and DAQ system are important parts of the experiment. The readout plane placed in one endcap of the TPC consists of around 15,000 sensors for charge measurement. It is crucial to read out data from all of these sensors efficiently. This paper will introduce the design of the demonstrator system for the digital readout chain, including the front-end digital sensor array, the data aggregation module and the DAQ system in the back-end.

### **Summary (500 words):**

Double beta decay has been observed with a few nuclides. However, the neutrinoless double beta decay ( $0\nu\beta\beta$ ) is still unobserved though the lower limit of half-life period has been pushed to magnitude of 1026 years for some nuclides.  $^{82}\text{Se}$  is a nuclide candidate for  $0\nu\beta\beta$  experiment, with the decay energy of about 3 MeV. NvDEx is an experiment for  $0\nu\beta\beta$  detection with a high pressure TPC. For the first step, the NvDEx-100 TPC will be filled with around 100 kg  $\text{SeF}_6$  under 10 atm pressure. The uniqueness of NvDEx is that the charge drifted to the endcap is measured without avalanche amplification. Around 15,000 charge sensors will be placed on the readout plane, on which each sensor will have 6 neighbors with the pitch of 8 mm. Each sensor can measure the charge collected by the electrode on it, then the decay energy and the track of the drifted ions can be calculated. The final version of sensor is expected to include the electrode for charge collection, the Charge-Sensitive-Amplifier for charge measurement, the ADC for pulse digitization and the digital I/O module for data exchange between sensors. Currently the CSA is still under testing, and improvement on the design is needed to achieve 45 e- ENC. The first version of digital I/O ASIC has been taped-out and tested. In this paper we will introduce the design of the DAQ system especially the hardware and firmware, the data aggregation module and the integration with a small digital sensor array for full chain bidirectional digital data transmission.

The DAQ system in the back-end is based on the PCIe infrastructure. A 16-lane PCIe card supporting 24 fiber optical links has been designed. The throughput from the card to the server is around 180 Gbps. The card supports 28 Gbps optical transmission, but slower QSFP modules could be used in the NvDEx

experiment. With the digital I/O, data of the 15,000 sensors will be transferred to the plane edge. In total, there are about 300 digital I/O with speed of about 50 Mbps. A few data aggregation module (DAM) will be placed on the edge of the plane to reduce the quantity of cable connections, which helps to reduce the radioactive background. On one side, high-speed transceiver chips on these modules connect these bidirectional digital I/O. On the other side, the transceivers communicate with the DAQ system via 20 optical links of 1 Gbps. Full digital chain of both directions has been evaluated. For the downlink, commands from the server are encoded in the PCIe card firmware and sent to the DAM. The DAM forwards the 8B10B decoded commands to the digital I/O ASIC, which does the further decoding based on a custom protocol. For the uplink, the encoded data is transferred through the digital I/O chain. The transceiver carries out the 8B10B encoding for data from 16 digital I/O and sends data to the DAQ system. The data is finally sent to the server after decoding in the DAQ firmware.

## Power, Grounding and Shielding / 13

### CMS Outer Tracker Phase-2 Upgrade on-module powering

**Author:** Angelos Zografos<sup>1</sup>

**Co-authors:** Georges Blanchot<sup>1</sup>; Irene Mateos Dominguez<sup>1</sup>; Kevin Schleidweiler<sup>2</sup>; Mark Istvan Kovacs<sup>1</sup>; Patryk Szydlik<sup>3</sup>

<sup>1</sup> CERN

<sup>2</sup> *Ministere des affaires etrangeres et europeennes (FR)*

<sup>3</sup> *Wroclaw University of Science and Technology (PL)*

**Corresponding Author:** angelos.zografos@cern.ch

The Compact Muon Solenoid (CMS) Tracker Phase 2 Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) will use two module types, 2S and PS, which contain different sensor configurations and custom ASICs. Guaranteeing the power integrity of all the built modules and for the full lifetime of the detector is crucial for the detector performance. This article describes the historical evolution of the powering architecture, the problems encountered, and the solutions implemented for the 2S and PS modules, as well as the final on-module powering strategy along with the data and modelling that led to it.

#### Summary (500 words):

Two module types (2S and PS) will be used in the Compact Muon Solenoid (CMS) Tracker Phase 2 Upgrade for the High Luminosity Large Hadron Collider (HL-LHC). The 2S modules contain a double strip sensor configuration with an active area of  $(10 \times 10)$  cm<sup>2</sup>, wire bonded to two front-end hybrids (FEHs) that are powered and controlled by a service hybrid (SEH). The PS modules contain a strip sensor and a macro-pixel sensor of  $(5 \times 10)$  cm<sup>2</sup> wire bonded to two FEHs interconnected with a power hybrid (POH) on one side and with an optical readout hybrid (ROH) on the opposite side.

The 2S and PS modules integrate 2 types of custom ASICs (the bPOL12 and bPOL2V5) in a 2 stage DC-DC conversion scheme in order to deliver the required power to all the data acquisition and control ASICs of the modules. The total consumption of the 2S module when configured for data taking is close to 5W and the PS close to 10W. The voltages needed for the operation of the different ASICs are nominally 1.2V and 2.5V for the 2S case and the same plus 1.0V for the PS.

The module and hybrid designs need to guarantee power integrity for the full range of operating conditions, for all the different modules produced and for the lifetime of the detector operation. Three main parameters are affecting the module power integrity: The output voltage of the DC-DC converters, the effective module power distribution network resistance (including power and ground resistance and connector contact resistance) and finally the current consumption of all the ASICs on the module. Even when considering a fixed design for hybrids and ASICs there is great complexity that arises because of two reasons: First, none of these parameters are in fact stable in time or even the same between different ASICs, hybrids and modules and second, the very small operating voltage margins of the ASICs operating at such low nominal voltages.

The issue of module power integrity was considered since early in the prototyping phase and the hybrids went through multiple changes that targeted specifically the power integrity of the modules. These changes were initially guided by simulations. Later on, prototype module powering data were gathered

in a systematic way. With the hybrids now in the production phase, all the information gathered during the prototyping phase from modules, hybrids and ASICs was used to make complete models regarding the module powering including all the parameters that affect it. With these models, the output voltage of the dc-dc converters could be chosen and a final tweaking of the module design could be performed optimizing for power consumption.

In this contribution the powering architecture and the historical evolution of it will be described along with the lessons learned for the 2S and PS modules. The problems encountered and the solutions implemented will be detailed. Finally, the final on-module powering strategy will be presented along with the data and modelling that led to it.

**Thursday posters session / 14**

## **RD53A Quad Modules Production and QC for the ATLAS Inner Tracker Outer Barrel (OB) Demonstrator.**

**Author:** Yahya A R Khwaira<sup>1</sup>

<sup>1</sup> *Université Paris-Saclay (FR)*

**Corresponding Author:** khwaira@ijclab.in2p3.fr

Thirty-four RD53a Pixel detector modules arriving from different assembly sites are received at CERN in order to be integrated into the ITk demonstrator. The modules will go through different production validation stages, to monitor any performance degradation before the last stage with a full system test on the demonstrator. To mimic real detector services, multiple modules integrated on special mechanical loading supports and cooled down with a Co2 plant are tested. The objective of the demonstrator is to study the module's performance between the reception stage to the final integration operation and to develop the necessary infrastructure needed for testing.

### **Summary (500 words):**

ATLAS innermost detector layer will undergo a broad range of upgrades for the HL-LHC phase. To be able to cope with the new detector design and a large set of modules to be integrated on the ITk, a demonstrator-based project at SR1 facility in CERN is conducted, to test and integrate a large number of Pixel modules equipped with RD53a electronics.

To mimic the ITk detector, a demonstrator project for the outer barrel section is ongoing with 34 modules. RD53a modules will encounter several production operation stages to be loaded on the OB demonstrator and finally integrated with real on-detector services for a full system test of multiple modules. Additionally, to monitor the module's performance from the reception stage to the final system test on the demonstrator, electrical scans ranging from the front-end readout chip to the sensor level are carried out, with an additional X-ray scan to find any open bumps at each production step. Furthermore, the module performance is compared at different production stages to allow a better understanding of any undesired trend of performance degradation.

A comprehensive study will be presented; tracking the main module performance features and applying a newly developed tool to identify, categorize and locate different Pixel defects, to allow a better understanding of any degradation foreseen in the large production phase for the ITk modules and define a detailed quality control (QC) scheme.

Besides, the anticipation of the overall testing stages will quantify the production yield based on module performance. Using the module QC tool, a combined analysis of the electrical scans for the Pixel detector circuit, starting from the digital front-end part towards the sensor is carried out. Indeed, if at any incidence a Pixel defect is found, it will get recorded by the tool and counted for the individual module and later for the total number of Pixel channels in the OB demonstrator project.

This approach is used to tackle the difficulties expected in modules and stave ratings once the ITk production starts. Hence, an envision of the most likely Pixel defects to occur is studied, based on classifying the origin of the Pixel defect failure with the QC tool. Moreover, to enable a deeper understanding of the expected difficulties, the 34 modules Pixel matrices are stacked to identify any specific geographical Pixel region containing any large number of Pixel defects.

In summary, this work is initiated to study in depth the Pixel quad module performance using RD53a front-end electronics, considering the implications of different testing stages during integration in the OB construction. The methodology applied here can be extended or adapted in the future, for the final

module production to allow quick and systematic identification of defects in the module production and on-stave integration.

**Thursday posters session / 16**

## **Silicon photonic, planar coupled, 4-channel WDM transmitter**

**Authors:** Marc Schneider<sup>1</sup>; Marc Schneider<sup>1</sup>

**Co-authors:** Birgit Burger<sup>1</sup>; Frank Simon<sup>1</sup>; Thomas Kühner<sup>1</sup>

<sup>1</sup> *KIT - Karlsruhe Institute of Technology (DE)*

**Corresponding Authors:** marc.schneider@cern.ch, marc.schneider@kit.edu

We report on our current developments towards a silicon photonic, 4-channel wavelength division multiplexed transmitter system with planar fiber chip coupling. The optical core components consisting of the photonic chip and the connecting V-groove mounted glass fibers were assembled with sub-micrometer accuracy on a glass plate with low thermal expansion for a stable fiber chip coupling. This setup is ready to attach the DC-biasing and termination board as well as a fan-out board for 4x10 Gb/s drivers or a 4x32 Gb/s driver board. Experimental results of the optical and optoelectrical performance will be presented.

### **Summary (500 words):**

Optical links using silicon photonic transmitters and wavelength division multiplexing (WDM) are the future in particle detector instrumentation, as single channel links with directly modulated laser diodes are not suitable for the projected radiation levels and data amounts anymore. Using silicon photonic modulators, the optical source can be placed in low-radiation areas and radiation hard devices are used inside the detector volume.

We use 3 mm long Mach-Zehnder type modulators for our 4-channel WDM transmitter system. The wavelength demultiplexing and multiplexing is performed by planar concave gratings on-chip, so that just two optical fibers for input and output are required. The coupling is polarization sensitive and to avoid polarization controllers for each wavelength, a polarization maintaining fiber is used to launch light to the chip.

An overview of the setup is shown in figure a). The WDM chip can be seen in the middle on a 770  $\mu\text{m}$  high, thin-glass platform to match its surface height to the fibers. The angle polished optical fibers for a compact and stable coupling [1] are placed in V-groove chips for positioning and mounting and are located diagonally on the upper left and lower right in the picture. After positioning, all components are fixed on a microscope slide using UV-glue. The low shrinkage of the glue while curing introduces just a negligible increase of coupling loss of less than 1 dB. This might even be decreased by a smaller amount and more precise application of the glue.

A side view of the setup is shown in figure b). The fibers protrude 6 mm from the V-grooves to allow for more space for wire bonding the chip to its electronics. In later setups this can be optimized for a smaller size and higher stability.

Current driver electronics are made of commercial driver ICs and are rather bulky. To attach the 4x10 Gb/s version, we developed a fan-out board, shown on the left side of figure c). It converts SMA connectors for each of the four channels on one side to bondpads with a pitch of 140  $\mu\text{m}$  on the other side for wire bonding to the chip. This board can be replaced by another driver board for data rates of up to 4x32 Gb/s, but with decreased voltage swing. As the transmission lines of the modulators needs termination, a second board with termination resistors will be attached on the other side of the chip. This board, shown on the right side of figure c), also includes the DC-biasing circuitry for the modulators, which consists of two bias-Tees per modulator. For illustration a silicon photonic system chip is placed between the two boards and will be replaced by the setup shown in figure a).

At the time of writing this abstract, electrical tests of the individual modulators are being prepared. Full system performance tests will then be performed after bonding the electrical boards to the chip.

[1] M. Schneider et al., “Planar fiber-chip-coupling using angle-polished polarization maintaining fibers”, JINST, DOI 10.1088/1748-0221/18/01/C01069

**System Design, Description and Operation / 17**

## **HEPS-BPIX40: the upgrade of the hybrid pixel detector for the High Energy Photon Source**

**Authors:** Wei Wei<sup>None</sup>; Jie Zhang<sup>1</sup>; Zhenjie Li<sup>2</sup>; Mingyi Dong<sup>2</sup>; Zhe Li<sup>2</sup>; Xiaolu Ji<sup>2</sup>; Ke Fang<sup>2</sup>; Hangxu Li<sup>2</sup>; Yan Zhang<sup>2</sup>; Si Ma<sup>2</sup>; Zengqiang Gao<sup>2</sup>; Peng Liu<sup>2</sup>; Yuanbai Chen<sup>2</sup>

<sup>1</sup> *Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)*

<sup>2</sup> *IHEP, CAS*

**Corresponding Authors:** jie.z@cern.ch, weiw@ihep.ac.cn

HEPS-BPIX40 is a new hybrid pixel detector for the High Energy Photon Source in China. It is a full upgrade from BPIX20, with a 128 x 96 pixel matrix and 140  $\mu\text{m}$  x 140  $\mu\text{m}$  pixel size. The circuit operates in single photon counting mode with dual thresholds and programmable gains. The tested frame rate is 2 kHz in continuous readout mode. A detector module covers 3.7 cm x 8.1 cm and consists of 2 x 6 chips. The full system will have 40 modules and approximately six million pixels. This paper presents the detector's design and test results.

### **Summary (500 words):**

HEPS-BPIX is a series of hybrid pixel detectors that have been specifically designed for the High Energy Photon Source, which is currently under construction in Beijing, China. Over the past decade, three generations of prototype systems have been designed based on the former version of the BPIX20 chip. It includes a pixel matrix of 104 x 72 pixels, with a pixel size of 150  $\mu\text{m}$  x 150  $\mu\text{m}$ . After ten years of iteration, the demand for a full upgrade of the chip is increasing, especially in terms of periphery interface, pixel working mode, and module assembly enhancement.

We have developed the BPIX40 pixel chip as the successor to the BPIX20. It includes a pixel matrix of 128 x 96 pixels, measuring a pixel size of 140  $\mu\text{m}$  x 140  $\mu\text{m}$ . Dual threshold photon counting mode has been introduced for energy window discrimination, with each threshold having a counting depth of 14 bits, while the maximum counting rate can reach 2 Mcps per pixel. The measured equivalent noise was about 79 e<sup>-</sup> for the bare die, compared with 112 e<sup>-</sup> after bump bonding, using the S-curve method. Meanwhile, the non-uniformity before and after threshold equalization were 402 e<sup>-</sup> and 102 e<sup>-</sup>, respectively.

The chip was designed using CMOS 130 nm 1P8M technology on 12-inch wafers, with a manufacturing yield tested to be better than 93%. Two rows of six chips are to be bumped with a 320- $\mu\text{m}$  thick Si PIN sensor to form a detector module, which covers an area of 3.7 cm x 8.1 cm. In order to minimize the assembly gap between modules, the height of all the periphery circuits has been compressed to less than 600  $\mu\text{m}$ . This way, the dead zone between modules is only determined by the width of the sensor guard ring and the clearance required by wire bonding. Thus, the reliability of module fabrication is greatly enhanced compared to the TSV (through silicon via) technology used in our former systems.

96 columns of the chip were grouped into 12 super columns, each comprising 8 columns with a single readout chain implemented by a shift register. The outputs of all super columns were concentrated into a high-speed serializer and then transmitted off-chip at a data rate of 702 Mbps. At this speed, the frame rate of the chip is about 2 kHz, and deadtimeless continuous readout is supported by the systems for all modules. For the targeted 6M pixel system, the estimated maximum data rate will reach 332 Gbps at this frame rate, which poses a significant challenge for both the backend electronics and the data acquisition system.

Currently, preliminary tests have verified the module and chip design. X-ray imaging results have been obtained by a module (uncalibrated). More detailed results for the full system design will be presented in this paper.

Tuesday posters session / 18

## System level tests of large-scale multi-module prototype structures of the ATLAS ITk pixel detector

**Authors:** Benedikt Vormwald<sup>1</sup>; Helen Hayward<sup>2</sup>

<sup>1</sup> CERN

<sup>2</sup> University of Liverpool (GB)

**Corresponding Authors:** sanha.cheong@cern.ch, benedikt.vormwald@cern.ch

The ATLAS collaboration will replace its inner detector by an all-silicon tracker (ITk) for the HL-LHC. The new pixel detector will cover a sensitive area of 13m<sup>2</sup>. The pixel modules are loaded on light-weight carbon structures in the form of (half)rings and staves. Electrically functional prototypes of these local supports based on the RD53A readout chip were built and extensive system-level tests of these structures were carried out evaluating serial powering, grounding and shielding, system monitoring, and the overall performance of the multi-module detector systems.

In this contribution, the results of these system tests will be presented.

**Summary (500 words):**

The ATLAS collaboration is going to replace its entire inner detector by an all-silicon inner tracker (ITk) in order to be able to cope with the harsh conditions of the HL-LHC in terms of data rate and radiation damage and to extend the tracking to a pseudo rapidity of 4.0. One part of ITk is a new pixel detector made of planar and 3D silicon sensors with an overall sensitive area of 13m<sup>2</sup>. The readout chip is developed by the RD53 collaboration and features serial powering in order to save material in the required power cables. For further material reduction, the detector is going to use 2-phase CO<sub>2</sub> cooling. The detector modules are loaded on light-weight carbon structures in the form of (half)rings and staves which represent feature-complete building blocks of the final pixel detector. Electrically and thermally functional prototypes of these local support structures have been built based on a close-to-final detector design. Extensive tests of these structures on system level have been carried out evaluating aspects like serial powering, grounding and shielding, monitoring, and the overall module performance after the integration into a multi-module detector system. The completion of these tests mark a very important milestone in the prototyping phase of the ITk pixel detector design and allows to transition to pre-production of these detector parts. Valuable experience was gained during the electrical testing of the components (and their interplay) which for the first time work together on the level of local supports. This integration aspect of many different electronics components makes the results very interesting for the audience at TWEPP.

Production, Testing and Reliability / 19

## Hybrid designs and kick-off production experience for the CMS Phase-2 Upgrade

**Author:** Mark Istvan Kovacs<sup>1</sup>

**Co-authors:** Angelos Zografos<sup>1</sup>; Georges Blanchot<sup>1</sup>; Irene Mateos Dominguez<sup>1</sup>; Kevin Schleidweiler<sup>2</sup>; Patryk Szydlik<sup>3</sup>

<sup>1</sup> CERN

<sup>2</sup> Ministère des affaires étrangères et européennes (FR)

<sup>3</sup> Wrocław University of Science and Technology (PL)

**Corresponding Author:** mark.istvan.kovacs@cern.ch

The CMS Tracker Phase-2 Upgrade requires the production of new sensor modules to cope with the requirements of the HL-LHC. The two main building blocks of the Outer Tracker are the Strip-Strip (2S) and Pixel-Strip (PS) modules. All-together 47520 hybrid circuits will be produced to construct 8000 2S and 5880 PS modules. The circuit designs for the mass production were fine tuned and the kick-off batches were manufactured. The presentation will focus on lessons learned from the prototyping stage, design optimization details for the mass production, test results and yield from the kick-off batches.

**Summary (500 words):**

Two main module types were designed and prototyped for the Compact Muon Solenoid (CMS) Tracker Phase-2 Upgrade. The 2S modules are constructed from two co-planar strip sensors of (10 × 10) cm<sup>2</sup>, two front-end hybrids and a service hybrid. The PS modules are more complex, they consist of a strip and a macro pixelated-strip sensor of (5 × 10) cm<sup>2</sup> assembled into a module with two front-end hybrids, a readout hybrid and a power hybrid. The PS readout hybrid ensures the communication with the back-end while the PS power hybrid hosts the DC-DC power converters and powers the electronics. In the 2S service hybrid these two functions are combined in the same circuit. The front-end hybrids are hosting the front-end readout ASICs and concentrator ASICs on both module types.

All circuits are based on a flexible substrate reinforced with carbon-fibre or FR4 stiffeners in the case of the PS power hybrid. The hybrids are using advanced High Density Interconnect (HDI) features such as micro-vias with copper filled laser drills ranging from 25-50 μm diameter, via capture pads of 110 μm diameter and track width and spacing of 45 μm in the critical routing areas. Flip-chip ASICs are bonded to the circuits without additional redistribution layers, therefore via-in-pad technology is used to fan out the 250 μm and 270 μm pitch bump arrays. In order to increase the reliability of the hybrids, high reliability design practices were used, such as staggered vias, teardrops and crosshatched metal structures.

The hybrids were prototyped extensively before launching their production. Various, mostly minor issues were discovered during this phase. In response to the discovered problems, design changes were implemented to improve the performance and the yield of the circuits for the production phase. Due to the high production quantities, even minor changes can reduce the cost of the hybrids significantly.

The 2S and PS front-end hybrids were fitted with noise reduction features and a new alignment design that improves the precision and the yield of the carbon fibre stiffener lamination process. The PS power hybrid and 2S service hybrid designs were modified to achieve lower noise injected into the sensor modules. In order to reduce the risk involved in the modifications, two versions were designed from each circuit, a split-plane version and a regular version. Simulations and system level analysis were made to compare the expected performance of the different designs. The PS readout hybrid was fitted with a light shield to reduce light emissions from the optical transceiver unit.

The presentation will introduce the different hybrid types, the challenges resolved during the prototyping phase and the utilized design techniques. The modifications carried-out on the different hybrid types and the reasons why they were required will be presented. The simulation results will be compared with measured performance for the 2S Service hybrid and PS power hybrid designs. The effectiveness of the modifications such as the achieved noise reduction and yield increase will be presented alongside with the general yield numbers from the kick-off hybrid production.

**Tuesday posters session / 20**

## **A high time resolution and dynamic range monolithic pixel detector-ASIC for Micro Vertex Detector in PANDA experiment**

**Author:** Hui Zhang<sup>None</sup>

**Co-author:** Ivan Peric<sup>1</sup>



<sup>1</sup> *KIT - Karlsruhe Institute of Technology (DE)*

**Corresponding Author:** hui.zhang@kit.edu

A monolithic pixel sensor test chip for PANDA micro-vertex detector has been implemented in 180 nm HVCMOS technology on a high resistivity substrate. The sensor should have very high time resolution (1 ns sigma) and high dynamic range (up to 1000). The pixel electronics contains a Charge Sensitive Amplifier (CSA), a feedback circuit and two comparators. One comparator receives the fast signal and enables accurate time measurement. The other comparator receives the low pass filtered signal and is used for precise amplitude measurement. This publication presents several novel features of PANDA ASIC, its characterization and several measurement results.

**Summary (500 words):**

We are developing a monolithic particle pixel sensor for PANDA micro-vertex experiment. To evaluate the design a test chip has been designed, produced and tested. The test chip contains a pixel matrix with 29 x 64 pixels of 165µm x 50µm size and digital readout circuits. The chip has been implemented in a 180 nm HVCMOS technology on two high resistivity substrates (370 Ωcm and 5 kΩcm). The pixel electronics contains a Charge Sensitive Amplifier (CSA), a feedback circuit and two comparators. One comparator receives the fast signal and enables accurate time measurement. The other comparator receives the low pass filtered signal and is used for precise amplitude measurement. Several novel features have been implemented such as variable gain amplifier and time to digital converter with time-amplification. The design goal is to achieve a time resolution of 1 ns sigma and high dynamic range (1000). The high time resolution can be achieved by the use of two comparators, TDC and by correction of time walk. The high dynamic range can be achieved by the adaptive gain amplifier circuit. The chip has been tested by electric signals. Time resolution of 1.3ns and a dynamic range of 1000 have been measured in this way. Measurements with particles will be done in next weeks.

**Programmable Logic, Design and Verification Tools and Methods / 21**

## **Fault Tolerance Evaluation Study of a RISC-V Microprocessor for HEP Applications**

**Author:** Alexander Walsemann<sup>None</sup>

**Co-authors:** Michael Karagounis <sup>1</sup>; Alexander Stanitzki <sup>2</sup>; Dietmar Tutsch <sup>3</sup>

<sup>1</sup> *Fachhochschule Dortmund Univ. of Applied Sciences and Arts (DE)*

<sup>2</sup> *Fraunhofer IMS*

<sup>3</sup> *University of Wuppertal*

**Corresponding Author:** alexander.walsemann@fh-dortmund.de

The use of a radiation-hard microprocessor or the application of a System-on-Chip (SoC) design methodology has a considerable beneficial impact on the future design of ASICs within the HEP community. The STRV (SEU-tolerant-RISC-V) is a Triple Modular Redundancy (TMR) protected RISC-V microprocessor designed to withstand Single Event Effects (SEE) and operate close to a beamline or interaction point.

The results of evaluation studies on the impact of SEEs on the reliability of a RISC-V microprocessor-based system are presented. These evaluation studies include information derived from extended fault injection simulation and heavy ion testing of STRV-R1 samples.

**Summary (500 words):**

The STRV-R1 is a RISC-V microprocessor designed for the harsh radiation environment found in locations close to the beamline or interaction point, such as the ATLAS and CMS detectors installed at the Large Hadron Collider (LHC). Therefore, the microprocessor must tolerate a total ionizing dose (TID) of 1 GRad and a high single event effect (SEE) rate due to a particle flux of up to 1.5 GHz/cm<sup>2</sup>, which is not possible with current unprotected RISC-V implementations.

The use of a microprocessor, as opposed to the custom digital logic used in current ASICs, is intended to allow the implementation of reprogrammable functions and algorithms, thus enabling flexible and reconfigurable embedded systems. The applications of a RISC-V microprocessor could range from a low-performance control and monitoring of on-detector electronics to high-performance variants intended for data processing of physical events. The integration of a pre-existing verified RISC-V core would enable a SoC design flow that reduces the required design and verification effort, since compared to a fully customized ASIC, only a small portion of the code is customized for the target application, while the rest is handled by the RISC-V core and other pre-existing IP blocks connected to an interconnect bus. The result would be faster development turnarounds and better reusability across multiple designs and applications.

The STRV-R1 has a RISC-V core that implements the RV32I ISA variant and has a three-stage pipeline. An ISA extension for accelerated multiplication and division is also integrated. The system is designed to run at a base clock frequency of 50 MHz and has 32 kB of available SRAM for data and instructions. While the STRV-R1 is intended as a reference platform for evaluation, its specifications are designed to meet the requirements of control and monitoring systems for detector electronics. The STRV-R1 uses Triple Modular Redundancy (TMR) to mitigate errors caused by SEE. The STRV-R1 incorporates a self-refresh algorithm that periodically refreshes the instructions and data stored in the SRAM content independently of the RISC-V core to prevent the critical accumulation of SEUs. TID effects are targeted through the use of 65nm process technology in combination with thin gate oxide transistors.

This contribution will present the results of evaluation studies on the fault tolerance against SEEs achievable with a TMR-based protection scheme. The evaluation studies are performed using a simulation-based fault injection framework to replicate the behavior of different types of single-event effects to trigger functional interrupts in the RISC-V core. The evaluation studies will provide an understanding of the major contributors to functional interrupts and the susceptibility to failure of the primary components of a microprocessor system, such as the pipeline and memories.

Heavy ion irradiation was performed on samples from the STRV-R1. The results of the heavy ion tests will be correlated and compared with the information derived from the simulation-based evaluation of the impact of single event effects.

**Thursday posters session / 23**

## **A Charge-integration Pixel Detector Readout Chip Features High Frame Rate with in-pixel ADCs.**

**Author:** Mujin Li<sup>1</sup>

**Co-authors:** Jie Zhang<sup>2</sup>; Wei Wei

<sup>1</sup> IHEP

<sup>2</sup> Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)

**Corresponding Author:** limujin@ihep.ac.cn

HYLITE (High dYnamic range free electron Laser Imaging deTEctor) is a charge-integration pixel detector readout chip designed for SHINE (Shanghai high repetition rate XFEL and extreme light facility). The chip features a frame rate of 10kHz and a successive readout mode. HYLITE200S is the third prototype chip in the HYLITE series, including correlated double sampling circuits to improve noise performances. The signal-to-noise ratio of the chip with a single 12keV photon injection is 9.31. To achieve high-speed data output, HYLITE200S incorporated a clock management block. Tests demonstrated that the data transmission can be achieved steadily at a speed of 3.125Gbit/s.

**Summary (500 words):**

The charge-integration readout chips of pixel detectors have been widely adopted in XFEL (X-ray Free Electron Laser) facilities. Almost all of them are designed for a specific light source according to the beam feature. SHINE is been built in Shanghai, China. The beam generated by SHINE will be successive pulses with a repetition frequency of 1MHz. Thus, the pixel detectors of SHINE must work in a successive mode

to keep in sync with the beam. HYLITE is the pixel readout chip designed for SHINE with a frame rate of 10kHz and an automatic gain-switching function. To achieve such a high-speed readout in a successive mode, an ADC is integrated in each pixel so that the outputs of pixels are digital signals.

HYLITE200S is the third prototype chip in the HYLITE series with a pixel pitch of 200  $\mu\text{m}$ . Prior to HYLITE200S, HYLITE0.1 and HYLITE0.2 were both manufactured using a 130 nm CMOS process and underwent full testing. The result showed that the in-pixel ADC scheme is successful. However, some issues were not been solved by these two tape-outs. For example, the signal-to-noise ratio of the original pixel is 2.31, which cannot fulfill the requirement of a single photon resolution of 12 keV. To improve the noise performance, a CDS (Correlated Double Sampling) circuit was added to the HYLITE200S pixel to mitigate the reset noise. The signal-to-noise ratio on the high gain stage of HYLITE200F is 9.31.

The I/O pads of a pixel readout chip are limited due to the single-side I/O structure. However, the amount of control signals in a HYLITE chip is large as many switch-capacitor circuits are adopted. A frame logic was designed to generate ten control signals according to two external signals: a clock and a frame refresh signal. Timing of the generated signals can be configured by a common SPI bus.

The array size of the full-size chip will be  $128 \times 128$ , resulting in a data rate of 3.28Gbit/s per single chip. In the full-size chip architecture, two high-speed serializers and corresponding CML (Current Logic Logic) drivers will be adopted. To validate the design, a clock management block and a high-speed data port were integrated into the periphery of HYLITE200S. The clock management block consists of a PLL (Phase Lock Loop) and a frequency divider. The high-speed data port includes an 8b10b encoding logic, a serializer, and a differential CML driver. An eye diagram analysis confirmed that the data port operates effectively at a data rate of 2 Gbit/s. By FPGA decoding, the data rate was further proved at 3.125 Gbit/s. These results demonstrate the successful design of the clock management block and the data port. In the next step, a full-size chip of HYLITE will be produced on the basis of HYLITE200S.

## Tuesday posters session / 24

# Prototype electronics for the silicon pad layers of the future Forward Calorimeter (FoCal) of the ALICE experiment at the LHC

**Authors:** Carolina Arata<sup>1</sup>; Damien Tourres<sup>1</sup>; Jean-Luc Bouly<sup>1</sup>; Nicolas Ponchant<sup>2</sup>; Olivier Bourrion<sup>1</sup>; Rachid Guernane<sup>1</sup>

<sup>1</sup> Centre National de la Recherche Scientifique (FR)

<sup>2</sup> CNRS/IN2P3/LPSC

**Corresponding Author:** olivier.bourrion@lpsc.in2p3.fr

A new Forward Calorimeter (FoCal) system has been proposed as part of the ALICE upgrades planned for LHC Run 4 which features a Si+W electromagnetic calorimeter. A first tower prototype corresponding to 1/5 of the nominal module of the electromagnetic calorimeter has been built in 2022. It is composed of 20 passive layers of tungsten absorber interleaved with 18 active layers of low-granularity silicon pads. Each pad layer is read out by 110 silicon pad sensors of 72 channels, amounting to a total of 1980 channels. This contribution describes the electronics developed from front-end to back-end.

## Summary (500 words):

The prototype tower is a sandwich of tungsten and silicon sensors covering a surface of about  $9 \times 8 \text{ cm}^2$ . The sensors are 320  $\mu\text{m}$ -thick p-type silicon PIN photodiode arrays segmented into 72 cells (plus two calibration cells of smaller size). The front-end solution used for the silicon sensor readout is the High Granularity Calorimeter Readout Chip (HGCROC) Application Specific Integrated Circuit (ASIC) developed for the CMS High Granularity Calorimeter (HGCAL). Dedicated printed circuit board (PCB), named "single pad boards", were designed and fabricated to accommodate the silicon pad sensors glued on one side and the very front-end electronic components mounted on the other side. The sensors are wire-bonded to the single pad boards through sensor access

holes for wire bonding.

The single pad board design was first validated with an FPGA evaluation kit and an external charge injection board (72 channels). This charge injector board, featuring an FPGA and driven synchronously by the acquisition electronics permitted the qualification of the 18 single pad boards before prototype assembly.

The 18 single pad boards are connected through a proprietary interface board, to a dedicated control and readout board, named “aggregator”. This board features a single FPGA that drives synchronously the 18 HGCROCs with a total of 36 downstream links, gathers the data provided in return by the 144 readout links and configures the ASICs via I2C links.

Each front-end ASIC is clocked by a eight-time multiple of the LHC machine frequency (320 MHz), triggered through a fast serial command link (320 Mbps) and read-out by four high speed links (each working at 1280 Mbps). Upon trigger reception, the HGCROC provides three measurements (ADC, TOA, and TOT) for each of its 72 channels.

The aggregator board handles the raw data and permits to either interface the prototype with the ALICE data acquisition through GBT links or with a standalone computer through Ethernet for in lab test and characterization. Without zero suppression and using the GBT links a maximum trigger rate of 33 kHz can be reached to record the 1296 channels.

To speed up firmware and software validation, several test features were embedded in the aggregator such as front-end fake data generators, ALICE Central Trigger Processor message generator. This enabled fast prototype commissioning in preparation for the three test beams conducted at CERN PS and SPS with the official ALICE O2 DAQ system.

This contribution describes, the electronics architecture, the technological choices and the firmwares developed to instrument a tower prototype composed of 18 silicon pad sensors. The companion tools developed will be presented as well.

ASIC / 25

## Development of monolithic pixel sensor prototypes for the CEPC vertex detector

**Author:** ZHANG Ying zhangying83<sup>None</sup>

**Co-authors:** Wei Wei ; Jun Hu ; Xiaomin WEI ; Xiaoting Li <sup>1</sup>; Liang ZHANG <sup>2</sup>; Tianya Wu <sup>3</sup>; Jia Wang <sup>4</sup>; Ziyue Yan <sup>1</sup>; Xiaoxu Zhang <sup>3</sup>; Wei Wang <sup>1</sup>; Shuqi Li <sup>1</sup>; Jia Zhou <sup>1</sup>; Xinhui Huang <sup>1</sup>; Jianing Dong <sup>2</sup>; Zhijun Liang <sup>1</sup>; Hongyu Zhang <sup>1</sup>; Mingyi Dong <sup>1</sup>; Raimon Casanova <sup>6</sup>; Lei Zhang <sup>5</sup>; Ming Qi <sup>2</sup>; Sebastian Grinstein <sup>6</sup>; Joao Guimaraes da Costa <sup>1</sup>

<sup>1</sup> IHEP

<sup>2</sup> Shandong University

<sup>3</sup> Chinese Academy of Sciences (CN)

<sup>4</sup> NWPUP

<sup>5</sup> Nanjing University

<sup>6</sup> IFAE

**Corresponding Authors:** weiw@ihep.ac.cn, zhangying83@ihep.ac.cn

The TaichuPix chip is a dedicated monolithic CMOS pixel sensor that is being developed for the first 6-layer silicon vertex detector prototype of the Circular Electron Positron Collider (CEPC) vertex detector R&D. Two small-scale demonstrator chips (25 mm<sup>2</sup>) had been designed to optimize the in-pixel circuit and readout architecture, and to verify the radiation hardness. The positive results of the small-scale prototypes led to a submission of the first full-scale (2.6 cm × 1.6 cm) TaichuPix prototype in 2022. The design details and test results of TaichuPix prototypes and development of the readout electronics will be given.

**Summary (500 words):**

The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption. The TaichuPix chip need to provide a spatial resolution better than 5 μm, a power density lower than 200 mW/cm<sup>2</sup>, and

a Total Ionizing Dose (TID) tolerance higher than 1 MRad. Fig.1 shows the architecture of a full-scale TaichuPix chip, including a matrix of  $512 \times 1024$  pixels with a size of  $25 \times 25 \mu\text{m}^2$ . Each pixel integrated a sensing diode, a front-end and a hit storage registers and logic for pixel mask and test. Pixels are arranged in double columns, with priority encoder within column and timestamp recorded at the end of double column (EOC). All the 512 double columns are read out in parallel, in order to minimize the dead time. For each double column, a fast-or busy signal delivers to the EOC when any pixel generates a hit signal. The timestamp with a resolution of 25 ns is generated whenever a new fast-or busy signal is received. Fired pixels in the same cluster share a common timestamp as the Trigger ID. The pixel addresses of the fired pixels are temporarily stored in a column level FIFO (FIFO1). The 512 double columns and the corresponding EOC logics are divided to 4 blocks, and each one integrating a chip level FIFO (FIFO2). There are four groups in each block with each group including 32 double columns. The 32 FIFO1 inside each group are read out according the address priority, while the 4 groups are read out sequentially to the FIFO2. The four FIFO2 are read out through a hierarchical data multiplier. The readout of TaichuPix chip is compatible to both trigger and trigger-less modes.

Two small-scale prototypes have been developed and characterized to address the chip architecture and major functionalities. The test results show the average pixel noise is 10-29 e<sup>-</sup> and the threshold dispersion is 25-58 e<sup>-</sup>, depending on the pixel variants. One of the two parallel in-pixel digital designs is properly operating at a 40 MHz clock. The tests with X-ray and <sup>90</sup>Sr sources proved the functionality of the pixel array and digital periphery. The highest serial data transmission rate is tested to be 3.36 Gbps. The positive results of the small-scale prototypes led to a submission of the first full-scale ( $2.6 \text{ cm} \times 1.6 \text{ cm}$ ) TaichuPix-3 prototype in 2022.

To verify the spatial resolution of the sensor prototype, a beam telescope based on TaichuPix-3 chips was built. The readout electronics for both the single sensor and the telescope have been developed (see Fig.2). The full-scale sensor chip was characterized at the DESY test beam facility. The preliminary results indicate that the best spatial resolution of the individual TaichuPix-3 sensor is better than  $5 \mu\text{m}$  combined with a detection resolution of around 99% (see Fig.3). The TaichuPix-3 also fulfill the power consumption and TID tolerance requirements.

## System Design, Description and Operation / 26

### ALICE ITS3: a bent stitched MAPS-based vertex detector

**Author:** Ola Slettevoll Groettvik<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** ola.slettevoll.groettvik@cern.ch

ALICE ITS3 is a novel vertex detector replacing the innermost layers of ITS2 during LS3. Composed of three truly cylindrical layers of wafer-sized 65 nm stitched Monolithic Active Pixel Sensors, ITS3 provides high-resolution tracking of charged particles generated in heavy-ion collisions. This contribution presents an overview of the ITS3 detector, highlighting its design features, integration and cooling, and the latest results from the ongoing development towards the final sensor. Furthermore, the presentation introduces the off-detector service electronics, which play an essential role in the readout, control, and power supply of the detector.

#### Summary (500 words):

The ALICE Inner Tracking System (ITS) is a key component of the ALICE experiment, providing precise tracking of charged particles produced in heavy-ion collisions. ITS3, the third version of ITS, will replace the Inner Barrel of ITS2 during the LHC Long Shutdown 3 (2026-28). The novel detector consists of three truly cylindrical layers of wafer-scale stitched Monolithic Active Pixel Sensors in 65 nm technology. The sensors are thinned down to below  $50 \mu\text{m}$  and bent at specific radii for each layer to create the cylindrical shape. The innermost layer of ITS3 is positioned just 18 mm from the interaction point and the detector has an unprecedentedly low material budget of  $0.05\%X_0$ .

The reduced material budget of ITS3 is made possible by eliminating water cooling and instead relying on low-speed airflow at  $< 2 \text{ ms}^{-1}$ , which is feasible due to a low power density of  $< 20 \text{ mW cm}^{-2}$ . At the periphery of the sensor, where the power density is higher, carbon foam rings act as radiators to improve heat exchange with airflow. Power and signal are routed on the detector silicon to avoid an FPC

in the active area, further decreasing the material budget. Ultimately, the detector material comprises primarily of the Si of the sensor chip and the carbon of localized foam spacers.

Two prototypes of stitched sensor chips developed with CERN EP R&D, the MOlonithic Stitched Sensor (MOSS) and MOlonithic Stitched Timing (MOST), were submitted with Engineering Run 1 (ER1) in Q4 of 2022, and the wafer arrived for testing at CERN in Q2 2023. MOSS, which measures 14 mm × 259 mm, composes 10 stitched repeatable sensor units that can be powered and interfaced individually or collectively via the chip backbone addition using an endcap unit. An extensive testing campaign aims to verify that inter-stitch power and data routing is feasible with reasonable yield.

A MOSS successor, the ITS3 sensor prototype, will be submitted with Engineering Run 2 (ER2) in Q2 of 2024. The ER2 chip has been optimized in terms of power, using on-chip regulation to maintain voltage level and introduces high-granularity power domain segmentation to accurately handle on-chip shorts. Multiple high-speed data links per chip segment of 10.24 Gbps transmit data upstream. The data is encoded using the lpGBT-scheme in order to transmit data with negligible bit- and frame-error rates.

The ITS3 off-detector service electronics are using an alternative approach to the ITS2 service electronics. Its components will be located at a distance of 0.2 m to 0.4 m from the edge of the sensors, in the service barrel of the detector, still within the acceptance of the forward detectors of the experiment. The high-speed data links are connected directly to optical transceivers (VTRx+) within 0.5m and fibers of up to 135m are drawn directly to the backend electronics avoiding data processing in the radiation environment. The detector powering is based upon radiation-hard DC/DC converters.

This contribution provides an overview of the various aspects of the ITS3 detector, including integration, cooling, chip development, and readout architecture.

## Tuesday posters session / 27

# Software mitigation scheme to increase availability under the radiation of microcontroller-based design for LHC accelerator environment

**Author:** Alessandro Zimmaro<sup>1</sup>

**Co-authors:** Alessandro Masi<sup>2</sup>; Jerome Boch; Rudy Ferraro<sup>2</sup>; Salvatore Danzeca<sup>2</sup>; frederic saigne

<sup>1</sup> *Universite Montpellier II (FR)*

<sup>2</sup> *CERN*

**Corresponding Author:** alessandro.zimmaro@cern.ch

This paper addresses the challenge of mitigating the effects of radiation on the electronic systems of the Large Hadron Collider (LHC) by introducing BatMon, a battery-powered, MCU-based wireless radiation monitoring system. The paper proposes software mitigation schemes that can be used alongside an external watchdog to guarantee higher availability of the application without impacting the system performance. Tests conducted at the CHARM facility show that the proposed schemes enable BatMon to achieve 99.9996% availability in the harsh environment of the LHC. The manuscript highlights that the result obtained will also allow the system to be used for critical tasks.

### Summary (500 words):

The LHC employs numerous electronic systems, including high-criticality and low-criticality applications, with the latter increasingly utilizing off-the-shelf Commercial Off-The-Shelf (COTS) MicroControllers Units (MCU) for cost, power, size, and flexibility advantages. In this complex environment, single-event effects (SEE) can have a strong impact on the reliability of these systems, requiring effective mitigation schemes to ensure high system availability during operation.

This paper introduces the BatMon, an MCU-based battery-powered wireless radiation monitoring system for the LHC. It is designed with qualified low-power COTS components, uses LoRa wireless transmission technology and can tolerate up to 275 Gy. It is modular allowing the platform to be application

independent and be used for different purposes. It embeds an external watchdog as a hardware mitigation scheme to cover possible failures due to SEE. However, it alone cannot detect all possible SEFIs and consequently cannot always restore the system functionalities. An example is the case of the MCU stacked in a while loop due to a SEE: the MCU will continue to serve the external interrupt toggled by the external watchdog. As consequence, the failure will remain undetectable and the device not operational.

The primary aim of this work is the definition of software mitigation strategies that can be employed alongside an external watchdog, while maintaining high performance and compatibility with any MCU-based design. These schemes include triplication of the counters, storage of the configuration and previous measurements in internal flash memory, an internal software watchdog, an automatic dummy-handler recovery scheme, and control of the wireless communication link. Triplication of the counters and storing the configuration and previous measurements in an internal flash can help identify and correct errors due to SEE in the MCU SRAM. The internal software watchdog supervises software execution and prevents the non-detection of errors. Finally, the control of the wireless communication link guarantees reliable communication. These strategies can be classified into three groups based on their usage requirements: C-0, which does not require any peripheral; C-1, which necessitates internal or external hardware peripherals; and C-2, which requires an acknowledgment from an external source, such as a network. This paper will explain this classification in greater detail, outlining the necessary prerequisites for a system to implement these mitigation strategies.

The effectiveness of the proposed software mitigation schemes is demonstrated through a comparison of system availability under radiation. In this work tests conducted at CHARM facility compare the performance of BatMon with and without the implemented software mitigation techniques. The results show that the proposed schemes enable BatMon to achieve an availability of 99.9996% in the harsh LHC environment. The downtime would be related to self-recovery time. This availability agrees with the requirements defined by CERN for a critical system for the LHC which corresponds to 99.537%. Although radiation monitoring is not a critical task for the accelerator and does not have to fulfil these requirements, since the BatMon is application-independent, compliance with these constraints allows it to be used for critical tasks such as equipment control and reset in the future.

ASIC / 28

## SET sensitivity study of a VCRO-based PLL for HL-LHC ATLAS HGTD

**Author:** Maxime Morenas<sup>1</sup>

**Co-authors:** Christophe De La Taille<sup>1</sup>; Damien Thienpont<sup>2</sup>; Elena Vernazza<sup>3</sup>; Nathalie Seguin-Moreau<sup>2</sup>

<sup>1</sup> OMEGA (FR)

<sup>2</sup> OMEGA - Ecole Polytechnique - CNRS/IN2P3

<sup>3</sup> Centre National de la Recherche Scientifique (FR)

**Corresponding Author:** maxime.morenas@cern.ch

We report the characterization of the Single Effect Transient (SET) sensitivity of an analogue Phase-Locked Loop under a 63 MeV proton beam of instantaneous fluence  $10^{10}$  protons/cm<sup>2</sup>/s. The clock generator is embedded in a front-end ASIC, namely ALTIROC designed in CMOS 130 nm, reading out Low-Gain Avalanche Diode (LGAD) for the High-Luminosity Large Hadron Collider (HL-LHC). Observed SET-induced phase jumps allow the estimation of the total cross-section of the PLL. Results are extrapolated to the HL-LHC radiation conditions.

### Summary (500 words):

As part of the ATLAS experiment Phase-II upgrade, the High Granularity Timing Detector (HGTD) will offer a time resolution better than 35 ps RMS per hit for collected charges over 10 fC. An internal PLL provides 1.28 GHz clock from which is derived a 40 MHz clock used for the timing measurement. Designed in CMOS 130 nm as part of the front-end read-out ASIC ALTIROC, the PLL must therefore exhibit a low sensitivity to Single-Event Transient (SET) so as not to corrupt the clock reference and thus the timing data. Furthermore, output data are serialized at a maximum rate of 1.28 Gbps, but serializer

logic is prone to failures such as bit flips when the clock exhibits transient phase errors. Thus, the reliability of the serializer depends on the SET sensitivity of the PLL. Therefore, the phase detector and the feedback clock divider were triplicated while the charge pump, the low-pass filter and the voltage-controlled ring oscillator were not specifically SEE-hardened.

Proton-beam campaigns were conducted in the ARRONAX facility (Nantes, France) which provides a 63 MeV proton with an instantaneous fluence of  $10^{10}$  protons/cm<sup>2</sup>/s (i.e. 2 to 3 orders of magnitude higher than HL-LHC conditions). The proton flux was estimated measuring both the beam diameter with a radio-chromic film and the current of a photomultiplier from an ionization chamber. Tests reported a large variety of SET occurring predominantly in the VCO, identified as frequency transients and in other parts of the design. Peak phase errors up to several tens of nanoseconds were measured with a total cross-section of 4 10<sup>-12</sup> cm<sup>2</sup> (accounting for all phase error amplitudes observed).

With a 10 ps RMS dominant random jitter, the PLL jitter envelop can easily be disturbed by SET, even by low amplitude phase errors. Consequently, the peak phase error is not an appropriate metric for the figure of merit of the SET sensitivity for HGTD. Instead, the timing requirements call for reducing the fraction of the time the PLL provides a wrong clock phase. This estimation can be obtained knowing both the total cross-section and the recovery time of the phase error. Measurements have shown a recovery time below 5  $\mu$ s. Using conservative data regarding the HL-LHC radiation environment (safety factor of 3 for SEE, giving a flux of 1E8 cm<sup>-2</sup>s<sup>-1</sup> for hadrons above 20 MeV), the time corruption rate can be extrapolated to 5 minutes per year of operation of the full HGTD detector (16k PLL running simultaneously). Note that the cross-section estimation relies strongly on the phase error sensitivity. As SET affecting the VCRO produce large phase deviations due to its intrinsic large voltage-to-frequency gain, SET phase jumps were detected using a Lecroy Waverunner 640Zi. Using the “smart trigger” time interval functionality, the oscilloscope allowed for a period deviation sensitivity of  $\pm 200$  ps around the nominal period of the 40 MHz clock monitored.

Details of the triplication implemented in this PLL along with characterisation results will be presented.

#### Thursday posters session / 29

## A Low-Power Gated-Vernier Ring Oscillator TDC for Cryogenic Detectors

**Author:** Soumyajit Mandal<sup>None</sup>

**Co-authors:** Sanjeevi S. Karri<sup>1</sup>; Vamsy P. Chodavarapu<sup>1</sup>; Grzegorz Deptuch<sup>2</sup>

<sup>1</sup> Prixarc, LLC

<sup>2</sup> Brookhaven National Laboratory (US)

**Corresponding Author:** smandal@bnl.gov

High-resolution time-to-digital converters (TDCs) are required for time-of-flight measurements in many applications, including particle identification for high-energy physics. FPGA-based TDCs are popular for such applications but suffer from limited resolution and high power consumption compared to custom ASICs. Full-custom TDC designs can also be integrated within multi-channel or pixelated front-end ASICs, thus eliminating power-hungry low-latency links to external FPGAs. Several applications for such integrated TDCs, such as photon time stamping in rare-event searches, also require cooled detectors and front-end electronics. Here we describe a full-custom TDC in 90nm CMOS technology designed for high-resolution and low-power operation in such cryogenic environments.

#### Summary (500 words):

Key requirements for a cryogenic TDC include high resolution, wide dynamic range (DR), low power consumption, and minimal hardware usage. The proposed design uses ring oscillators (ROs) to improve the trade-off between these parameters relative to delay-line based flash TDCs. Specifically, the number of open-loop delay stages required for a full-scale range of  $T_{max}$  is given by  $N = T_{max}/\Delta$ , where  $\Delta$  is



the resolution. By contrast, RO-based TDCs have unlimited DR since the “start” signal continuously circulates through a set of delay stages. Fig. 1 shows a generic model for an oscillator-based TDC. The oscillator is switched between two operating modes, with the control signal being generated by a logic circuit (the oscillator controller) based on the “start” and “stop” signals. A phase processor uses an array of arbiters to sample the oscillator output, thus generating the TDC output code.

The resolution of RO-based TDC architectures can be improved by using the Vernier principle. Here we describe a 12-bit gated Vernier RO (GVRO) that combines high resolution with large DR, small layout area, and low power consumption. The time difference,  $T_{meas}$ , is quantized by comparing the multi-phase signals generated by slow and fast ROs that are triggered to start oscillating at the rising edges of “start” and “stop”, respectively. The slow RO acquires extra phase during the  $T_{meas}$  interval, so the time required for the fast RO to catch up with it becomes proportional to  $T_{meas}$ . An arbiter detects this coincidence event, and  $T_{meas}$  is quantized by counting the number of RO edges that have elapsed until the arbiter changes state.

Fig. 2 shows a block diagram of the proposed GVRO TDC, which uses the SkyWater S90 90nm bulk CMOS process and was simulated using cryogenic device models (45-150K). The design uses 1) fully-differential 8-stage ROs; 2) dynamic TSPC flip-flops to minimize propagation delays; 3) custom dynamic latches as arbiters; and 4) single-transition end-of-conversion (EOC) detectors to minimize the number of logic transitions during each conversion. The 4-bit output of the EOC detectors provides a thermometer-coded version of the LSB outputs. The next 4 bits are generated by counting cycles of the fast RO after the “stop” signal has been detected. Finally, the 4 MSB bits are generated by counting cycles of the slow RO during the  $T_{meas}$  interval.

The simulated performance of the TDC at 300K and 77K is summarized in Table 1. The proposed design has good resolution (5-6ps) and high DR (30ns, can be extended) with low power consumption (<1.1mW at 1.0V). Chip layout area is also expected to be small since the two ROs use a combined total of only 16 delay stages. Post-fabrication linearity (as quantified by INL and DNL) will be improved via digital correction of the raw TDC output, i.e., populating an on-chip lookup table (LUT) during foreground calibration by using the statistical code density test (CDT) method.

Thursday posters session / 32

## A High Time Resolution Monolithic Active Pixel Sensor with Node-Based, Data Driven and Parallel Readout for Vertex Detector in particle physics Experiments

**Authors:** Le Xiao<sup>None</sup>; Xiangming Sun<sup>None</sup>; Bihui You<sup>None</sup>

**Corresponding Author:** lexiao@mails.ccnu.edu.cn

We present the design of a high-time resolution MAPS sensor prototype MIC6\_V1 based on a 55nm Quad-well CMOS Image Sensor process for the high energy physics experiment vertex detector application. In order to achieve high-spatial resolution, fast readout, and low power consumption, MIC6\_V1 has implemented a new node-based, data-driven parallel readout architecture. The integration time is 5 $\mu$ s, and by sharing VCO in the pixel group, the hit arrival time resolution can reach 10ns. The pixel size of MIC6\_V1 is 23.6 $\mu$ m  $\times$  20 $\mu$ m. The pixel matrix is 64 rows by 64 columns, and the size of MIC6\_V1 is 2.8mm  $\times$  2.8mm.

### Summary (500 words):

The vertex detector in high energy physics experiment requires high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) is the most promising candidate technology to satisfy all those requirements. We have developed the MAPS sensor MIC6\_V1 in a 55 nm quad-well CMOS image sensor process with a node-based data-driven readout scheme.

MIC6\_V1 contains a pixel matrix of 64 rows by 64 columns with a pixel size of 23.6  $\mu$ m 20  $\mu$ m. Each pixel contains a sensing diode, an amplification, a discriminator, and a hit storage register connected to a node-based sparse readout circuitry. Every double-column of pixels share a readout circuit, and

42 pixels form a super pixel group. The 8 pixels in each super pixel share a VCO for hit arrival time measurement. The VCO oscillates only when the super pixel group is hit to reduce power consumption. The oscillation frequency of VCO can be configured between 100 ~ 200 MHz. Each super pixel also includes a node of sparse readout logic circuit, and the hit information will be asynchronously transmitted to the bottom of the double-column through the readout nodes. Readout nodes transmit data based on request-acknowledge handshake protocol. When a super pixel group is hit, 22 bit data will be generated, including 4-bit super pixel group address, 10-bit time counter and 8-bit hit shape.

In the bottom of MIC6\_V1, a periphery readout module also based on asynchronous readout node has been implemented to readout 22-bit data and 5-bit column address from each double-column. Then, a synchronizer module is connected to the peripheral readout module, which is responsible for processing handshake, data synchronization, data bit-width conversion, and finally outputting the data. In addition, an asynchronous handshake multiplexer module is implemented, through which any double-column can be tested independently.

The test system is being developed and consists of a test board, a Kinex-7 FPGA and control software. The test firmware and software are based on IPbus. The 1 Gbps Ethernet interface, IPbus master, and IPbus slavers are implemented in the FPGA. The test commands from the control software on PC are received by the 1 Gbps TCP/IP module and then transmitted to IPbus master. The commands from the IPbus master are sent to one of the IPbus slavers. The current DAC, voltage DAC and the MIC6\_V1 are configured by the respective IPbus slaver. The data flow of the MIC6\_V1 is opposite to the flow of test command. The output data of MIC6\_V1 are transmitted to PC through ipbus slave, ipbus master and Ethernet interfaces in turn. The test results of MIC6\_V1 will be presented in the workshop.

ASIC / 33

## The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results

**Author:** Gianluca Aglieri Rinella<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** gianluca.aglieri.rinella@cern.ch

The MOSS (Monolithic Stitched Sensor) chip is a monolithic pixel prototype chip measuring  $(25.9\text{ cm}) \times (1.4\text{ cm})$ . It was designed to explore the stitching technique, to investigate the achievable yield and as a proof of concepts for the sensors for the ALICE ITS3 upgrade. It was manufactured in early 2023.

This submission will focus on the MOSS chip and on its testing. It will give an overview of the chip and describe the system developed to characterize it. It will report on the early experience of testing in the laboratory and include the first experimental results.

**Summary (500 words):**

The ALICE ITS3 upgrade project aims at replacing the three innermost layers of the current ALICE tracker during the LHC Long Shutdown 3. The new layers will be made with single die sensors implemented in a 65 nm CMOS Imaging Process and with dimensions up to  $(266\text{ mm}) \times (92\text{ mm})$ . This can be achieved using stitching, a technique to manufacture modular chips that are much larger than the design reticle. The sensors will be thinned below  $50\text{ }\mu\text{m}$  and bent as true half-cylinders.

The MOSS (Monolithic Stitched Sensor) chip is a monolithic pixel prototype chip measuring  $(25.9\text{ cm}) \times (1.4\text{ cm})$  (fig. 1). It was designed in 2022 to explore stitching, to investigate the yield and as proof of concepts for the ALICE ITS3 sensor developments. Its manufacturing was completed in April 2023.

The MOSS chip is made abutting ten Repeated Sensor Units (RSU) of  $(25.5\text{ mm}) \times (14\text{ mm})$  and two small end-cap regions at the two sides of the abutted RSUs. Each RSU is subdivided in two half-units. The top one contains four pixel arrays of  $(256 \times 256)$  pixels with a pitch of  $(22.5\text{ }\mu\text{m})$  while the bottom unit contains four arrays of  $(320 \times 320)$  pixels with a pitch of  $(18\text{ }\mu\text{m})$ . The two halves differ for the densities of circuits and interconnects, in order to investigate the potential impact on yield of layout density. The MOSS chip contains 20 half units and 6.72 million pixels. It has 107 supply or biasing nets, 2192 bonding pads, 390 digital and 480 analog I/Os. The design contains interconnects crossing the stitching boundaries to transfer data over distances reaching  $(26\text{ cm})$ , entirely on die. Metal stripes of every power domain also traverse the stitching boundaries.

The testing of such a complex chip presented several challenges. There was no previous experience with the handling and bonding on carriers of chips of such dimensions. The supply domains, I/Os and internal blocks are remarkably numerous. At least few tens of samples need to be tested accurately to address questions related to yield quantitatively.

An electronic system was developed to enable the semi-automated testing of MOSS chips. This system consists of one large Carrier, 5 Proximity Boards and 5 Automation boards (fig. 2). The Carrier is a custom board with features to facilitate gluing and bonding of the chip. Die picking and wire bonding required adapting techniques and developing tools. The Proximity Board is a custom PCBA with many programmable components providing supplies, biasing and analog monitoring. The Automation board is a commercial FPGA based board. It interfaces to the lab host computer, to the Proximity Board and to the MOSS chip through it.

This submission will focus on the MOSS chip design, testing and the related challenges. It will describe the chip and the hardware system developed to characterize it. It will present the test plans and the first experience from testing in the laboratory. The first test results are expected to become available by the time of the workshop and will be included in the contribution.

**Tuesday posters session / 34**

## **The Prototype Design of PEB - a Component of the HGTD In-detector Electronics for the ATLAS Phase-II Upgrade**

**Authors:** Jie Zhang<sup>1</sup>; Lucia Castillo Garcia<sup>2</sup>

<sup>1</sup> *Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)*

<sup>2</sup> *IFAE - Barcelona (ES)*

**Corresponding Author:** jie.z@cern.ch

The HGTD is a novel detector introduced to augment the new all-silicon Inner Tracker in the pseudo-rapidity range from 2.4 to 4.0, adding the capability to measure charged-particle trajectories in time as well as space.

A prototype of Peripheral Electronics Board (PEB), which supports up to 55 front-end modules with 12 lpGBT, 9 VTRx+ and 52 bPOL12v, is developed to work as a bridge between the front-end modules and the off-detector TDAQ.

The on-going R&D effort carried out to study the readout and transmission chips, and the other components, supported by laboratory results, will also be presented.

**Summary (500 words):**

The increase of the particle flux (pile-up) at the HL-LHC with instantaneous luminosities up to  $\sim 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$  will have a severe impact on the ATLAS detector reconstruction and trigger performance. The High Granularity Timing Detector (HGTD), an ATLAS Phase II upgrade project, will provide an accurate measurement of the time of the tracks ( $< 50 \text{ ps}$ ) in order to mitigate the effect of the pile-up in the object reconstruction as the jets, the electrons or the b-jets. In addition, the number of collected hits being proportional to the luminosity, it will provide an instantaneous measurement of the luminosity, which will be read out at 40 MHz.

HGTD is composed of 8032 front-end modules. Each module consists of two Low Gain Avalanche Detectors (LGADs) of approximately  $2 \times 2 \text{ cm}^2$  bump-bonded to two ATLAS LGAD Timing Integrated Read-Out Chips (ALTIROC) and held together by a module flex (flexible PCB). These modules are arranged with overlap on the two sides on each disk. In order to facilitate the detector assembly, the modules will be mounted on support units forming detector units (a detector unit is a support unit with modules mounted on it). Each module will be connected to the Peripheral Electronic Boards (PEB) through a flex tail (another flexible PCB). The detector units and PEBs will be mounted on the HGTD cooling plates. The connections between on-detector and off-detector electronics are performed via optical fibers, high/low voltage cables, interlock cables and monitoring signal cables. The PEB acts as a bridge between the front-end modules and the off-detector systems. The optical fibers provide shared data streams for Timing, Trigger and Control (TTC), Detector Control System (DCS) and Data Acquisition System (DAQ), and dedicated data streams for the luminosity system.

For error-free data transmission at the bandwidths (320 Mbps, 640 Mbps, or 1.28 Gbps) required by the expected HGTD data volume, the PEB uses the low-power GigaBit Transmission chip (lpGBT) and the Versatile Link + Transceiver (VTRx+). The PEB also includes the 12 V to 1.2 V DC-DC converters (bPOL12v) for the digital and analogue voltages supplied to the front-end modules. The supply voltages are monitored using the internal multiplexed ADC on the lpGBTs. Since the input channel number of this ADC is limited to 8, a multiplexing chip is required to handle all the signals connected to PEB. A full custom 64-to-1 multiplexing ASIC (MUX64) has been developed with a radiation tolerance suitable for its implementation on the PEB.

According to the optimization of mirror structure for the layout of the modules, 6 types of PEBs need to be designed for HGTD. Based on previous development experience, the PEB 1F was chosen to be designed first as a prototype since it is the most complicated PEB type, which supports up to 55 front-end modules with 12 lpGBT, 9 VTRx+ and 52 bPOL12v in a very limited space. The requirements and overall specifications of the electronics of HGTD will be presented as well as the technical design and the project status.

## Programmable Logic, Design and Verification Tools and Methods / 35

### Front-End RDMA Over Converged Ethernet, real-time firmware simulation

**Author:** Gabriele Bortolato<sup>1</sup>

**Co-authors:** Andrea Triossi<sup>1</sup>; Matteo Migliorini<sup>1</sup>; Antonio Bergnoli<sup>1</sup>; Marco Angelo Bellato<sup>1</sup>; Daniele Mengoni<sup>1</sup>; Damiano Bortolato<sup>2</sup>; Fabio Montecassiano<sup>1</sup>; Sandro Ventura<sup>1</sup>; Jacopo Pazzini<sup>3</sup>; Marco Zanetti<sup>1</sup>

<sup>1</sup> *Universita e INFN, Padova (IT)*

<sup>2</sup> *INFN - National Institute for Nuclear Physics*

<sup>3</sup> *Università e INFN, Padova (IT)*

**Corresponding Author:** gabriele.bortolato@cern.ch

Several physics experiments are moving towards new acquisition models. In this work implementation of Remote Direct Memory Access (RDMA) directly on the front-end electronics has been explored, in this way is possible to free part of the computing farm's CPU resources. The work also introduces new verification techniques for verifying RDMA over Converged Ethernet (RoCE) firmware block developed at ETH, including real-time firmware simulation using Verilog Simulator. The result is a stripped down firmware version, allowing its implementation on smaller FPGAs, such as rad-hard parts.

**Summary (500 words):**

Several physics experiments are moving (or are evaluating the possibility to move) towards new acquisition models. The tendency is to leave the hardware trigger system in favour of a complete or partial acquisition of the front-end data paired with a powerful online software event discrimination. Hardware trigger systems usually have to deal with a tight latency budget due to the narrow readout buffering. To reduce the selection inefficiencies resulting from the adoption of not optimal trigger algorithms due to the limited time budget and online computing resources, the main trigger schema is going to be revisited. The traditional first trigger level is going to be replaced by a hardware pre-processing of the data stream followed by a software online selection.

In a DAQ system a large fraction of CPU resources is engaged in networking rather than in data processing. The common network stacks that take care of network traffic usually manipulate data through several copies performing expensive operations. Thus, when the CPU is asked to handle networking, the main drawbacks are throughput reduction and latency increase due to the overhead added to the data transmission process. Networking with zero-copy can be achieved by adding a RDMA layer to the network stack and making dedicated hardware take care of the burden of the stack handling.

The main goal of the RDMA implementation in the detector front-end electronics is to move up the adoption of clever networking protocols to the data producer. Therefore, the front-end electronics can initiate the RDMA transfer to the computing farm, eliminating the point-to-point connection between the front-end and back-end allowing the freedom of dynamically switching the routing to the computing nodes according to their processing availability. By appropriately choosing the network protocol for RDMA it is also possible to obtain a two-fold benefit. The possibility of adopting commodity hardware makes the DAQ system reduce reliance on custom hardware and it exploits all the advantages of a mature technology. In this way, the DAQ system gains in scalability and easiness of maintainability. RoCE is the industry-standard Ethernet-based RDMA solution with a multi-vendor ecosystem, making it the natural choice. In this work the implementation and verification of the main firmware blocks for the realisation of the RoCE endpoint have been explored. A real-time firmware simulation of the RoCE network stack has been developed where real network packets are exchanged between free-running Systemverilog code and the host machine via a TUN/TAP device which emulates a connection with a physical device (FPGA). The second part is devoted to show the verification process of the modified RoCE stack using the tools developed so far such as the novel simulation framework. The lightweight RoCE will be a stripped down version of the already verified firmware allowing the deployment on FPGAs with a low resource pool possible target devices could be rad-hard FPGAs used in front-end detector boards.

**Thursday posters session / 36**

## **An FPGA-based Front-end Module Emulator for the High Granularity Timing Detector Readout Module**

**Authors:** Lucia Castillo Garcia<sup>1</sup>; Zhenwu Ge<sup>2</sup>

<sup>1</sup> IFAE - Barcelona (ES)

<sup>2</sup> Nanjing University (CN)

**Corresponding Author:** zhenwu.ge@cern.ch

The HGTD aims to mitigate the effect of large pile-up interactions in the ATLAS Phase II upgrade project by providing accurate time measurements for tracks. However, since HGTD readout modules are unavailable during early stage, an FPGA-based front-end module emulator is designed as a substitute for system testing. This emulator also provides a flexible and cost-effective means to

verify the digital logic of the ASIC chip used in the HGTD readout module. This presentation offers a solution for replacing ASIC chips with FPGAs during system test, and also provides a method for verifying the design of an ASIC chip.

**Summary (500 words):**

The large increase of pileup is one of the main experimental challenges for the High Luminosity LHC project (HL-LHC) physics program. A High-Granularity Timing Detector (HGTD) is proposed for the ATLAS Phase-II upgrade to measure the time of the tracks accurately in order to mitigate the effect of the pile-up in the object reconstruction. The time information of tracks is measured, encoded and formatted in the HGTD readout module based on the ALTIROC chip. The data are transmitted through a flexible PCB and the peripheral electronic board (PEB), and eventually are collected by the data acquisition system (DAQ). At the same time, the HGTD readout module is also responsible for handling the slow control information from detector control system (DCS) as well as the fast command from time trigger control system (TTC).

HGTD readout module is essential when testing the individual components as well as the full chain of the HGTD readout system. However, because of the lengthy ASIC chip design and manufacturing process, HGTD readout modules are unavailable in the early stage of the project. We design a front-end module emulator based on Xilinx-Spartan 7 FPGA (XC7S15-2CPGA196C) to mitigate the influence to HGTD tests. It realizes four primary functionalities of HGTD readout module.

Firstly, it generates pseudo time data of tracks, and then packages and encodes the data in the same manner as the HGTD readout module. The emulator plays a crucial role in bit error rate test for the HGTD DAQ path as data source. The test results in turn instruct us to determine the optimal parameters for pre-emphasis. Meanwhile, the emulator's output has the same encoding mode and data frame as HGTD readout module. As a result, it can be used to verify the decoding and storage functions of the DAQ.

Secondly, the emulator's fast command control unit receives and decodes fast commands from TTC, which helps verify different fast commands and their stability of transmission.

Thirdly, the slow control unit of the emulator ensures that we can configure the emulator to different working modes online.

Lastly, the emulator can generate analog signals which are feed to a dedicated mux chip on PEB, and then to the ADC of lpGBT chip located on PEB. These signals can be used to verify the mux chip and calibrate the ADC.

Besides the logic functions, the emulator shares same overall dimensions and connectors with HGTD readout module. These features allow that the emulator can substitute for HGTD readout module in system test while the HGTD readout module is unavailable.

In addition, the emulator also provides a cost-effective and flexible means to verify the design of the ASIC chip used in HGTD readout module. We transplanted the slow control simulation code of the ASIC chip to emulator and verified it works well.

The emulator has played a crucial role in HGTD project. It also offers a solution for replacing ASIC chips with FPGAs during system test, and also provides a method for verifying the design of an ASIC chip.

**Programmable Logic, Design and Verification Tools and Methods / 37**

## **Verification Environment for ALTIROC ASIC of the ATLAS High Granularity Timing Detector**

**Authors:** Lucia Castillo Garcia<sup>1</sup>; Simone Scarfi<sup>2</sup>

<sup>1</sup> IFAE - Barcelona (ES)

<sup>2</sup> CERN

**Corresponding Author:** simone.scarfi@cern.ch

ALTIROC3 is the second version of the ASIC for the ATLAS High Granularity Timing Detector to read out full size LGAD sensors (15x15 pixels of 1.3mm x 1.3mm). The ASIC, designed in 130nm technology, comprises around 250k flip-flops, more than 1000 8-bit configuration registers, and several clock domains and implements different analog IP-blocks critical for digital data acquisition and processing. This contribution presents the verification approach and tools employed, including a new

System Verilog verification environment based on Universal Verification methodology (UVM) for functional, power and SEE verification, complemented with formal verification for Clock Domain Crossing (CDC) and Reset analysis.

**Summary (500 words):**

ALTIROC ASIC of the ATLAS High Granularity Timing Detector (HGTC) is required for the High Luminosity LHC where there will be a large increase in pile-up. The ASIC will provide luminosity measurement at each Bunch Crossing (BC) and precision timing information with 20 ps resolution for Time-Of-Arrival (TOA) and 40 ps resolution for Time-Over-Threshold (TOT) only upon reception of a trigger.

ALTIROC3 ASIC followed a Digital-on-Top approach in order to enable digital tools capabilities in constraining, designing and better verifying the ASIC reducing the Turn-Around-Time (TAT) of the design flow.

Taking advantage of the automatization and reproducibility of the design and verification flows, a new System Verilog verification environment based on Universal verification Methodology (UVM) has been developed to cover all intended functionalities of the design at full chip level to give the designers enough confidence before submission.

The objective of the new verification environment has been to verify the full chip using digital tools. For the first time, analog IP blocks have been characterized with cycle accurate Verilog models that represent a breakthrough for a more comprehensive mixed-signal full chip functional verification.

For instance, the modeling of the analog front-end together with the two TDCs allowed stimulating the hit sampling digital logic in unexpected ways. The verification framework provided assistance to verify the chosen architecture.

The functional verification of critical interfaces between analog world and digital world consisted in verifying not only the behavior of the analog IP block, but also the how they have been integrated in the Digital-on-Top implementation.

The new UVM verification environment comprises reusable UVM Verification Components (UVC), register abstraction layer (RAL) block for the configuration and design specific verification components to assist the design phase and to stimulate the design efficiently exploiting constrained randomization and functional coverage collection.

The high number of clock domains present in the ASIC, together with the complex clock and reset architecture, required to complement the classical functional verification approach with formal methods, whose performances are necessary to exhaustively prove the correctness of the design.

Moreover, the verification environment developed for ALTIROC3 has also been helpful to assist power verification, namely IR drop and dynamic power consumption, and extensively used to verify SEE at RTL level and on the final netlist.

**Thursday posters session / 38**

## **Commissioning of the Test System for the Phase-2 Upgrade of the CMS Outer Tracker**

**Author:** Patryk Szydlik<sup>1</sup>

**Co-authors:** Angelos Zografos<sup>2</sup>; Bruno Allongue<sup>2</sup>; Georges Blanchot<sup>2</sup>; Irene Mateos Dominguez<sup>2</sup>; Kevin Schleidweiler<sup>3</sup>; Mark Istvan Kovacs<sup>2</sup>; Riccardo Carnesecchi<sup>2</sup>

<sup>1</sup> *Wroclaw University of Science and Technology (PL)*

<sup>2</sup> *CERN*

<sup>3</sup> *Ministere des affaires etrangeres et europeennes (FR)*

**Corresponding Author:** patryk.szydlik@cern.ch

The Phase-2 Upgrade of the CMS Outer Tracker requires the production of 8000 Strip-Strip and 5880 Pixel-Strip modules, altogether incorporating 47520 hybrid circuits of 15 variants. Module design makes the potential repairs unfeasible; therefore, performing production-scale testing of the hybrids is essential. Accordingly, a scalable, crate-based test system was designed and manufactured, allowing for parallel, high-throughput testing. To reproduce the operating conditions, the system was integrated within a climatic chamber, including the development of a remote control interface

and the calibration of thermal cycles. The results and lessons learned from the system integration and commissioning will be presented.

**Summary (500 words):**

The Compact Muon Solenoid (CMS) Outer Tracker Phase-2 Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) is composed of two main types of modules: the strip-strip (2S) and the pixel-strip (PS). The 2S modules contain two parallel strip sensors of (10×10) cm<sup>2</sup>, two front-end hybrids and a service hybrid. The PS modules consist of a strip sensor and a macro-pixelated strip sensor of (5×10) cm<sup>2</sup>, two front-end hybrids, power hybrid, and a data readout hybrid. Ten different front-end hybrid variants and five additional service, power, and readout hybrid variants have been designed. Currently 9 of those variants are in kick-off production at the manufacturer's premises, which will be followed up with pre-series and full production.

The modules constructed for the upgrade are permanently joining the components with gluing. Failure in any of the components would result in a discarded high value module. In order to reduce the losses at this level, it is fundamental to test the hybrids extensively. Given the large quantity of hybrids scheduled to be manufactured, a high-throughput testing system was required. Therefore, the test infrastructure was designed based on a 3U 19-inch sub-rack with custom-developed multiplexer backplanes, enabling the multiplexed testing of twelve hybrid circuits in one crate. The backplanes connect to FC7 data acquisition boards, which controls the selection of plug-in cards and processes the data.

Overall, six types of test cards were designed and produced. With the usage of interchangeable sockets and interconnection circuits, each card can accommodate all the hybrid variants from the same family. The total system quantity, accounting for spares, consists of 645 test cards. During the commissioning process, each card had to be inspected, assembled with mechanical sockets, and then fused with a serial number. After that, each card was fully tested and approved using reference hybrids. During the process, multiple problems arose and were solved before the final integration within the test system.

In order to integrate the test system within the climatic chamber, a custom-made frame was procured and mounted inside the chamber. To remove the necessity for supervision of a trained operator over the functioning chamber, a remote control interface was developed, allowing for partial control, monitoring, and error handling from within the test procedure.

Additionally, to protect the electronics from humidity condensation, external humidity and temperature probes were added. The supplementary sensors were used to obtain dewpoint characteristics of the test system during thermal cycling, which subsequently allowed for the calibration of temperature ramps and the utilization of additional protections.

In this contribution, the quantitative results of test system commissioning will be analyzed, including overall yield, test results, and common problems. Additionally, the process of safe-proofing and calibrating the climatic chamber will be presented, along with the capabilities of developed remote control interface. The conclusions presented could be exceptionally useful for future production-scale, reliability or lifetime-testing campaigns incorporating thermal cycling.

**Tuesday posters session / 41**

## **Test Result of the New ASD2 Chips for Phase-II Upgrade of the ATLAS MDT Chambers at HL-LHC**

**Author:** Paolo Iengo<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Authors:** k.penski@physik.uni-muenchen.de, paolo.iengo@cern.ch

For the  
-II upgrade of the ATLAS Muon Spectrometer to the High Luminosity LHC  
(HL-LHC), a new first-level muon track trigger is needed to make use of the high momentum



resolution of the Monitored Drift Tube (MDT). The current front-end electronics of the MDT chambers do not meet these conditions, they have to be replaced. Therefore, a new ASD2 ASIC chip has been developed. Finally, 50000 ASD2 chips are needed for the ATLAS experiment. The development of the final testing procedure and the reliability of a first batch ASD2 chips will be presented.

**Summary (500 words):**

A new first-level muon track trigger is installed for the

-II upgrade of the ATLAS Muon

Spectrometer to the High Luminosity LHC (HL-LHC), which will make use of the high momentum resolution of the Monitored Drift Tube (MDT) chambers. Due to the long drift times in the MDT, a triggerless readout is needed. Since the current front-end electronics of the MDT chambers do not meet these conditions, they have to be replaced. For this purpose, a new ASD2 ASIC chip in 130 nm Global Foundries CMOS technology has been developed. For the ATLAS experiment, 80000 chips are produced and tested before integration, since in the end 50000 well-performing chips are needed. The overall goal of the ASD2 chip test procedure presented is to find optimized parameters and cut values that characterize the performance of the chip and are used for production testing in the company.

Phase

First, the influence of the different programmable parameters on the chip's behaviour is investigated. For this purpose, 100 pre-production chips are tested with tester board prototype and analysed with respect to four measurement criteria: Basic Health, Threshold, Dead Time and Pulse Width. Cuts are introduced to reject non-functioning chips and achieve high uniformity among the channels and chips. In a second step, about 100 pre-production and production chips are compared. Both ASD2 chip types show no practical difference. In both cases, about 80 % of the chips work considering the introduced selection criteria and cut intervals.

For the production testing a new QAQC tester board was designed, and its performance is examined using the 100 production chips. The results are compared with those of the tester prototype. Despite of an offset in some values due to a larger bias current in the new tester, there is no difference of practical relevance.

Finally, in order to define final testing parameters and cut intervals for the production testing at the company

,  
1175 production ASD2 chips are tested with the new tester. The yield of well-performing chips is about 86%, with a homogeneous distribution for all channels and chips regarding all four measurement criteria. For finer differentiation, the cut criteria are further extended, and the chips are divided into three categories, with 14 % of the chips in C (non-working chips), 16 % in B (working chips outside some cut intervals) and 70 % in A (working chips inside all intervals). These results are used as input for the automatized production chip testing which took place in spring 2023 using 80000 chips.

ASIC / 42

## 3D-integrated pixel circuit for a low power and small pitch SOI sensor

**Author:** Yunpeng Lu<sup>1</sup>

**Co-authors:** Yang Zhou<sup>1</sup>; Jia Zhou<sup>1</sup>; Hongyu Zhang<sup>1</sup>; Jing Dong<sup>1</sup>; Mingyi Dong<sup>1</sup>; Qun Ouyang<sup>1</sup>

<sup>1</sup> *Institute of High Energy Physics, Chinese Academy of Sciences*

**Corresponding Author:** yunpeng.lu@cern.ch

Targeting on low power consumption and high spatial resolution, the CPV-4 SOI pixel sensor requires about 100 transistors to implement the analog-digital mixed circuit functionality within a given pixel area around 16  $\mu\text{m} \times 20 \mu\text{m}$ . By utilizing 3D vertical integration, signal amplification and threshold discrimination are achieved in the lower-level circuitry, while hit information storage and sparse readout are achieved in the upper-level circuitry, thereby maximizing pixel size reduction and

power consumption reduction. This work will present the pixel circuit design and the test results on the completed 3D chips.

**Summary (500 words):**

This work starts from the design challenges of the vertex detector for the future Circular Electron Positron Collider (CEPC) and introduces the main design constraints on the pixel sensor design. In the development of the Compact Pixel for Vertex (CPV) series of pixel sensors, a high spatial resolution implementation method is proposed, especially the overall solution of the CPV-4 chip using 3D-SOI design. Based on the conventional 200nm SOI pixel process, 3D-SOI technology adds a vertically stacked upper circuit layer and a high-density micro-bump array connection. This provides the technical conditions for reducing the pixel pitch while maintaining the pixel circuit function. The CPV-4 design uses a low-power analog front-end circuit placed in the lower tier, while hit information storage and sparse readout are placed in the upper tier, successfully reducing the pixel size to  $17\mu\text{m} \times 21\mu\text{m}$ . Currently, the lower tier and upper tier of the chip have been functionally verified and the first vertical integration trial has been carried out. The control of the lower tier and upper tier has been achieved on the completed 3D chip, and the successful 3D connection of the IO Pads has been verified. However, this was obtained on different 3D chips, and no single 3D chip has been able to control both the lower tier and upper tier simultaneously. Improving the yield of 3D integration seems to be very challenging.

This work provides an alternate technical route for achieving pixel sensors with extremely high spatial resolution. Compared with another technical route of shrinking the pixel pitch by reducing the size of transistors using the new generation of smaller CMOS process, this method has the advantages of depleted layer thickness and high signal-to-noise ratio, and is expected to meet the comprehensive requirements of the CEPC vertex detector for spatial resolution of  $3\mu\text{m}$ , average power consumption of 50mW/square (cm), and time resolution of a few  $\mu\text{s}$ .

**Tuesday posters session / 43**

## **An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs**

**Authors:** Dmitry Eliseev<sup>1</sup>; Dmitry Eliseev<sup>1</sup>

**Co-authors:** Carsten Presser<sup>2</sup>; Erik Ehlert<sup>3</sup>; Markus Karl Merschmeyer<sup>4</sup>; Thomas Hebbeker<sup>1</sup>

<sup>1</sup> Rheinisch Westfaelische Tech. Hoch. (DE)

<sup>2</sup> RWTH Aachen

<sup>3</sup> RWTH Aachen University

<sup>4</sup> RWTH Aachen University (DE)

**Corresponding Authors:** dmitry.eliseev@cern.ch, eliseev@physik.rwth-aachen.de

High-speed multichannel ADCs are costly and require complex FPGA firmware to communicate with them. The Multi-Voltage Thresholding (MVT) approach can replace to some extent an external ADC with internal resources of an FPGA, thus reducing costs and complexity. The MVT approach needs only a few low-cost external components. The focus of the talk is presenting an open-source IP-Core that implements the MVT approach and simplifies implementation on a standard FPGA. The talk also provides an overview of characterization measurements and specific calibration methods. Our example application demonstrates the viability of the developed IP-Core for signal acquisition from multiple SiPMs.

**Summary (500 words):**

The Multi-Voltage Thresholding (MVT) approach offers an alternative to high-speed multichannel ADCs for signal acquisition. While the approach has similarities to comparator-based Flash-ADCs, it utilizes

FPGA internal resources to replace external ADCs. This reduces costs, complexity, and energy consumption for applications that strongly require fast multichannel digitization, but are satisfied with a low ADC resolution.

One may note that most inputs in modern FPGAs are capable of operating in Low-Voltage Differential Signaling (LVDS) mode, which enables the implementation of MVT with LVDS differential receivers. LVDS receivers of an FPGA are not ideal and can have a positive or negative bias of up to  $\pm 40\text{mV}$ , which must be determined and compensated for every LVDS receiver through a calibration procedure. The calibration procedure involves applying a known voltage as a threshold and a test pulse of triangle form with exactly known parameters to the LVDS receiver. The bias of an LVDS receiver results in a switching delay (positive or negative) in respect to the predicted moment when the LVDS receiver should have switched. From the measured delay we calculate the needed bias compensation for the particular LVDS receiver.

Our focus in this talk is on the introduction of an open-source IP-Core, which we have named MVT-Quad IP-Core. This IP-Core is designed to sample analog signal from a single input and is equipped with four LVDS receivers. It enables users to easily and efficiently integrate the MVT approach into their FPGA designs. The IP-Core integrates a streaming output for the acquired data and a memory mapped interface for registers, which are relevant for calibration and configuration. To implement the MVT-based signal acquisition for multiple input channels in a particular FPGA design, one needs to instantiate the respective number of MVT-Quad IP-Cores and provide some minimal additional external schematics for the voltage thresholding. A reference design for this external schematics is also present in the scope of this talk. The successful functioning of our IP-Core is demonstrated in a test application where signals from multiple SiPM sensors are acquired, allowing for the acquisition of cosmic muons with scintillating stripes. Overall the MVT approach, together with the proposed MVT-Quad IP-Core, has the potential as a viable solution for fast multichannel signal acquisition in various applications.

**Thursday posters session / 44**

## **Design and implementation of Neural Network based conditions for the CMS Level-1 Global Trigger upgrade for the HL-LHC**

**Author:** Gabriele Bortolato<sup>1</sup>

**Co-authors:** Artur Lobanov<sup>2</sup>; Benjamin Huber<sup>3</sup>; Dinyar Rabady<sup>4</sup>; Elias Leutgeb<sup>3</sup>; Hannes Sakulin<sup>4</sup>; Jaana Heikkilae<sup>5</sup>; Maria Cepeda<sup>6</sup>

<sup>1</sup> *Universita e INFN, Padova (IT)*

<sup>2</sup> *Hamburg University (DE)*

<sup>3</sup> *Technische Universitaet Wien (AT)*

<sup>4</sup> *CERN*

<sup>5</sup> *University of Zurich (CH)*

<sup>6</sup> *CIEMAT*

**Corresponding Author:** gabriele.bortolato@cern.ch

The High-Luminosity LHC upgrade will have a new trigger system that utilizes detailed information from sub-detectors at the bunch crossing rate, which enables the Global Trigger (GT) to use high-precision trigger objects. Novel machine learning-based algorithms will also be included in the trigger system to achieve higher selection efficiency and detect unexpected signals. The focus of this study is on optimizing the implementation of these novel algorithms, in particular software-based to more hardware-based optimizations are studied in detail. Finally, the study will analyse how the applied optimizations affect performance degradation and the model's resource footprint.

**Summary (500 words):**

The new trigger system for the High-Luminosity LHC upgrade will exploit detailed information from the calorimeter, muon and tracker trigger paths at the bunch crossing rate. The final stage in the trigger,

the Global Trigger (GT), will receive high-precision trigger objects from the upstream trigger channels. It will evaluate a menu of more than 1000 cut-based and neural-net based trigger algorithms in order to determine the Level-1 trigger accept decision. Traditionally, algorithms used to build the so called trigger menu have employed simple selections on one or more physics objects for instance cutting on a specific or combination of reconstructed particle properties. The Phase-2 CMS GT aims to go beyond this approach and include neural network-based conditions alongside the usual algorithms already in use today in Run-3 in order to reach higher selection efficiency and selection of unexpected signals. Implementing these neural network-based conditions in the GT algorithm chain requires meeting stringent requirements, particularly in terms of latency and resources. The upgrade targets a total latency of 1 $\mu$ s (40 Bunch Crossings) for the entire GT, this implies that model optimizations are essential to meet the target latency. Neural networks are typically resource-intensive, so extensive optimization is required during and after training to integrate them alongside the large number of cut-based algorithms. Two different flavours of neural networks are considered: deep binary classifiers and deep auto-encoders. A deep binary classifier is designed to distinguish a specific signal signature from unwanted background noise through supervised training. In contrast, a deep auto-encoder aims to characterize as much as possible the background and identify anything that does not resemble it marking it as anomalous. For this reason, it is also known as an anomaly detection trigger and uses unsupervised training. The Hls4ml tool has been employed to convert a Tensorflow/Keras models into hardware description language like VHDL and Verilog. To reduce the model resource footprint and latency, multiple optimizations have been applied to the code. Some of these optimizations, such as variable and synapse pruning, hyperparameter quantization and precision tuning, can be performed without completely redesigning the model. However, others require a new model to be designed and trained from scratch, for instance in this work a technique known as knowledge distillation was used. A prototype firmware has been implemented and evaluated. It contains various models that differ in the optimization techniques applied and target signal signature. The firmware encompasses neural networks, the entire GT infrastructure (including the I/O logic, de-multiplexers, and object distribution) and the interfaces necessary for the communication between the neural network and the GT framework. GT objects are streamed at a frequency of 480 MHz, whereas the neural network accepts a single vector of objects every 25 ns (40MHz). After multiple tests the model has been tuned to run at 240 MHz with an initiation interval (II) of 1. Firmware resource usage and performance are studied to extract the best compromise between latency and logic footprint.

Tuesday posters session / 45

## Adaptability and efficiency of the CMS Level-1 Global Trigger firmware implementation for Phase-2

**Author:** Benjamin Huber<sup>1</sup>

**Co-authors:** Dinyar Rabady<sup>2</sup>; Elias Leutgeb<sup>1</sup>; Gabriele Bortolato<sup>3</sup>; Hannes Sakulin<sup>2</sup>; Jaana Heikkilae<sup>4</sup>; Maria Cepeda<sup>5</sup>

<sup>1</sup> *Technische Universitaet Wien (AT)*

<sup>2</sup> *CERN*

<sup>3</sup> *Universita e INFN, Padova (IT)*

<sup>4</sup> *University of Zurich (CH)*

<sup>5</sup> *CIEMAT*

**Corresponding Author:** benjamin.huber@cern.ch

We present details on the new Level-1 Global Trigger at CMS for the upcoming high-luminosity operation of the LHC. Our focus is on the newly developed firmware, which employs a bottom-up generic approach to enhance menu adaptability and accommodate the increase in upstream information. We also highlight our efficient pipelining strategy that ensures excellent routability at 480 MHz. Furthermore, we discuss the three Serenity boards for which a prototype exists, together with their current and future testing and validation endeavours.

**Summary (500 words):**

In preparation for the Phase-2 operation at the high-luminosity LHC, scheduled to commence in 2029, the CMS detector is undergoing significant upgrades to its detectors and readout electronics. The increased luminosity also poses additional challenges for the CMS trigger system. To ensure that the physics performance is maintained or improved under the new pile-up conditions, a completely new Level-1 trigger system is being designed as part of the upgrade. The new system will process information from the calorimeter, the muon systems as well as reconstructed tracks from the silicon tracker. An increased latency budget of 12.5  $\mu\text{s}$ , compared to 3.5  $\mu\text{s}$  in the current trigger, will also allow for sophisticated algorithms such as vertex finding, particle flow reconstruction and the extensive use of neural networks, which were previously only possible at later software-driven stages of the trigger system. From the side of the final stage of the Level-1 trigger pipeline, the Global Trigger is being entirely redesigned, including a modern continuous-integration-driven development and testing infrastructure and a completely rewritten firmware to cope with the increase of available data from the upstream trigger systems. Here, we employed the approach of writing every module as generic as possible, which not only guarantees that they are usable with a wide variety of upstream information but also that the menu is highly adaptable to the changing run conditions at CMS. Conversions to a common scale ensure that comparisons can be performed irrespective of the subsystem that provided the trigger object.

In terms of implementation, the Phase-2 firmware is designed to operate at 480 MHz, a frequency that is twelve times the LHC clock, allowing for the efficient reuse of comparator and calculation logic. This is accomplished by pipelining objects and later combining the aggregated comparator results in a final step before arriving at a decision for a specific physics signature check. This approach is applicable not only for simple checks on individual quantities such as  $p_T$ ,  $\eta$ ,  $\phi$ ,  $z_0$ , etc., but also for correlational quantities that involve calculations, such as invariant mass,  $\Delta R$ , transverse mass, combined  $p_T$ , charge, and others. Albeit for correlational checks, only one of the two involved object collections can be pipelined, while the other has to be available in parallel to form all possible correlation pairs within an event. The efficient pipelining technique we have implemented is a crucial aspect of maintaining routability of the design at such a high clock frequency.

The CMS collaboration has developed new generic ATCA processing boards capable of handling the data rates during high-luminosity operation. These feature either a Xilinx Virtex Ultrascale+ VU13P, VU9P or a Xilinx Kintex Ultrascale+ KU15P FPGA. Prototypes of our firmware currently exist for all three of them. While the algorithm implementation remains consistent across all prototypes, variations are observed in the interface design, the number of algorithms, and the distribution of input information across Super-Logic-Regions. The VU13P FPGA has been designated as the target for the final implementation, while the other boards are retained for testing and prototyping.

**Thursday posters session / 46**

## **A Custom Discrete Amplifier-Shaper-Discriminator Circuit for the Drift Chambers of the R3B Experiment at GSI**

**Author:** Michael Wiebusch<sup>1</sup>

**Co-authors:** Henning Heggen<sup>1</sup>; Michael Heil<sup>1</sup>

<sup>1</sup> *GSI Helmholtzzentrum für Schwerionenforschung GmbH*

**Corresponding Author:** m.wiebusch@gsi.de

This contribution presents a pragmatic approach to read-out electronics for drift chambers used in particle physics experiments, specifically for the R3B experiment at GSI. The proposed circuit design uses discrete miniature SMD components and LVDS inputs of a low-cost FPGA to achieve a performance similar to the classic ASD8 ASIC. The presented approach offers an attractive solution for small to medium sized detector systems that require specialized read-out electronics but cannot afford the high cost and development effort associated with ASICs.

**Summary (500 words):**

This contribution presents a pragmatic approach to read-out electronics for drift chambers used in particle physics experiments, specifically the R3B experiment at GSI.

The drift chambers used in this experiment and their 512 individual drift cells play a crucial role in particle tracking, momentum measurements as well as particle identification and require a specialized front-end electronics system to achieve the desired sensitivity and accuracy in terms of leading edge time (drift time) and pulse charge (particle energy loss). The aim was to develop discrete front-end electronics with similar performance as the classic ASD8 ASIC, which is no longer available due to its outdated manufacturing process.

The proposed circuit design consists of a discrete amplifier-shaper-discriminator circuit implemented in miniature SMD technology. Sixteen amplifier channels are integrated onto a single credit card-sized board which connects directly to the chamber. Each amplifier channel comprises three individual transistors in a TSLP-3 package (size of a 0402 resistor) and a number of 0201 passive components. The charge sensitive amplifier features a three-stage unipolar pulse shaper with a (measured) peaking time of  $14\text{ ns}$  and two pole-zero filters for ion tail suppression. The input impedance of the amplifier is  $330\ \Omega$ , which matches the impedance of the drift chamber cell. The overall gain of the circuit is  $3.5\text{ mV/fC}$ .

Pulse discrimination for all 16 channels is carried out with the help of the numerous low-voltage differential signaling (LVDS) inputs of a low-cost FPGA.

The total power consumption of the ASD circuit is only  $36\text{ mW}$  per channel, while the transistor circuit alone accounts for  $16\text{ mW}$  per channel.

The front-end board feeds LVDS signals to an FPGA-based TDC data acquisition board which was also developed by our group. The employed TDC has a bin width of  $416\text{ ps}$ , which yields a time measurement precision of  $170\text{ ps}$ , and is thus sufficient for drift chambers.

A first test measurement was performed using a  $^{55}\text{Fe}$  source with the chamber. The time-over-threshold spectrum shows clear peaks indicating the successful detection of the photo peak and the Argon escape peak at  $6\text{ keV}$  and  $2.7\text{ keV}$ , respectively. The evaluation of the circuit's performance is ongoing, and further results will be presented at the time of the conference.

The presented approach demonstrates that modern SMD component dimensions and minimalist analog circuit design can be utilized to develop analog read-out solutions that can compete with ASIC solutions, at least in moderately high density detector set-ups. The proposed circuit design offers an attractive solution for experiments that require specialized read-out electronics but cannot afford the high cost and development effort associated with ASICs.

## Production, Testing and Reliability / 47

### CMS ECAL VFE design, production and testing

**Author:** Werner Luster<sup>1</sup>

**Co-authors:** Alexander Singovski<sup>2</sup>; Alexandre Dolgoplov<sup>2</sup>; Daniel Abadijev<sup>3</sup>; Guenther Dissertori<sup>1</sup>; Krzysztof Stachon<sup>1</sup>; Luke Thomas Martin<sup>3</sup>; Marc Dejardin<sup>4</sup>; Tomasz Gadek<sup>1</sup>

<sup>1</sup> *ETH Zurich (CH)*

<sup>2</sup> *University of Notre Dame (US)*

<sup>3</sup> *Northeastern University (US)*

<sup>4</sup> *Université Paris-Saclay (FR)*

**Corresponding Author:** werner.lustermann@cern.ch

Maintaining the required performance of the CMS electromagnetic calorimeter (ECAL) barrel at the High-Luminosity Large Hadron Collider (HL-LHC) requires the replacement of the entire on-detector electronics. 12240 new very front end (VFE) cards will amplify and digitize the signals of 62100 lead-tungstate crystals instrumented with avalanche photodiodes. The VFE cards host five channels of CATIA pre-amplifier ASICs followed by LiTE-DTU ASICs, which digitize signals with

160MS/s and 12bit resolution. We present the strategy and infrastructure developed for the testing, burn-in, calibration and assembly of the VFE cards. Moreover, we summarize the test results obtained with 60 prototype cards.

#### Summary (500 words):

The electromagnetic calorimeter (ECAL) [1] barrel of the Compact Muon Solenoid (CMS) experiment [2] is made of 61200 lead-tungstate crystals read out by avalanche photodiodes (APDs). Its readout electronics are arranged into towers of 5x5 channels, comprising five very front end (VFE) cards (Fig. 1), one digital interface card (FE) and one low voltage regulator card (LVR) conditioning the power of one tower. Each VFE card hosts five channels of a pre-amplifier (CATIA) followed by an analog-to-digital converter (LiTe-DTU). The tower electronics will be replaced for operation at HL-LHC in order to maintain ECAL's performance under increased luminosity conditions. This involves the production and testing of ~14000 new VFE cards.

ECAL is a single layer detector. Missing readout channels degrade the energy resolution and missing towers may allow photons or electrons to remain unidentified. Extracting an ECAL module for repair requires several months and is not foreseen for the operation period of ~20 years. Another important aspect is the monitoring of the production yield, avoiding complete failures of production batches.

Therefore, quality control is of highest importance. We are aiming at <0.5% of all channels failing at end-of-life. We will achieve this applying a bundle of measures:

- We require class 3 for the VFE PCBs.
- ESD protection will be systematically implemented at all steps.
- We produce ~500 VFEs per week, fast enough to complete the production in ~6 months and slow enough to follow the production with testing and burn-in.
- VFE cards are tested first by the manufacturer, using automatic optical inspection and a ~1min electrical test. The same electrical test is repeated at the reception of the cards followed by accelerated aging with thermal cycling. Finally, the cards are electrically tested again and if fully operational, calibrated.
- Failing cards and outliers are excluded from further use. Healthy cards are assembled with their mechanical housing and the thermal interface materials.

An electrical test setup has been developed, comprising:

- An FPGA based interface card connecting the VFE via ethernet to a PC
- A signal and power interface card.
- A computer-controlled power supply.
- A precision test pulse generator (optionally).

We scan the pedestal setting of the CATIA, the PLL locking range of the LiTE-DTU and perform gain and linearity measurements with internal and external test-pulses (see figure 2). We develop test software with a graphical user interface (see figure 3).

The VFE card burn-in is done simultaneously with the LVR card burn-in. In this way we have correctly conditioned power for the VFE cards and at the same time the LVR cards have the correct load. We are self-developing appropriate cabinets. Heating is provided by the dissipated power of the electronics under test and cooling is achieved by ventilation with ambient air. Three cabinets hosting up to 200 VFE cards each, will enable to follow the production pace. The detailed aging procedure will be defined in a dedicated test of pre-production cards.

#### Tuesday posters session / 48

## HGTD PEB DC/DC Power Block in Low Temperature and Magnetic Field Operation

**Authors:** Lucia Castillo Garcia<sup>1</sup>; Mingjie Zhai<sup>2</sup>

<sup>1</sup> IFAE - Barcelona (ES)

<sup>2</sup> Chinese Academy of Sciences (CN)

**Corresponding Author:** mingjie.zhai@cern.ch

The High Granularity Timing Detector (HGTD) is an ATLAS Phase II upgrade project, the goal of which is to provide accurate time measurements for tracks to mitigate pile-up effect. DC/DC converters, BPOL12V, are implemented in the Peripheral Electronic Boards (PEB) and used to generate voltages for a bunch of ASICs. Due to the working environment constraints of HGTD, the BPOL12V

will be operated in low temperature and under magnetic field. Therefore, it is essential to perform a comprehensive study of BPOL12V under different operation conditions. This report will present such study, including the BPOL12V efficiency, ripple and other.

**Summary (500 words):**

The ATLAS Phase II upgrade will employ the High Granularity Timing Detector (HGTD), which provide a time measurement per end-cap track with a resolution of about 30ps in the High Luminosity LHC. The HGTD will be placed between the barrel and the end-cap calorimeters, at a radial distance of 110 to 1000 mm and a z-distance of about 3.5 m from the interaction point. The Peripheral Electronics Boards (PEB), at the outer radius of the HGTD, contains various functions such as control, monitoring, data transmission, power-supply distribution, and temperature sensor routing for interlock system. As a part of PEB, the DC/DC converters, BPOL12V, will be used to generate 1.2V and 2.5V for the ALTIROC ASIC and other components of PEB. The BPOL12V will work in low temperature (around -30C) and magnetic field (around 0.4T) conditions during operation, so a comprehensive study of its performance is essential.

We set up a test system to evaluate the performance of BPOL12V at low temperature. The system consists of a climate chamber to control the temperature, a source meter to supply and measure the input voltage and current, a load to provide and measure the output current and voltage, and an oscilloscope to examine the ripple and transient behavior. We tested two versions of PCB, (power block version 3) p3 and (power block version 4) p4, with output voltages of 1.2V and 2.5V. We measured the efficiency and output ripple as functions of input voltage, output current, and temperature. The results showed that p4 is more efficient than p3 at low output current. In general, p4 has lower output ripple than p3 for 2.5V output but higher output ripple than p3 for 1.2V output. We also investigated the ripple suppression and transient response by adding an input ripple and varying the input rise and fall rates. We observed that for all BPOL12V, input ripple below 100mV has negligible effect on the output ripple. The output rise edge does not depend on the input rise rate. The output fall edge depends on the input fall rate but is fast for all BPOL12V. More details of our study can be seen in the supporting material.

The magnetic field in the PEB region is mainly driven by the ATLAS solenoid, which changes over the radius and z axis, while negligible in phi. The magnetic field is also symmetric with respect to z axis. In PEB phase space, the magnitude of magnetic field is 0.382-0.433T and the angle between magnetic fields direction and the z axis is 23.1- 32.3°. To evaluate the BPOL12V performance under magnetic fields, we plan to place the BPOL12V inside a magnetic barrel that can produce adjustable (0 - 4T) magnetic fields using a superconducting solenoid. We also designed a support material to fix the BPOL12V at the center of the magnetic field and to control the angle between the BPOL12V and the magnetic field. The support material is being 3D printed and we expect to conduct this test in May.

ASIC / 49

## Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology

**Authors:** Adriano Lai<sup>1</sup>; Alberto Stabile<sup>2</sup>; Gian Matteo Cossu<sup>3</sup>; Lorenzo Piccolo<sup>None</sup>; Luca Frontini<sup>4</sup>; Sandro Cadeddu<sup>1</sup>; Valentino Liberali<sup>5</sup>

<sup>1</sup> *Università e INFN, Cagliari (IT)*

<sup>2</sup> *Università degli studi di Milano*

<sup>3</sup> *INFN, Cagliari (IT)*

<sup>4</sup> *INFN and Università degli Studi di Milano*

<sup>5</sup> *Università degli Studi di Milano*

**Corresponding Author:** sandro.cadeddu@ca.infn.it

The IGNITE project is developing solutions for the next generation of trackers at colliders. It plans to implement an integrated system module, comprising sensor, electronics, and fast readout, aimed at



4D-tracking. System pixels are required to have pitch around 50  $\mu\text{m}$  and time resolution below 30 ps. In the present paper we present recent advancements on the design of a prototype ASIC, exploring several circuitual solutions on the front-end side, in view of the first IGNITE ASIC, featuring a 64x64 pixel matrix, which is being completed in the coming months.

#### Summary (500 words):

The IGNITE project, funded by INFN, is developing solutions for the next generation of trackers at colliders, which may require high time resolution measurement at the pixel level, while keeping the pixel size and system power consumption substantially unaltered with respect to the present generation of inner tracking systems (e.g., CMS/ATLAS-phase2, LHCb Upgrade-1).

Following up and finalizing the developments of former INFN projects (TimeSPOT, Falaphel, Scaltech28), IGNITE plans to implement an integrated system module, comprising sensor, electronics, and fast read-out, specifically aimed at 4D-tracking. System pixels are required to have pitch around 50  $\mu\text{m}$  and time resolution below 30 ps. In the paper we present recent advancements on the design of a prototype ASIC (named Ignite\_0), designed in CMOS 28-nm technology, which wants to explore several circuitual solutions on the front-end side. The Ignite\_0 development is preparatory to the design of the first IGNITE full-ASIC, featuring a 64x64 pixel matrix, being completed in the subsequent months.

The Ignite\_0 ASIC is implemented as a mini-ASIC and contains new versions of the former TimeSPOT pixel, consisting of an Analog Front End (AFE) and a high-resolution Time-to-Digital-Converter.

The TimeSPOT-type AFE is a Charge Sensitive Amplifier with Krummenacher feedback and discrete-time Offset Compensation. Some imperfections, present in the TimeSPOT 32x32 matrix version, are here corrected and accurately simulated. New ideas on the AFE input stage and feedback circuit, aimed at obtaining a faster response to optimize the system performance in terms of time resolution, are here explored as well.

The TimeSPOT TDC, based on a Vernier-type architecture, have several improvements in terms of operational and SEU robustness. Furthermore, the front-end pixel size is also reduced from 55  $\mu\text{m}$  (TimeSPOT) to the level of 40  $\mu\text{m}$ , in order to make it possible the read-out of smaller pixel sensors.

The Ignite\_0 ASIC integrates additional important service circuits, and in particular DACs and PLLs, to test them on silicon before their integration on the 64x64 pixel matrix, which has already started.

The explored solutions will be critically illustrated during the talk, highlighting their pro and cons.

#### Tuesday posters session / 50

## Design and First Experience of the Prototype Pixel Layers for the ALICE FoCal

**Author:** Tea Bodova<sup>1</sup>

<sup>1</sup> *University of Bergen (NO)*

**Corresponding Author:** tea.bodova@uib.no

University of Bergen is involved in developing two calorimeters: (1) the pixel section of the Electromagnetic Forward Calorimeter (FoCal-E) for the ALICE Upgrade and (2) the Digital Tracking Calorimeter (DTC) for the proton Computed Tomography (pCT) prototype. Both designs utilize the ALPIDE sensors which are connected to aluminum-polyimide flexible cables applying Single-point Tape Automated Bonding (SpTAB). This contribution describes the development of the first multi-chip string prototypes, their performance, and the characterization of the high-speed links of the front-end electronics and towards the readout. Moreover, we present the experience with the prototypes both in the laboratory and test beam setups.

#### Summary (500 words):

Both FoCal-E and pCT will arrange the ALPIDE sensors in so-called strings. A string consists of several ALPIDE sensors, a chip cable, and a flex cable. The cables are assembled using adhesiveless polyimide-aluminum flexible cables. Each individual sensor is SpTABed (otherwise known as ultrasonic welded) to a shorter single-layer flex (called chip cable). Multiple of these are then bonded to a longer double-layer flex cable, see Figure 1. This flex cable has a stiffener at the end to ease the insertion of the string in a

ZIF connector. Furthermore, passive SMD components such as termination resistors and capacitors are soldered on the aluminum traces of the flex cable. For improved handling, groups of strings are glued side by side on a metal carrier.

To ensure one large active area, two carriers can be positioned either face-to-face (as in pCT) or back-to-back (as in FoCal-E). The constraint in both cases is the mechanical design of individual calorimeters. Also, in regard to the absorber material and thickness between the layers. As of now, there are two different segmentation of the string design:

9-chip string for the pCT offering an active area of 15 mm x 270 mm and total dimensions of 27 mm x 310 mm.

15-chip string for the FoCal-E offering an active area of 15 mm x 450 mm and total dimensions of 27 mm x 490 mm.

The string design ensures the typical impedance of 100  $\Omega$  complying with the LVDS lines for ALPIDE sensor. This is important in particular for the 1.2 Gbps data links of the ALPIDE and the total bandwidth of the string. Considering that the ALPIDE sensor requires a recommended operational voltage of about 1.8 V, the string design must also guarantee low voltage drop. This is especially true for the longer 15-chip string. Several prototypes of the 9-chip string have been successfully produced and verified. The first 15-chip string prototype is expected to be produced and tested in 2023. The string development doesn't only take into account the electrical and mechanical quality of the string but the optimization of the production too.

We will present the design approach that ensures good signal and power integrity between the front-end and the off-detector electronics (readout). We will also show the simulations and measurements that verify the design. In addition, a possible solution will be presented on how to connect the string via an intermediate PCB to the readout and power. Finally, we will outline the experience with the SpTAB interconnection technique and the flexible cables.

**Invited / 52**

## **Best Practices in Design Verification of ASICs for High Energy Physics Experiments**

**Authors:** Adithya Pulli<sup>1</sup>; Matteo Lupi<sup>1</sup>; Simone Scarfi<sup>1</sup>; Stefano Esposito<sup>1</sup>; Xavi Llopart Cudie<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** adithya.pulli@cern.ch

As the complexity and costs of ASICs designed for high-energy physics experiments continue to soar, verification emerges as a crucial factor in completing projects within reasonable timelines and budgets. Recognizing the escalating significance of verification, CERN and other high-energy physics institutes have invested significantly in enhancing the rigor of this essential process. In this talk, we emphasize the critical role of verification, delve into the unique challenges posed by ASIC designs in HEP, and discuss a set of best practices aimed at enhancing verification efficiency. By improving the quality of the verification process, these practices pave the way for predictable project execution and improved product outcomes. Drawing on successful experiences from ASIC verification at CERN and lessons learned from ineffective strategies, this talk provides valuable insights for achieving successful ASIC designs in high-energy physics experiments.

**Summary (500 words):**

FE readout ASICs are responsible for receiving analog signals from a sensor, converting them into digital signals, and transmitting the resulting values outside of the ASIC. Typically, a FE readout ASIC includes multiple readout channels, which can range from 1 to over 1,000,000, as well as a data transport layer that combines the data from all active readout channels and sends it to the outside world. Each readout channel is a mixed signal circuit that consists of an analog portion for signal shaping and discrimination and a digital module for measuring one or more characteristics of the digitized signal. The digital

module also carries out functions such as filtering, data compression, and transmission of the resultant values.

FE readout ASICs perform similar functions with minor variations to meet detector requirements. Therefore, to achieve their verification goals, similar verification strategies can be used. Several best-known methods (BKMs) that are applicable to the verification of FE readout ASICs are presented in this paper to summarize these strategies.

The following is a brief list of BKMs discussed in this paper:

1. Design partitioning to handle longer simulation times during netlist verification
2. Greybox reference models to reduce reference model complexity
3. Approximate and precise scoreboarding
4. Readout data recording at a higher abstraction level for offline scoreboarding
5. AMS simulations at the channel level to identify issues at analog/digital boundaries that cannot be found in digital simulations
6. Define and capture Key Performance Indicators (KPIs) such as detection inefficiency, error rates, link losses, etc.
7. Readable register layer and test scenario dump to improve KPI tracking and debugging
8. Reuseable verification components that promote content reuse across projects and enable building complex verification environments with multiple ASICs

Although some of these BKMs are solely related to verification, several also address architectural and design partitioning aspects that significantly impact the verification process. All the BKMs discussed in this paper are based on our experiences of working on various FE readout ASIC projects at CERN. In the contribution, we will elaborate on each BKM and show examples from concluded and ongoing projects on how following them improved verification quality and efficiency.

While most of the BKMs discussed in this paper are already well-known among verification engineers, this article is the first attempt in the HEP community to summarize them for a wider audience. Future FE readout ASIC projects can use these BKMs as design and verification guidelines to avoid common pitfalls that were encountered during the development of various FE readout ASICs designed for HL-LHC upgrades. By following these relevant guidelines, design teams can increase productivity and prevent unforeseen project delays.

**Tuesday posters session / 53**

## **A high frequency radiation hardened DC/DC-converter with low volume air core inductor**

**Author:** Jeremias Kampkötter<sup>None</sup>

**Co-authors:** Michael Karagounis<sup>1</sup>; Rainer Kokozinski<sup>2</sup>

<sup>1</sup> *Fachhochschule Dortmund Univ. of Applied Sciences and Arts (DE)*

<sup>2</sup> *University of Duisburg*

**Corresponding Author:** jeremias.kampkoetter@fh-dortmund.de

The hfrh-buck (high frequency radiation hardened-buck) is a radiation hardened DC/DC-converter operating at a high switching frequency of 100MHz with a small air core inductor of 22nH. To ensure a high radiation dose, the circuit is designed with core transistors of a 65nm TSMC technology. By stacking the transistors of the power stage, the converter can be supplied with a voltage of up to 4.8V. Stable operation can be achieved at an output voltage of 1.2V with a maximum load current of 1A. The prototype demonstrates the ability to power parallel connected hybrid-pixel modules in the innermost layers.

**Summary (500 words):**

The increasing demand for reliable power management systems due to higher luminosity, higher power consumption and higher radiation doses, requires innovative power supply concepts for future applications. Since the detector systems are designed to be as light as possible, the voltage regulators are designed in the same technology as the readout electronics to enable on-chip integration. In a parallel supply approach, the hybrid pixel modules are connected in parallel and supplied by a DC/DC-converter that converts the supply voltage to the desired module voltage.

Low-inductance switching converters are required to meet the strict space requirements and to ensure the operation in high magnetic fields. In addition, the circuit must be able to withstand a high radiation dose of up to 1 Grad. Low-voltage core transistors can withstand a high radiation because their thin gate oxide makes them less susceptible to radiation damage. Since thick gate oxide transistors are used for higher input voltages, the power stage is stacked with four NMOS and four PMOS core devices each. A driver network is required to ensure that the transistors operate within their voltage limits. The chosen driver network monitors the drain potential of the stacked transistors and ensures that the required gate voltage is applied to the devices, depending on the switching state. The presented prototype was designed in a 65nm TSMC technology, while the entire circuit is built using only core transistors. With the selected switching frequency of 100MHz, a small air core inductor of 22nH can be used. The converter can regulate a supply voltage of 4.8V to 1.2V and drive a maximum load of 1A. A voltage controlled PWM regulator is used to control the output voltage. To ensure a safe operation with fast switching edges and a wide duty cycle range, a sawtooth oscillator based on two triangular waveforms that becomes active alternately was chosen. Further features are implemented to ensure a safe operation at high frequencies and to reduce the effects of crosstalk and kickback for the comparators used. The power transistors have to carry high currents with very fast switching edges. In order to sufficiently damp the oscillations at the supply terminals and to prevent the circuit from malfunctions and faulty switching behavior, a careful decoupling of the critical voltages is required. The functionality of the DC/DC-converter is demonstrated by various measurements that confirm stable operation over the entire load range.

Thursday posters session / 54

## The optimization, design and performance of the FBCM23 ASIC for the upgraded CMS beam monitoring system

**Authors:** Grzegorz Jan Wegrzyn<sup>1</sup>; Jan Kaplon<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** grzegorz.jan.wegrzyn@cern.ch

We present the development of the FBCM23 ASIC designed for the Phase-II upgrade of the Fast Beam Condition Monitoring (FBCM) system built at the CMS experiment. The FBCM system should provide reliable luminosity measurement with 1ns time resolution enabling the detection of beam-induced background. The FBCM23 ASIC comprises six channels of fast preamplifier working in transimpedance configuration followed with CR-RC3 shaper and leading edge discriminator. The paper will show the optimization of the design, overall architecture and the detailed implementation in a CMOS 65nm process as well as preliminary electrical performance.

**Summary (500 words):**

The primary role of the FBCM system is accurate luminosity measurement with 1ns time resolution that will provide the detection of beam-induced background. To meet this requirement from the physics point of view, the FBCM sensors should have a certain area and distance to the beam line, balancing occupancy, and acceptance. A good compromise between the area and position of the sensor is provided by 1.7×1.7mm silicon pad installed at a radius around 14.5cm. The radiation environment in this position is rather harsh, and the detector modules should stand up to 200Mrad of TID and particle fluxes up to  $2.5 \times 10^{15}$  N/cm<sup>2</sup> 1MeV equivalent. Although the 65nm CMOS process can stand the expected TID dose without major issues, the increase of the leakage and degradation of charge collection efficiency (CCE) from the heavily irradiated sensors have to be taken into account during the noise optimization of the front-end amplifier and final choice of the sensor thickness. In order to provide a reasonable signal-to-noise ratio (SNR) above 10 at the end of the detector lifetime for any sensor option, the series noise contribution from the input transistor should be kept below 700e- ENC. Figure ENC3D6pF8.pdf

shows the optimization of the input transistor dimensions and the bias for the worst case of 6pF input capacitance (e.g. 120 $\mu$ m sensor plus the parasitics).

The schematic of the preamplifier stage is shown in FBCMpreampTWP.pdf file. The input stage is built with the regulated telescopic cascode amplifier, with the NMOS input transistor of 2000/0.2  $\mu$ m biased with 2.1mA and loaded with low voltage cascode PMOS sources. The simulated open loop gain and GBP is around 69dB and 3.5GHz respectively. The preamplifier works in transimpedance configuration with selectable feedback resistor (25 or 50kOhm). The block diagram of the full channel is shown in FBCM-chanTWP.pdf file. The transimpedance preamplifier is DC coupled to the booster amplifier and leading edge discriminator. Although this intrinsically provides good stability of the baseline in case of high and variable hit rates, it is a less satisfactory solution from the standpoint of the mismatch variation which is amplified by DC-coupled stages. The DC variation at the discriminator input is nearly 100mV pk-pk and to compensate for this, two 8-bit threshold DAC's per channel have been employed. Another 8-bit DAC, common for the chip, is used for the global offset setting. The final gain of the full chain is around 60mV/fC. The adjustable RC filter provides adjustment of the peaking time between 6 and 8ns what helps in the optimization of SNR for various input load conditions. The outputs of the discriminators are sent outside the chip through SLVS interfaces. The ASIC comprises an internal calibration circuitry allowing for in-situ characterization of the chip. All bias and configuration registers are accessible via standard I2C interface. The FBCM23 ASIC has area of 3 $\times$ 3mm<sup>2</sup>. The chip has been submitted for MPW in May and the preliminary results from the electrical characterization are expected at the time of the workshop.

ASIC / 55

## A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs.

**Author:** Gianmario Bergamin<sup>1</sup>

**Co-author:** Alexandre Pierre Soulier<sup>2</sup>

<sup>1</sup> CERN

<sup>2</sup> Université Clermont Auvergne (FR)

**Corresponding Author:** gianmario.bergamin@cern.ch

The combination of 3D tracking and high-precision timing measurements has been identified by the European Committee for Future Accelerators as a fundamental requirement to increase detection capabilities for future applications. Among others, on-chip high-quality clock is a key factor determining the overall resolution of Timing ASICs. However, in large and dense chips, power-grid drops can severely affect the non-deterministic jitter of the clock, representing a limit to the performances. This contribution aims at presenting a simulation framework based on commercial tools to evaluate power supply-induced jitter, providing a pre-silicon methodology to assess its impact on timing indeterminism.

### Summary (500 words):

The European Committee for Future Accelerators (ECFA) has identified high precision timing measurement as a critical research area for future accelerators. To address the challenges posed by increased luminosity and large particle track pile-up, the use of "4D techniques", which involve 3D tracking and Time of Arrival evaluation, is essential for improving vertex location in future High-Energy particle detectors.

High-performance sampling and high precision timing distribution are essential elements to be considered when dealing with resolutions on the order of tens of picoseconds. In this context, the classical approach of TDC-based chains is highly dependent on the quality of the reference clock distributed on ASIC to each measurement channel. The continuous scaling and integration of VLSI technology pose a severe limitation to the quality of the clock due to the phenomenon of power supply-induced jitter: the dynamic iR drop generated by the running logic reflects into a non-deterministic transition time of the CMOS logic, and eventually to an uncertainty in the time of arrival of the reference clock. Large Pixel ASICs are more sensitive to this phenomenon due to the commonly known limitations of power PADS position, area, and routing resources availability.

A simulation-based methodology exploiting commercial tools has been developed to correlate the ASIC activity with the induced clock jitter, to derive the non-deterministic components to be added as uncertainty in the measured value.

First, the digital-on-top design is simulated with digital tools and different stimuli, ranging from low activity (similar to an idle state) to high activity. The extracted activity information is then used to perform dynamic power and IR drop analysis, where the effective instance voltage (EIV), calculated as the difference between the supply and ground seen by the clock buffers, is derived and recorded at every cycle. Analog simulators are then used to simulate the extracted clock network together with the EIV values annotated per each cell, allowing to derive the real arrival time of the clock to all the sinks for every cycle. Finally, the contribution to the non-deterministic part of the jitter can be calculated identifying the two cycles with maximum difference in clock arrival time.

The proposed methodology provides the designer with a powerful tool to estimate the power supply induced jitter on clock trees, showing the effect of ASIC activity into the real arrival timing of the reference clock, allowing also further optimizations before tapeout. The technique will be shown together with its application to the Altiroc3 ASIC, where the results clearly reflect the internal floorplan and power distribution characteristics.

## System Design, Description and Operation / 56

# Cryogenic Charge Readout Electronics for the ProtoDUNE-II Program and DUNE

**Authors:** Roger Guo Huang<sup>1</sup>; Roger Huang<sup>1</sup>

<sup>1</sup> *Lawrence Berkeley National Lab. (US)*

**Corresponding Authors:** roger.guo.huang@cern.ch, rghuang@lbl.gov

The upcoming ProtoDUNE-II program at the CERN neutrino platform will consist of 2 liquid argon time projection chambers, which will serve as demonstrators of the technologies that will be used in the first 2 far detectors of the Deep Underground Neutrino Experiment (DUNE). A core component of these detectors is the cryogenic charge readout electronics, which are immersed in liquid argon along with the detectors and are responsible for reading out charge signals from the anodes of the time projection chamber. This talk will discuss the design of these electronics and preliminary performance results from the ProtoDUNE-II assembly experience.

### Summary (500 words):

The DUNE far detectors require readout of several hundred thousand charge-sensing channels immersed in the largest liquid argon time projection chambers ever built, calling for cryogenic front-end electronics in order to be able to adequately instrument the full detector. These electronics must satisfy power constraints of < 50 mW per channel to minimize the thermal load on the cryogenic system, be designed with lifetimes of 20+ years to remain functional throughout the expected lifetime of DUNE, and be able to reliably communicate with warm interface electronics on the other side of cold cables that are up to 30 meters long.

The cryogenic front-end electronics that will be used for charge readout of the first far detector and the bottom half of the second far detector of DUNE satisfy these requirements with a front-end motherboard (FEMB) containing a chain of 3 different ASICs: LArASIC for analog charge amplification, ColdADC for digitization into 14-bit signals, and COLDATA for multiplexing, serialization, and digital control. Each FEMB operates in liquid argon, placed directly on the detector module and reading out 128 channels with a combination of 8 LArASIC, 8 ColdADC, and 2 COLDATA. The ProtoDUNE-II experiments contain FEMBs with the final designs of each of these ASICs and will serve as the final large-scale testbeds for their performance in a DUNE-style detector collecting physics data, including the same electronics grounding scheme that will be used in DUNE and including full integration testing with the other DUNE detector components.

Although the ProtoDUNE-II experiments have not yet begun operation, the cold ASICs have undergone individual quality control tests prior to installation on the detectors, and the fully assembled constituent

detector modules have been individually tested in coldbox setups at the CERN neutrino platform prior to installation in their final positions in the ProtoDUNE-II cryostats. The results of these tests are being used to refine the testing procedures that will be used for the electronics prior to their installation on the DUNE detector modules, and for the assembled DUNE detector modules prior to their installation in the DUNE far detectors. Over the course of these tests we have ascertained a > 99% good yield in manufactured ASICs and a < 0.1% loss of electronics channels after installation on the detector modules. We have also measured pedestal RMS noise levels of < 500 electrons equivalent noise charge (ENC) on collection channels and < 600 electrons ENC on induction channels while the detector is under cryogenic operating conditions, far surpassing the < 1000 electrons ENC pedestal noise required by DUNE.

**Tuesday posters session / 57**

## SiC based beam monitoring system for particle rates from kHz to GHz

**Author:** Simon Emanuel Waid<sup>1</sup>

**Co-authors:** Andreas Gsponer<sup>1</sup>; Jürgen Maier<sup>1</sup>; Philipp Gaggel<sup>1</sup>; Richard Thalmeier; Thomas Bergauer<sup>1</sup>

<sup>1</sup> *Austrian Academy of Sciences (AT)*

**Corresponding Author:** [simon.waid@oeaw.ac.at](mailto:simon.waid@oeaw.ac.at)

The extremely low dark current of silicon carbide (SiC) detectors, even after high-fluence irradiation, is utilized to develop a beam monitoring system for a wide range of particle range, i.e., from the kHz to the GHz regime. The system is completely built from off-the-shelf components and is focused on compactness and simple deployment. Beam tests on a 50 μm thick SiC detector reveal, that even single particles of a 62.4 MeV proton beam (equivalent to 5.03 MIP) can be detected. Overall accurate results can be achieved up to a particle rate of 10<sup>9</sup> particles per second.

### Summary (500 words):

SiC is, due to its intrinsic material properties, an attractive detector material. On the one hand the, compared to silicon, very high displacement energy results in a potentially increased resilience against radiation damage. The low leakage current, on the other hand, allows to deploy SiC detectors without any dark current compensation, even when the particle flux is measured in DC coupled mode. The fact that the leakage current does not even increase for samples irradiated at up to 10<sup>16</sup>  $\frac{n_{eq}}{cm^2}$  1 MeV neutron equivalent flux is another big advantage. Overall, these properties make SiC a very interesting material for beam monitors measuring fluxes which have to be distinguished from single particles monitors but still provide the possibility to detect the latter.

In this work we report on a beam monitoring system which is based on 4H-SiC strip detectors. The system was designed for particle rates ranging from the kHz to the GHz regime. In the kHz regime, the system operates in single particle counting mode. At particle rates in the GHz regime, the DC current through the detector is measured, which is proportional to the particle flux. We designed the system using only commercial off the shelf (COTS) components, omitting the long and expensive development of a front-end application specific integrated circuit(ASIC). At the core of the system, a commercial X-Ray thin film transistor (TFT) front-end chip is utilized for sensor readout. A 14 bit analog digital converter (ADC) provides accurate current measurements while a freely programmable gate array (FPGA) with built-in central processing unit (CPU) is responsible for data read-out and transmission to the host computer.

Emphasis was put onto making the system compact and easy to integrate. A single Ethernet port is used for both, controlling the system and data transfer. Only a single high voltage supply for the detector and an unregulated low-voltage is required to supply the system.

Beam test using a 50μm thick 4H-SiC pad detector prove our system sufficient to count single particles when subjected to a 62.4 MeV proton beam (particle energy equivalent to 5.03 minimum ionizing particles, MIP).

Using a Si strip detector, the setup was employed to reveal the time structure of the proton beam of the

MedAustron facility. The system can sample 128 strips at a rate of 37 kHz. It works at beam rate up to  $10^9$  particles per second, with intensity peaks being up to an order of magnitude larger.

**Thursday posters session / 58**

## **Universal test system for boards hosting bPOL12V DC-DC converters.**

**Author:** Krzysztof Stachon<sup>1</sup>

**Co-authors:** Guenther Dissertori<sup>1</sup>; Tomasz Gadek<sup>1</sup>; Werner Luster<sup>1</sup>

<sup>1</sup> *ETH Zurich (CH)*

**Corresponding Author:** krzysztof.stachon@cern.ch

ECAL Barrel (EB) and MTD Barrel Timing Layer (BTL) subdetectors of the CMS are approaching series production of electronic boards, including voltage conditioning PCBs: LVR and PCC respectively. 2448 LVRs and 864 PCCs will be installed during LS3 of the LHC. These boards are hosting radiation-tolerant bPOL12V ASICs which convert a broad input voltage range into required voltage levels for microelectronics between 1.2–2.5V. Each card must be tested multiple times at various production stages to ensure its quality. This contribution describes a methodology of testing bPOL12V conversion quality including the detection of instability regions at certain load levels.

### **Summary (500 words):**

CMS phase II upgrade is approaching the series production of electronic components which will be installed during LS3 and must reliably operate in the HL-LHC era. Testing these electronic boards prior to installation is crucial to ensure the proper operation of subdetectors because maintenance and replacement of faulty boards is not foreseen within their lifetime.

There was a common decision in the CMS to use bPOL12V for the point of load DC-DC conversion. These ASICs convert 7-12 V supplied to the detector into 1.2-2.5V required to supply microelectronics. EB and MTD BTL use them on boards conditioning voltage –Low Voltage Regulator (LVR) and Power Conversion Card (PCC) respectively.

We designed a universal testing methodology which will be applied to both mentioned PCBs. Testing equipment, validation conditions and data storage will be described in this contribution with a particular focus on instability regions detection of bPOL12V converters.

The test system architecture is presented in Figure 1. DMM with waveform acquisition is a key component to assess whether we are in the region of instability of the bPOL12V converter. It is acquiring output voltage with a 100 kHz sampling rate for a period of 20 ms. Based on standard deviation (SD) or pk-pk of this waveform we discriminate whether there are oscillations at certain operating points. Example comparison of stable and unstable operation is shown in Figure 2. Oscillations measured are periodic, sine-shaped signals, which are usually within 10-20 kHz range with a pk-pk value of up to 40 mV.

On top of the equipment, a dedicated Python software with a GUI was implemented, which may be used by unskilled personnel to perform a full test of a board. To assess the quality of PCBs, the program validates:

- Initial temperature and thermal equilibrium of the PCB
- Idle input current and output voltages
- Input current when all channels are disabled (enable pin of bPOL12V is used)
- Load regulation curve
- Conversion efficiency versus load curve
- Voltage SD versus load curve

For scalar values, we check whether values are within fixed (configurable) bounds. For load-dependent curves, we use a template curve fit to obtain a scalar value from the plot and then compare it with fixed



bounds.

Each production board has its unique barcode and test data is stored in a relational database, which will be kept until the end of the lifetime of the detector. We expect to have a few measurements for each PCB, done at certain stages of production.

The test system was validated with the final PCB prototypes: 80 PCC boards and 52 LVR boards hosting 448 conversion channels in total. Based on that, preliminary bounds were determined that will be used in the factory acceptance test. Validation methods proposed not only determine completely faulty boards, but also boards that have significant deviation from the expected distribution (are outliers). These outliers will be assessed on the individual basis and, if the deviation does not prevent from using them, they are kept as spare parts.

ASIC / 59

## Testing and characterisation of the prototype readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker

**Author:** Michael Grippo<sup>1</sup>

<sup>1</sup> *Universita e INFN Torino (IT)*

**Corresponding Author:** michael.grippo@cern.ch

This talk describes the characterisation and validation campaign of the prototype of the CMS Readout Chip (CROC), a 65 nm CMOS pixel readout ASIC for the CMS Inner Tracker upgrade for High Luminosity LHC. This validation campaign includes tests with single-chip and multi-chip modules, irradiation campaigns, test beams and wafer-level tests. The main results obtained in the testing of the CROC prototype will be outlined. Key improvements and fixes that have been implemented in the final version of the chip before the summer 2023 submission will be described.

### Summary (500 words):

The CMS Readout Chip (CROC) is a 65 nm CMOS hybrid pixel readout chip for the High Luminosity LHC upgrade of the CMS Inner Tracker. The new detector will be instrumented with approximately  $13 \times 10^3$  of these readout chips, covering an area of about  $5.2 \text{ m}^2$ .

The chip must be able to withstand very high radiation doses (500 Mrad) and hit rates ( $3 \text{ GHz/cm}^2$  on the innermost tracking layer) during operation. Moreover, it must handle an increased sensor granularity ( $2500 \mu\text{m}^2$  pixels) with respect to current detectors and operate at low detection thresholds (1000 e-).

In order to fulfill these challenging requirements, the RD53 collaboration has been established in 2013, with the task of developing the readout chips for both the CMS and ATLAS inner tracker upgrades for HL-LHC. The collaboration first studied the radiation hardness of the 65 nm CMOS technology and found it suitable for the development of the chip. After that, the required radiation-hard IP blocks (ADC, DACs, PLL, analogue pixel front-end, ...) were developed and validated.

A prototype (CROCv1) has been submitted in 2021. The chip includes a low-power, linear analogue front-end, charge measurement with a time-over-threshold counter, several mitigations for radiation-induced problems (such as the triplication of important storage elements) and a novel powering scheme designed to reduce the material budget of the detector. The mitigation of radiation-induced effects in storage elements is particularly important, given that, during operation, it is estimated that the data in about 100 storage elements will be corrupted by radiation every second even with triple redundancy.

Twenty wafers of the prototype chip have been produced, amounting to 2760 chips. Several of these wafers have been used to produce single-chip cards, detector module prototypes, and for sensor hybridisation. More than half of these wafers have been subjected to wafer-level testing in order to discard the dies with manufacturing problems or insufficient performance and to commission the waferprobing facilities for production testing.

The prototype chip has been thoroughly studied and its suitability for operation at HL-LHC has been assessed. The chip has been studied in single-chip assemblies, in prototype detector modules with bump-bonded sensors, and at wafer-level. The performance of fresh and irradiated CROCv1 ASICs has also been studied in several beam tests, bump-bonded to sensors with different technologies (planar, 3Ds). The characterisation and verification campaign has, overall, demonstrated the radiation resistance of the chip and its performance, but a few important improvements have been identified. These improvements have been implemented in the final version of the chip, before the summer 2023 submission.

In this talk, key results from the characterisation and validation of the CROCv1 will be described. The submission of the final version of the chip will also be mentioned, along with the most important improvements and fixes that have been implemented in the CROCv2.

## Trigger and Timing Distribution / 60

# CMS Level-1 trigger Data Scouting firmware prototyping for LHC Run-3 and CMS Phase-2

**Author:** Rocco Ardino<sup>1</sup>

<sup>1</sup> *Universita e INFN, Padova (IT)*

**Corresponding Author:** rocco.ardino@cern.ch

A novel Data Acquisition (DAQ) system, known as Level-1 Data Scouting (L1DS), is being introduced as part of the Level-1 (L1) trigger of the CMS experiment. The L1DS system will receive the L1 intermediate primitives from the CMS Phase-2 L1 trigger on the DAQ-800 custom boards, designed for the Phase-2 central DAQ. Firmware is being developed for this purpose on the Xilinx VCU128 board, with features similar to one half of the DAQ-800, and validated in a demonstrator for LHC Run-3. This contribution describes the firmware development in view of the target design for the DAQ-800.

### Summary (500 words):

A novel Data Acquisition (DAQ) system, known as Level-1 Data Scouting (L1DS), is being introduced as part of the Level-1 (L1) trigger of the CMS experiment. The L1DS is complementary to the central CMS DAQ and it captures the L1 intermediate primitives produced by the trigger processors at the full 40 MHz bunch crossing rate. The system will provide vast amounts of data for multiple purposes, such as trigger diagnostics, luminosity measurements and the study of otherwise inaccessible signatures, either too common to fit in the L1 accept budget, or with requirements orthogonal to the standard physics triggers. For the High-Luminosity LHC upgrades, the L1DS system will receive the L1 intermediate primitives from the upgraded L1 trigger, capable of sophisticated feature searches with resolution often similar to the offline reconstruction. The DAQ-800 custom boards, designed for the CMS Phase-2 central DAQ and with an ATCA form-factor, will be used to collect data from the L1 processors over high-speed optical links. The DAQ-800 board is capable of accepting up to 48 L1 input links for a total of 1.2 Tb/s. The maximum theoretical output bandwidth being 1 Tb/s, a moderate data reduction will be necessary to allow the board to operate at a steady output data rate of 800 Gb/s. The data pre-processing logic will be implemented on the two Xilinx Ultrascale+ VU35P FPGAs hosted on the board and chosen for their built-in High-Bandwidth Memory (HBM). The latter is required for the central DAQ unit to provide sufficient data buffering between the LHC-synchronous back-end and COTS switched network, relaying data to standard compute servers. The L1DS will use a custom firmware implementation of the TCP/IP protocol on the DAQ board FPGAs, to transfer L1 primitives to a set of data servers, where they will be stored in memory prior to being sent to a computing farm for the final processing. The L1DS firmware is being developed on the VCU128, a Xilinx development board with features similar to one half of the DAQ-800 boards. The development is currently being validated in the LHC Run-3 demonstrator of the L1DS, which captures the primitives from the Global Muon Trigger (GMT) and Calorimeter Trigger, the trigger decision bits from the Global Trigger output and the input stubs to the Barrel Muon Track Finder (BMTF). Additionally, machine learning inference applications can be deployed directly on the FPGA to enhance the analysis capabilities of the L1DS. This contribution describes the scouting firmware development carried on the VCU128 board in view of the Phase-2 target design for the DAQ-800 custom board.

**Tuesday posters session / 61****40MHz trigger-less readout of the CMS Drift Tube muon detector****Authors:** Andrea Triossi<sup>1</sup>; Jacopo Pazzini<sup>2</sup>; Matteo Migliorini<sup>1</sup><sup>1</sup> *Universita e INFN, Padova (IT)*<sup>2</sup> *Università e INFN, Padova (IT)***Corresponding Author:** m.migliorini@cern.ch

The Level-1 trigger scouting system of the CMS experiment aims at intercepting intermediate data produced by the L1 trigger processors, before the final trigger decision.

This system can be complemented by adding the raw stream of data collected from the detector front-end, where the throughput is manageable. An implementation of the triggerless readout is realized by reading a sector of the CMS Drift Tubes detector, which has been equipped with the preproduction of Phase-2 upgrade front-end boards. A Xilinx VCU118 acts as a concentrator of the Phase-2 demonstrator lpGBT links and transmits data to a server via 100G TCP/IP.

**Summary (500 words):**

The 40 MHz L1-trigger scouting project of the CMS experiment aims at capturing intermediate data produced by the L1 trigger processors at the full bunch crossing rate, to perform online analysis independently of the final trigger decision. The system works as a parallel readout chain that processes copies of the streams between the L1 trigger boards, which are obtained via spare optical links. The data is then concentrated using commercial FPGA development boards and transmitted to dedicated computing resources.

The stream of L1 trigger primitives can be complemented with the raw stream of data collected from detector front-end boards, when the throughput is manageable for the links bandwidth and computing resources. This would enable the reconstruction of physics processes without the bias introduced by the L1 trigger, on top of real-time diagnosis of the detector status.

The CMS Drift Tubes (DT) muon detector offers a perfect candidate for the implementation of a triggerless-readout system thanks to its low occupancy. One of the sectors has been equipped with phase-2 front-end boards, the OBDT (On detector Board for the Drift Tube chambers), which digitizes the front-end signals and transmits them to the L1 trigger boards via high-speed optical links using the lpGBT protocol. Using spare links in the OBDTs, a copy of the data is sent also to the 40MHz DT scouting system. A commercial evaluation board, the Xilinx VCU118 evaluation board, is used to collect the front-end links. The receiver has been implemented using the CMS EMP firmware framework which contains an FPGA implementation of the lpGBT decoder and necessary components for interfacing with the CMS Timing and Control Distribution System (TCDS). Input streams from the lpGBT links are merged into frames and transmitted to dedicated servers via 100G TCP/IP links, implemented using a scalable network stack for FPGA developed by ETH. This framework was chosen as, in addition to TCP/IP and UDP/IP implementations it supports ROCEv2 (RDMA over Converged Ethernet), the target protocol for this system. In this scenario, the current TCP/IP implementation is used as a starting point of the development and for performance comparisons with ROCE.

**Tuesday posters session / 62****System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC****Author:** Tom Williams<sup>1</sup>

<sup>1</sup> *Rutherford Appleton Laboratory (GB)*

**Corresponding Author:** tom.williams@cern.ch

For the High-Luminosity Large Hadron Collider era, the trigger and data acquisition system of the Compact Muon Solenoid experiment will be entirely replaced. Novel design choices have been explored, including ATCA platforms with SoC controllers and newly available interconnect technologies with serial optical links with data rates up to 28 Gb/s. Trigger data analysis will be performed through sophisticated algorithms, including widespread use of Machine Learning, in Xilinx UltraScale+ FPGAs. The system will process over 50 Tb/s of detector data with an event rate of 750 kHz. The system design and prototyping are described and examples of trigger algorithms reviewed.

**Summary (500 words):**

The High-Luminosity LHC will open an unprecedented window on the weak-scale nature of the Universe, providing high-precision measurements of the standard model, as well as searches for new physics. Such precision measurements and searches require information-rich datasets with a statistical power that matches the high luminosity provided by the upgrade of the LHC. Collecting those datasets efficiently will be a challenging task in the harsh environment of 200 proton-proton interactions per LHC bunch crossing.

For this purpose, the Compact Muon Solenoid (CMS) collaboration has designed an efficient data-processing hardware trigger (Level-1) that will include tracking information and high-granularity calorimeter information [1]. The system design will take full advantage of advances in FPGA and link technologies over recent years, providing a high-performance, low-latency (<12.5 us) computing platform for large throughput and sophisticated data correlation across diverse data sources.

Modern technologies offer an effective solution to achieve these goals. The upgraded system will make use of Xilinx UltraScale+ FPGAs hosted on ATCA hardware platforms, including SoC controllers and communicating through optical interconnects at up to 28 Gb/s.

In order to enable the physics programme sophisticated trigger algorithms are required, for example to combine data from different detector elements optimally. Machine Learning algorithms will be used widely and a range of algorithms have been prototyped, in many cases using High Level Synthesis tools to produce firmware which has been tested in prototype hardware.

The talk will cover the technological aspects of the HL-LHC upgrade to the trigger system, emphasising the results of recent prototyping and slice tests, and their impact on the system design. Examples of conventional and Machine Learning algorithms that have been implemented and tested in prototype boards will also be presented.

[1] CMS Collaboration, The Phase-2 Upgrade of the CMS Level-1 Trigger, CERN-LHCC-2020-004 (<http://cds.cern.ch/record/>

**Tuesday posters session / 63**

## **CMS HGCal Electronics Vertical Integration System Tests**

**Author:** Milos Vojinovic<sup>1</sup>

**Co-authors:** André David<sup>2</sup>; Arnaud Steen<sup>2</sup>; Jan Troska<sup>2</sup>; Mehmet Ozgur Sahin<sup>3</sup>; Paul Dauncey<sup>1</sup>; Raghunandan Shukla<sup>1</sup>; Stavros Mallios<sup>2</sup>

<sup>1</sup> *Imperial College (GB)*

<sup>2</sup> *CERN*

<sup>3</sup> *Université Paris-Saclay (FR)*

**Corresponding Author:** milos.vojinovic@cern.ch

In preparation for the High-Luminosity era of the LHC, the CMS experiment will replace the existing calorimeter endcaps with a novel device - the High Granularity Calorimeter (HGCal), having around six million readout channels. The electronics system for this upgrade project is highly specialised and complex, involving multiple layers of data transfer, so testing must be carefully planned. The strategy has been to split the efforts between vertical (start-to-end) and horizontal (parallelisation) test systems. An important milestone for the former has been the development and operation of test systems to prototype one vertical slice of the future endcap electronics system.

#### Summary (500 words):

As for the final detector, the test systems consist of front-end (on-detector) electronics hardware with prototype custom ASICs and a back-end (off-detector) ATCA board (Serenity) running custom firmware and software. In addition, in both its front-end and back-end segments, the test system readout is split into two parts for the readout of coarse granularity data (for the trigger system) and high granularity data (for full event readout). The trigger back-end is responsible for using the coarse data to decide if the corresponding event should be read out in high definition. The DAQ back-end is also responsible for distributing a precise timing reference to both the front-end systems and also for their control and configuration.

The main goals of the tests have been to verify various kinds of data exchange between the front-end and the back-end electronics, specifically the timing distribution, slow and fast control, acquisition of coarse and high-definition data, etc., across all the relevant interfaces. The success in all these activities will allow the project to move towards horizontal system scaling. Everything listed, except the readout of the high-definition data (where the relevant prototype data concentrator ASIC is not yet fabricated), has now been achieved.

Specifically, the clock reference brought from the back-end can be reliably recovered in the front-end ASICs such that the two parts are fully synchronised. The clock phase noise jitter was measured to be 8.5 ps, well below the 15 ps specification. Regarding slow control, it is possible to read from and write to any register of any ASIC existing in the front-end. The reliability of the former was tested by performing O(1M) write and readback slow control transactions with the front-end ASICs. Considering fast control, the back-end can send various fast commands to the front-end ASICs and confirm their proper reception by receiving ASIC responses as per design. The front-end readout (ROC) ASICs can be configured to send user-defined trigger data. These data can then be transmitted through a sequence of several additional front-end ASICs, complete their journey via the fibre-optic channel to the back-end and be unpacked by the back-end firmware where they precisely match what the readout ASICs were configured to originally send out. In doing so, stable data acquisition from the front-end to the back-end was observed over a period of O(days) when a total of O( $10^{15}$ ) bits were transmitted without errors. The key challenges of this work were to integrate all the moving parts (which are coming from different worldwide institutes) and operate them together, synchronously, in a single system.

This presentation will give a general overview of the vertical HGCal electronics test system activities at CERN. Namely, it will illustrate the architecture of the test systems, explain how the prototypes are related to a vertical slice of the future endcap electronics system, and summarise the central objectives that have been achieved to date. In addition, it will give an outlook into future test system activities.

#### Tuesday posters session / 64

## Design of a very low power 12 bits 40 MS/s ADC based on a time-interleaved SAR architecture

**Authors:** Bontems William<sup>None</sup>; Daniel Dzahini<sup>1</sup>

<sup>1</sup> Tima Laboratory / CNRS

**Corresponding Authors:** [william.bontems@grenoble-inp.org](mailto:william.bontems@grenoble-inp.org), [dzahini@univ-grenoble-alpes.fr](mailto:dzahini@univ-grenoble-alpes.fr)

The paper describes a new figure of merit reachable in term of very low power dissipation for a 12 bit, 40MS/s Analog to Digital Converter in a CMOS 65nm process with 1V power supply. A

differential time interleaved successive approximations register architecture is used. Each individual ADC channel is optimized regarding power consumption hence parallelizing 28 ADC channels in an analog memory like method, the total power consumption is only 280 $\mu$ W including all the reference voltage drivers and the digital sections. The total layout area of this converter is 0.87 mm<sup>2</sup>. Crosstalk simulations results will be discussed regarding channel-to-channel discrepancies.

#### Summary (500 words):

In view of next generation of high granularity detectors, the necessary density for the readout systems leads to the design of various multichannel integrated circuits. 64 or 128-channel chips are becoming common. In the same time there is an increasing need to reduce the power dissipation. Since digitization stages are more and more integrated within the front-end circuit, low power and high resolution converters will play a key role in next generation read-out circuits. We introduce here one low power solution based on time interleaved SAR converters. Many publications pointed out that SAR ADC in 65nm process or below becomes one of the best choice for power reduction. In the same time many laboratories has published in the past very aggressive design based on so called "analog memories" which are array of sampled capacitors with or without input buffers. In the present design, we combine these two concepts to display a more aggressive feature in low power ADC.

Usually time interleaved ADC targets high-speed results (beyond GS/s). Nevertheless, our simulations results show that even around 40MS/s we can reach lower power dissipation compared to other Nyquist architectures (pipelined, fast SAR or even pipelined SAR). A fast sampling feature combined with a set of slower conversion stages, help finally to save power because the constraints on dynamic power is relaxed. In our design, each channel of ADC is coming with its own reference buffers. This helps to reduce significantly the crosstalk. The input sampling path includes bootstrap switches to compensate the linearity issues. We target in the present design 12 bits 40MS/s interleaving 28 ADC channels, each one converting at 1.5MS/s, based on a segmented array of capacitors. Due to the sensitivity of segmented architectures to mismatch and parasitic capacitors, we include an additional automated trimming algorithm to make the design robust against non-linearity and distortions issues. According to our simulations, the total power dissipated is only 280 $\mu$ W when sampling at an equivalent frequency of 40MS/s. The layout of each elementary ADC channel occupy an area of 40 $\mu$ m\*780 $\mu$ m. Hence, the total 28 interleaved ADC area is about 0.87mm<sup>2</sup>. The layout is organized to path the way for future multi-channels 40 MS/s ADCs.

#### Thursday posters session / 65

## Ionizing Radiation Influence on 28-nm MOS Transistor's Low-Frequency Noise Characteristics

**Author:** Martin Apro<sup>None</sup>

**Co-author:** Alicja Michalowska-Forsyth

**Corresponding Author:** martin.apro@tugraz.at

In this paper, we explore Total Ionizing Dose (TID) effects on low-frequency noise characteristics of 28-nm bulk CMOS transistors. In order to better understand the bias dependence of noise characteristics, measurements were performed at several operating points, both in linear and saturation regions. The challenge of differentiating between DC-induced shifts and newly generated Random Telegraph Noise (RTN) centers contribution to the Power Spectral Density (PSD) curve change demonstrates the insufficiencies of current analysis methods. We present examples of irradiation-generated RTN defects as well as various TID effects on noise PSD curves with pre-existing RTN sources.

#### Summary (500 words):

The origin of low-frequency noise in planar MOSFET transistors has been a point of debate for over 50 years, and it remains unresolved to this day. For older technology nodes, it has a Power Spectral Density (PSD) curve that is proportionally dropping with the frequency; hence, it was named 1/f, or as it is commonly referred to, flicker noise. With the rapid decline in transistor dimensions, occurrence of dominant Random Telegraph Noise (RTN) with a Lorentzian PSD shape (Figure 1) became more frequent. Additionally, for electronics manufactured in deep sub-micron technologies, noise is becoming

one of the most prominent reliability concerns. This is especially the case for electronics that are operating in conditions with constant stressing, such as ionizing radiation environments in high-energy physics experiments. Therefore, it is important to understand what effects can irradiation have on the noise characteristics of transistors used in novel radiation-robust ASIC designs.

Consequently, we exposed transistors fabricated in 28-nm bulk CMOS technology to Total Ionizing Dose (TID) of 1 Grad (SiO<sub>2</sub>). The irradiation campaign was carried out in the Seifert XRD Cabinet, at room temperature, with a tungsten tube biased at 40 kV and 70 mA, resulting in a 6.2 Mrad/h dose rate. The transistors were biased in a diode configuration with 0.9/-0.9 V at the gate and drain terminals of the NMOS/PMOS transistors during the 7-day period of irradiation stressing, as that is the reported worst-case scenario for performance degradation under TID influence. Low-frequency noise was measured before and after the stressing procedure on a custom-built noise-measurement setup, allowing for both time and frequency domain noise data acquisition.

Normalizing the current noise spectral density for the DC current is a common tool used in the pre- and post-stressing analysis. This technique proved valid for PSD spectra with 1/f-like curve shapes, where the existing noise models suggest that taking the DC current into account should negate the difference in noise PSD associated with the irradiation inflicted DC parameter degradation. However, in cases where a dominant RTN defect exists, we demonstrate that normalizing is not an applicable method. This is due to different bias dependencies of RTN defects and 1/f-like noise, indicating an alternative origin.

Firstly, it is important to point out that the pre-irradiation measurements of noise current on minimum-sized transistors exhibit a very high variability (Figure 2). Results of our measurements show that irradiation does not necessarily only increase the noise PSD, but it can also have a non-existent effect and even decrease the overall noise characteristic at a given operating point (Figure 3). Additionally, an example of new dominant RTN trap generation having a great impact on RMS value of noise is shown on Figure 4. Transistors with pre-existing Lorentzian-shaped noise spectra demonstrate a variety of possible changes. In the final paper, we will discuss the multitude of observed variations. The work so far is of qualitative character, as statistically representative data would require more experiments.

## Tuesday posters session / 66

# The CMOS Pseudo-Thyristor: A Zero-Static Current Circuit for Pixelized Detector Front-End Stage

**Authors:** Datao Gong<sup>1</sup>; Jinyuan Wu<sup>1</sup>; Ping Gui<sup>2</sup>; Tiehui Ted Liu<sup>1</sup>; Xianshan Wen<sup>None</sup>; Xing Huang<sup>3</sup>

<sup>1</sup> Fermi National Accelerator Lab. (US)

<sup>2</sup> Southern Methodist University (US)

<sup>3</sup> University of California, Santa Barbara

**Corresponding Author:** jywu168@fnal.gov

A novel ultra-low-power front-end discriminator circuit for pixelized detectors, named pseudo-thyristor, is described. It is based on a positive feedback topology using regular CMOS transistors with zero static current, rather than constantly drawing current in typical discriminators. When a small charge is injected at the input, the circuit flips rapidly due to the positive feedback and output a logic transition for further digitization. Simulation shows that in 65 nm process, it is capable of detecting at a threshold of 5 fC while maintain the average power consumption below 10 micro-Watts when the hit occupancy is <10% for 40MHz operation.

## Summary (500 words):

In contemporary high energy physics detectors, pixelized detectors such as silicon detectors or Low-Gain Avalanche Detectors (LGADs) are widely used for tracking, timing or calorimeters. As a large number of detector elements are used, very low power consumption of the front-end circuits required. In some applications, power consumption of as low as 10 micro-Watts per channel for the front-end is desired. In typical architectures today, the front-end circuits consist of pre-amplifiers and discriminators, each consuming about 1 milli-Watts implemented in 65-180 nm CMOS processes, which is a factor of 100 higher than what is desired in the future. To reduce the power consumption by up to two orders of magnitude, new topologies of the front end design are required. The Pseudo-Thyristor proposed here

is a novel CMOS circuit with zero static current for LGAD-like frontend electronics with the potential to have ultra-low power consumption.

The circuit is a positive feedback topology (which is rarely used in analog frontend circuits) using regular PMOS and NMOS field-effect transistors (FET's). The core of the circuit consists of a pair of PMOS and NMOS FET's with their drain and gate terminals cross connected to form a positive feedback loop. When a small amount of electronic charges is injected into the NMOS gate, both the NMOS and PMOS FET's are turned from OFF to ON state similar to a thyristor, except that in both ON and OFF states, the static current of the circuit is almost zero (with small leakage currents in deep nanometer fabrication processes) as in most digital CMOS circuits. The proposed thyristor is capable of converting a small input charge into a logic level transition and afterward can be reset from ON to OFF state with a set of FET's.

In the typical front-end circuits being used today for HEP, both the preamplifiers and discriminators operate with a static current so that the transistors are in high conductivity region to follow the input pulse at high speed. The topologies used in amplifiers usually employ negative feedback to improve bandwidth and linearity.

However, in pixelized detectors, full waveforms are rarely needed. In many cases, single-bit hits indicating the coordinates of the passing points of charged particles in a tracking detector are sufficient. Beyond that, one may digitize the arrival times of the particle hits and sometimes digitize the pulse widths for time walk correction. In these situations, the requirement of the front-end circuit is nothing more than providing a logic transition. This requirement can be fulfilled using very low power circuits consuming zero static current. Also, since the detector elements produce only one type of charges (negative charges), symmetric topologies in the front-end circuits are not necessary, which further simplifies the circuits and results in lower power consumption.

While the circuit can be at least utilized for 1-bit hit detection in tracking pixel detectors, it is also feasible to apply it for timing walk correction when the 4D detection is demanded, although further simulation and testing are needed.

**Thursday posters session / 67**

## SiGe integrated chip readout for fast timing

**Authors:** Abraham Seiden<sup>1</sup>; Bruce Andrew Schumm<sup>1</sup>; Gabriel Saffier-Ewing<sup>2</sup>; Hartmut Sadrozinski<sup>1</sup>; Hartmut Sadrozinski<sup>3</sup>; Jennifer Ott<sup>1</sup>; Mohammad Nizam<sup>None</sup>; Mohammad Nizam<sup>4</sup>; Simone Michele Mazza<sup>1</sup>; Taylor Shin<sup>None</sup>; Zachary Galloway<sup>2</sup>

<sup>1</sup> *University of California, Santa Cruz (US)*

<sup>2</sup> *Anadyne, Inc.*

<sup>3</sup> *SCIPP, UC Santa Cruz*

<sup>4</sup> *University of California Santa Cruz*

**Corresponding Author:** [simone.michele.mazza@cern.ch](mailto:simone.michele.mazza@cern.ch)

Advances in timing detector technology require new specialized readout electronics. Applications demand high rep rates, below 10 ps time of arrival resolution and, low power. A possible path to achieve O(10 ps) time resolution is an integrated chip using Silicon Germanium (SiGe) technology. Using DoE SBIR funding, Anadyne, Inc. in collaboration with UC Santa Cruz has developed a prototype SiGe front end readout chip optimized for low power and timing resolution (0.6 mW/channel, 10 ps of timing resolution for 8 fC). In this contribution the ASIC performance simulation and the results from the first prototype run will be shown.

### Summary (500 words):

Advances in fast detector technology and the direction of HEP experiments and applications require the development of new specialized readout electronics. Experimental demands include some combination of high rep rates (order of ns dead time), below 10 ps time of arrival (TOA) resolution and low power (between 0.1 mW and 1 mW per channel). A possible path to achieve O(10 ps) time resolution is an integrated chip using Silicon Germanium (SiGe) technology. Using DoE SBIR funding, Anadyne, Inc. in collaboration with University of California Santa Cruz has developed a prototype SiGe front end readout chip optimized for low power and timing resolution, with 0.6 mW per channel (front end and



discriminator) while retaining 10 ps of timing resolution for 8 fC of injected charge. Preamplifier output pulse and timing resolution vs charge and power dissipation are shown in Figure 1.

In the process some insight was developed into the challenges and potential performance of SiGe front end ASICs for future R&D effort. Channel matching to reduce calibration requirements and increase yield, timing resolution at the low end of the proposed detector dynamic range, and temperature stability were all considered during the design process to ensure the prototype performance would be deliverable in a full implementation. During this process we have developed some insight into the challenges and potential performance of SiGe front end ASICs if further R&D were undertaken. The developed single pre-amplifier stage and what is effectively a Time Over Threshold (TOT) discriminator topology is suitable for low repetition rate and quiescent power and sub 10 ps timing resolution applications. The TOT data is required to correct the TOA of pulses over the entire dynamic range of interest. These TOT discriminators are not literal TOT converters of the amplified analog input. The output pulse width of the discriminator is proportional to the input pulse height and have a dead time of up to 10 ns, an improved is necessary to increase the repetition rate capabilities. Some practical considerations for selecting a process for future R&D include the size and power efficiency of the CMOS transistors for the back-end electronics and diminishing performance gains of higher speed SiGe transistors. The currently available SiGe processes offer 130 nm CMOS at a minimum. Transistors faster than 25 GHz have little signal to noise or power improvements to offer when designing readout systems for signals in the 1-2 GHz regime ultra-fast silicon detectors operate in. Moving to faster and smaller SiGe transistors may only introduce unnecessary design challenges such as poor transistor matching, low breakdown voltages, higher Vbe, etc. The current prototype is designed in a 10 GHz process.

The chip production was submitted and will be ready by the end of May 2023, the chip schematic is shown in Fig. 2, Top. A readout board (Fig. 2, Bottom) was designed and will be submitted for production with the same time scale. In this contribution the simulated ASIC performance and the characterization of the first prototype will be shown.

## Power, Grounding and Shielding / 68

# NEW GENERATION B-FIELD AND RAD-TOLERANT DC/DC POWER CONVERTER FOR ON-DETECTOR OPERATION

**Authors:** Agostino Lanza<sup>1</sup>; Emanuele Romano<sup>1</sup>; Simone Ivo Selmi<sup>None</sup>

<sup>1</sup> *Pavia University and INFN (IT)*

**Corresponding Author:** emanuele.romano@cern.ch

The design of a new DC/DC power converter capable of being integrated with a detector is described. It works in harsh environment and can supply up to 170 W per channel. Up to four modules, each one equipped with 8 channels, can be accommodated in a water-cooled compact crate with a small volume of 24 dm<sup>3</sup>. Its electrical, environmental and thermal performance is detailed here.

### Summary (500 words):

The increase in the number of readout channels in new detectors, like the Micro Pattern Gas Detectors (MPGD), in the order of several millions, requires a large amount of electrical power to supply the Front-End (FE) electronics, up to hundreds kW. If this power is generated at long distances from the detector, the voltage drop on the connection cables puts a serious constraint to the maximum supply current, to the wire cross-section and to the power distribution. Furthermore, a large amount of voltage drop on the cables determines regulation and overvoltage issues on the load in case of current transients, and an increased power dissipation on wire resistance.

To mitigate these problems, a new generation DC/DC converter, working in a heavily hostile environment and with a power density greater than 200 W/dm<sup>3</sup>, was developed. It is modular, with up to 4 independent modules, 8 channels each, collected in a water-cooled crate, and can supply the load with an adjustable 10 to 12 V output up to 170 W per channel.

In this contribution, the design constraints of such a converter are analysed, taking as a basis the environmental, electrical and mechanical requirements of the ATLAS New Small Wheel (NSW) project.

Thermal considerations require the converter to be water cooled, and the dimensional constraints impose the adoption of an innovative design to convey the dissipated heat towards the heat exchanger.

The control and monitoring system allows the full remote management of the converter.

Main electrical parameters were measured and are reported here. The converter was also characterised in a harsh working environment, with radiation tests in the CERN CHARM facility beyond the limits estimated for 10 years operation in ATLAS, and with B-field tests in various orientations, using different magnets at CERN up to 1.3 T.

Two design improvements were implemented after the first characterization: a better common mode noise filtering and an optimization of the switching stage. Final performance measurements after the modifications are also reported.

## Trigger and Timing Distribution / 70

### A demonstrator for a real-time AI-FPGA-based triggering system for sPHENIX at RHIC

**Author:** Jakub Kvapil<sup>1</sup>

**Co-authors:** Alejandro Olvera <sup>2</sup>; Callie Hao ; Cameron Dean <sup>3</sup>; Cesar Luiz Da Silva <sup>1</sup>; Dantong Yu <sup>4</sup>; Gunther Roland <sup>3</sup>; Hao-Ren Jheng <sup>3</sup>; Hugo Pereira Da Costa ; Johann Joachim Schambach <sup>5</sup>; John Matthew Durham <sup>6</sup>; Kai Chen <sup>7</sup>; Micol Rigatti <sup>8</sup>; Ming Xiong Liu <sup>6</sup>; Nhan Tran <sup>8</sup>; Noah Wuerfel ; Or Hen ; Pan Li ; Philip Coleman Harris <sup>3</sup>; Song Fu <sup>2</sup>; Xuan Li <sup>6</sup>; Yasser Corrales Morales <sup>1</sup>; Yen-Jie Lee <sup>3</sup>; Youzuo Lin <sup>6</sup>; Zhaozhong Shi <sup>6</sup>

<sup>1</sup> Los Alamos National Laboratory (US)

<sup>2</sup> University of North Texas

<sup>3</sup> Massachusetts Inst. of Technology (US)

<sup>4</sup> New Jersey Institute of Technology

<sup>5</sup> Oak Ridge National Laboratory - (US)

<sup>6</sup> Los Alamos National Laboratory

<sup>7</sup> Central China Normal University

<sup>8</sup> Fermi National Accelerator Lab. (US)

**Corresponding Author:** jakub.kvapil@cern.ch

The RHIC interaction rate at sPHENIX reaches around 3 MHz in pp collisions and requires the detector readout to reject events by a factor of over 200. Critical measurements often require the analysis of particles produced at low momentum. This prohibits adopting the traditional approach, where data rates are reduced through triggering on rare high momentum probes. We propose a new approach based on real-time AI technology, adopt an FPGA-based implementation using a FELIX-712 board with the Xilinx Kintex Ultrascale FPGA, and deploy the system in the detector readout electronics loop for real-time trigger decision.

#### Summary (500 words):

The interaction rate in sPHENIX at RHIC will be increased to 3 MHz for pp collisions. The sPHENIX experiment produces streamed readouts for the MAPS based Vertex Detector (MVTX), Intermediate Silicon Tracker (INTT), and Time Projection Chamber (TPC) tracking detectors and triggered readouts for the calorimeters. Archiving the full detector data streams exceeds the current DAQ bandwidth limits. The proposed triggering system consists of a comprehensive pipeline based on Graph Neural Networks (GNN) to perform online displaced vertex tracklet-based analysis to trigger the TPC streams, enabling efficient data acquisition.

The MVTX and INTT send raw data readout streams (300 kHz and 3 MHz, respectively) into their respective Front-End Link eXchange (FELIX)-712 boards, with six boards for MVTX and eight boards for INTT. The FELIX consists of a Kintex Ultrascale XCKU115FLVF1924-2E FPGA, a 16-lane Gen-3 PCIe card, and 48 transmitter and receiver optical links. Two FELIX-712 will be used to implement the GNN (AI Engine), with each FELIX-712 processing half hemisphere of the MVTX and INTT event. The aim is to reuse the PCIe Interface of the FELIX boards, which allows taking advantage of the FELIX Software Infrastructure. A total of 144 incoming data fibers with 3.2 Gbps bandwidth from MVTX alone must be zero-suppressed, multiplexed, and transferred to the AI engine using SFP+ optical links with 8b10b

encoding. The optical links have been tested for transferring 14 Gbps data rate reliably with a low bit error rate. Consequently, we reduce the number of fibers from 144 to 48. There will be 24 links available for MVTX and 24 links for INTT for each hemisphere.

The AI Engine performs a fast inference for displaced tracks from heavy quark decays. The implementation is based on GNN using PyTorch ecosystem with FlowGNN models. The hls4ml package generates an intellectual property (IP) core for FPGA implementation. The entire latency for the trigger signal must be within the order of 10 $\mu$ s, which leaves the GNN model to perform inferences with less than 5 $\mu$ s latency per event.

Moreover, the reconstruction of heavy flavor particles requires continuous monitoring and adjustment of the beam trajectory, detector alignment, conditions, anomalies, and GNN latent variables. This implies the need for autonomous monitoring and feedback to control the overall real-time workflow. The final system will be based on a CPU/GPU platform connected to the AI engine over the PCIe, creating an embedded system.

The first version of AI Engine is based on the rm-4.11 version of the FELIX-711 Firmware and interfaces the tdaq-09-04-00 TDAQ Release (Software 4.2.4 and Driver 4.9.1). It utilized 51.8% LUT, 38.86% FF, and 59.68% BRAM.

The current effort aims to develop a demonstrator that uses VC-709/FELIX-711 as a data streamer and FELIX-712 as an AI engine to verify the system's feasibility in bandwidth, latency, and FPGA utilization. This is the first trigger R&D at RHIC using a unique hybrid mode of continuous and triggered readouts based on FPGA accelerated AI/ML modules. A deployment is planned for sPHENIX 2024 run and possibly the future Electron-Ion Collider.

## Radiation-Tolerant Components and Systems / 71

### Single Event Effects characterization of a commercial 28 nm CMOS technology

**Authors:** Giulio Borghello<sup>1</sup>; Davide Ceresa<sup>1</sup>; Risto Pejasinovic<sup>2</sup>; Francisco Piernas Diaz<sup>None</sup>; Gianmario Bergamin<sup>1</sup>; Kostas Kloukinas<sup>1</sup>

<sup>1</sup> CERN

<sup>2</sup> University of Novi Sad (RS)

**Corresponding Author:** giulio.borghello@cern.ch

In the context of the Strategic R&D on Technologies for Future Experiments, the sensitivity to single-event-effects of a commercial 28nm CMOS technology was investigated through heavy-ion and proton tests. Two chips were designed to study single- and multi-bit-upset, single-event-transient and single-event-latch-up. Bit upsets were studied on both D-Flip-Flops and foundry SRAMs. LET of heavy ions ranged from 1.3 to 88.39 MeV/mg/cm<sup>2</sup>, with fluences of 5e6 ions/cm<sup>2</sup> for each LET. Protons at 350 and 480-MeV were used. These results provide a comprehensive overview of the SEU sensitivity of the selected 28nm node, representing a milestone in its qualification for HEP applications.

#### Summary (500 words):

In the context of the Strategic R&D on Technologies for Future Experiments, the IC Technology Work Package 5 at CERN (WP5) has targeted 28nm CMOS process as common technology for the most advanced developments for High Energy Physics (HEP) applications. For this reason, a family of 3 ASICs, called EXPloit28 (EXP28), has been designed to study radiation effects on 28nm CMOS technology. This work reports the results of heavy-ions (HI) and proton irradiation campaigns performed on the two of the three chips in the EXP28 family designed for assessing the sensitivity of this technology to Single Event Effects (SEEs).

The first chip (EXP28-SEE) contains structures for studying single-event-transient (SET) and single-event-upset (SEU). The circuit to study SET is based on a vernier detector that allows measuring the

cross-section for transients, estimate transient length and detect multiple transients. Rate and cross-section of SEUs are assessed thanks to 7 matrices of 4096 D-Flip-Flop (DFF), with different threshold-voltage flavours, driving strengths and spacing among the DFFs, and 4 different foundry SRAM types (Single, Single Ultra-High-Density, Dual, Dual Ultra-High-Density).

The second chip (EXP28-ANA) is designed to study Single-Event-Latch-up (SEL). The SEL detector includes both digital and analog structures to evaluate the minimum distance between substrate contacts (taps) needed to prevent SEL.

The HI test was performed at the Heavy Ion Facility (HIF) of UCLouvain. The EXP28-SEE chip was tested for all available ions, at an incident angle of  $0^\circ$  and  $45^\circ$  and at a fluence of  $5e6$  ions/cm<sup>2</sup> for each ion-angle combination. LET ranged from 1.3 MeV/mg/cm<sup>2</sup> to 88.39 MeV/mg/cm<sup>2</sup>.

SET length has shown to increase with LET, ranging from  $\sim 70$  to  $\sim 180$  ps. Multi-SET were measured only for  $LET \geq 62.5$  MeV/mg/cm<sup>2</sup>.

After a  $LET \approx 20$  MeV/mg/cm<sup>2</sup>, errors in SRAMs are dominated by multi-bit-upsets (MBU). These results are confirmed in the DFF structure, where MBUs represent a large fraction of the measured errors. However, no MBU is measured in the matrix with a distance between FF of 5 $\mu$ m. This extremely important result provides the first indication of the minimum distance to avoid MBU, a crucial piece of information in triplication strategies.

The EXP28-ANA was tested with LET ranging from 20.4 to 241.48 MeV/mg/cm<sup>2</sup> and a total fluence of 166.75e6 ions/cm<sup>2</sup>. No SELs were measured in any of the 28 analog and 12 digital structures, even when the supply voltage was increased to 115% of its nominal value.

Protons at 350 and 480-MeV, with a total fluence of  $3.39e12$  p/cm<sup>2</sup>, were used to test 2 EXP28-SEE chips at the TRIUMF facility in Canada. Proton energy had little impact on the results.

Results show an SET length of  $90 \pm 15$  ps, with 81 total hits.

The percentage of MBUs in SRAMs was  $\sim 30\%$  regardless of the SRAM type. No MBUs were measured for protons when the distance between FFs was larger than 5 $\mu$ m.

These results provide a comprehensive overview of the SEU sensitivity of 28nm CMOS technology, representing a milestone in its qualification for HEP applications.

#### Thursday posters session / 72

## The End-of-Substructure (EoS) card for the ATLAS Strip Tracker Upgrade –from Design to Production

**Authors:** Anders Palmelund<sup>1</sup>; Artur Lorenz Boebel<sup>2</sup>; Cameron Michael Garvey<sup>3</sup>; Harald Ceslik<sup>2</sup>; Ingrid-Maria Gregor<sup>4</sup>; James Michael Keaveney<sup>3</sup>; Lars Rickard Strom<sup>2</sup>; Marcel Stanitzki<sup>2</sup>; Max Nikoi Van Der Merwe<sup>None</sup>; Mogens Dam<sup>1</sup>; Peter Goettlicher<sup>2</sup>; René Stennow Godfredsen<sup>1</sup>; Sara Ruiz Daza<sup>2</sup>; Sergio Diez Cornell<sup>5</sup>; Stefan Schmitt<sup>2</sup>

<sup>1</sup> University of Copenhagen (DK)

<sup>2</sup> Deutsches Elektronen-Synchrotron (DE)

<sup>3</sup> University of Cape Town (ZA)

<sup>4</sup> DESY & Bonn University

<sup>5</sup> Deutsches Elektronen-Synchrotron (DESY)

**Corresponding Author:** sara.ruiz.daza@cern.ch

The ATLAS Strip Tracker for HL-LHC consists of individual modules that host silicon sensors and front-end electronics. The modules are then mounted on carbon-fiber substructures hosting up to 14 modules per side. An End-of-Substructure (EoS) card connects up to 28 data lines to the lpGBT and VL+ ASICs that provide data serialization and 10 GBit/s optical data transmission to the off-detector systems respectively. The EoS is powered by a dedicated Dual-Stage DC-DC converter. With the EoS now moving into production we report on first experiences from production and also give a few lessons learned during the project duration.

**Summary (500 words):**

The silicon tracker of the ATLAS experiment will be upgraded for the upcoming High-Luminosity Upgrade of the LHC (HL-LHC). The main building blocks of the new strip tracker are modules that consist of silicon sensors and hybrid PCBs hosting the read-out ASICs. The modules are mounted on rigid carbon-fiber substructures, known as staves in the central barrel region and petals in the end-cap regions, that provide common services to all the modules. At the end of each stave or petal side, a so-called End-of-Substructure (EoS) card facilitates the transfer of data, power, and control signals between the modules and the off-detector systems. The module front-end electronics transfer data to the EoS card on 640 MBit/s differential lines. The EoS connects up to 28 data lines to one or two lpGBT chips that provide data serialization and uses a 10 GBit/s versatile optical link (VL+) to transmit signals to the off-detector systems. The lpGBT also recovers the LHC clock on the downlink and generates clock and control signals for the modules. To meet the tight integration requirements in the detector, several different EoS card designs are needed. Custom-made holders and clamps are produced to guide cables and optical fibers as well as to shield the sensors from the opto-electric system. The power to the EoS is provided by a dedicated dual-stage DC-DC package providing 2.5 and 1.2 V to the EoS cards. As the EoS card and its DC-DC-Stage have recently moved towards production, we will report on the first production experiences, results from the large-scale QC (quality control) and some design validation (QA) results. We will also report on the “lessons learned” during the duration of this project.

**Tuesday posters session / 76**

## **Performance profiling and design choices of an RDMA implementation using FPGA devices**

**Author:** Alexander Oh<sup>1</sup>

<sup>1</sup> *University of Manchester (GB)*

**Corresponding Authors:** matei.vasile@cern.ch, alexander.oh@cern.ch

RDMA communication is an efficient choice for many applications, such as data acquisition systems, data center networking and any other networking application where high bandwidth and low latency are necessary. RDMA can be implemented using a large array of options which need to be tailored to the needed use case in order to get optimal results. Aspects such as the effects of using multiple simultaneous connections, using various transport functions such as RDMA Write and RDMA Send and communication models such as sending individual bursts or continuous streams of data will be investigated for implementing RDMA on FPGA devices.

### **Summary (500 words):**

Starting with LHC Run3, the FELIX (Front-End Link eXchange) system is used for implementing the data acquisition system of a small number of ATLAS subdetectors, and from LHC Run4 onward, FELIX is planned to become the data acquisition system used by all ATLAS subdetectors. The FELIX system is based on a custom FPGA board which receives data from the front-end detector electronics via optical links and outputs data via a PCIe interface to a host computer which manages processing and relaying the data further to the readout system. The host uses the RDMA (Remote Direct Memory Access) support offered by network interface cards with RoCE (RDMA over Converged Ethernet) support to transmit data further towards the readout systems over Ethernet.

Taking into account the foreseen increase in data rate which will happen as a consequence of the High Luminosity LHC upgrade, a possible improvement of the FELIX system was proposed. This improvement would avoid the potential bottleneck of the PCIe interface and of the FELIX PC CPU by implementing RDMA support in the FELIX FPGA itself, thus removing the FELIX PC itself from the data path of the readout system. The data would now be flowing directly from the FELIX board to the Software ROD PCs in the server farm.

This proposed FPGA implementation of RDMA was demonstrated both outside FELIX (TWEPP2021) and with a modified version of FELIX (TWEPP2022). This showed that the FPGA RDMA implementation can reach the expected performance of an RDMA link.

To make this FPGA RDMA implementation useful in a production setting, a number of issues need to be explored, understood and handled:

First, there is the issue of multiple simultaneous connections between the FPGA board running the

RDMA implementation and multiple potential receivers. There is the matter of how many simultaneous connections can be handled, and what will be their effect on the operation of the FPGA device and the RDMA link(s).

Then, there is the issue of the RDMA transport function being used. RDMA Send is similar to how TCP/IP sockets work, offer easy to use streaming of RDMA messages but it involves both endpoints of an RDMA link, which can lead to higher overhead and latency. This is what is currently in use with FELIX software and Software ROD. RDMA Write needs a pre-allocated memory region on the receiver, can, theoretically, lead to higher bandwidth and lower latency, but, on the other hand, it will require some memory management mechanism to make sure that data is not lost when the memory region becomes full. Several approaches for the implementation of this mechanism for Software ROD will be investigated.

Finally, the existing demonstrator was working with bursts of data. But in a production environment data will need to be streamed continuously from the FPGA board to the receiver(s). This will need to be investigated to see how the throughput varies depending on time, incoming data rate or trigger frequency, especially in the context of the issue described in the previous paragraph.

## Programmable Logic, Design and Verification Tools and Methods / 78

### FLX-182, the hardware platform for ATLAS readout during High Luminosity LHC

**Author:** Alexander Oh<sup>1</sup>

<sup>1</sup> *University of Manchester (GB)*

**Corresponding Authors:** nikolina.ilic@cern.ch, alexander.oh@cern.ch

FLX-182 is a PCIe card designed for the readout system of the ATLAS experiment for the High Luminosity phase of LHC starting in 2029. FLX-182 is responsible for decoding and transferring data from the front-ends into the host server memory, and receiving and distributing timing, trigger and control information. About six hundred FLX-182 will sustain 4.6 TB/s of total throughput at 1 MHz data rate. FLX-182 is equipped with a Xilinx Versal Prime VM1802 SoC, a PCIe Gen4x16 interface and can operate up to 24 optical links at 25 Gb/s. FLX-182 runs firmware capable of interfacing with all different subdetectors.

#### **Summary (500 words):**

The FELIX readout system has been added to the data acquisition system of the ATLAS experiment at the LHC in the data-taking period called Run3 (2021-2025) and serves at present a subset of the ATLAS sub-detectors.

An evolved version of FELIX, dubbed Phase-II, will be deployed in Run 4 (2029 –2032) and will serve all ATLAS subdetectors. FELIX Phase-II will sustain a data rate (1 MHz) ten times higher than that of Run 3 and a total throughput of 4.6 TB/s. The entire system will comprise about 300 servers, each equipped with custom PCIe FELIX cards and 400 GbE network interfaces. In addition to performing high-throughput and low-latency readout, FELIX will distribute to/from the detector front-ends timing, trigger and control (TTC) information, as well as monitoring and configuration. Multiple direct-memory-access buffers on the host will permit the separation of different streams in the FELIX software and firmware.

At the core of the FELIX system is the custom PCIe card. The Phase-II FELIX card is called FLX-182 and is equipped with a Xilinx Versal Prime VM1802 SoC, a PCIe Gen4x16 interface and 24 optical links that operate at a speed up to 25 Gb/s. Four additional 25 Gb/s links allow to communicate with the TTC system, or, alternatively, to implement a 100 GbE interface. A flash memory is used to store firmware images.

A few firmware variants have been developed to support the different communication protocols adopted by sub-detectors as well as specific features. Communication protocols include lpGBT and GBT, used by the lpGBT [1] and GBTX [2] radiation-hard ASICs for front-end electronics, as well as simpler 8b10 or Interlaken encoding for FPGA-to-FPGA communication. FLX-182 prototypes have been built and are

undergoing integration tests. Quality-check software run on the SoC has been developed, while readout software is under development.

[1] <http://lpgbt-fpga.web.cern.ch>

[2] <https://espace.cern.ch/GBT-Project>

Tuesday posters session / 79

## Status of the MDT Trigger Processor for the ATLAS Level-0 Muon Trigger at the HL-LHC

**Author:** Alexander Oh<sup>1</sup>

<sup>1</sup> *University of Manchester (GB)*

**Corresponding Authors:** [rimsky.alejandro.rojas@cern.ch](mailto:rimsky.alejandro.rojas@cern.ch), [alexander.oh@cern.ch](mailto:alexander.oh@cern.ch)

The MDT Trigger Processor (MDTTP) is a key ATLAS Level-0 Muon trigger upgrade component designed to meet High-Luminosity LHC requirements. The MDTTP will use MDT hits in the trigger for the first in ATLAS to improve the momentum resolution of muon candidates provided by RPC and TGC detectors and reduce fake muon trigger rate.

The MDTTP hardware is based on the Apollo ATCA platform. The pre-production prototype includes a VU13P-FPGA, high-speed FireFly optical transceivers, peripherals, and other improvements learned from using the previous hardware demonstrator. We present the prototype status, firmware implementation, core algorithm, slow-control software, and first integration tests.

### Summary (500 words):

The first-level muon trigger (L0Muon) of the ATLAS experiment will be upgraded to operate in the substantially increased luminosity environment of the HL-LHC. The moderate spatial resolution of RPC and TGC trigger chambers limits the selectivity of the current system. The Monitored Drift Tube (MDT) chambers, currently used for offline precision tracking, will be included in the trigger to improve the transverse momentum resolution and reduce the rate of fake muon triggers.

Hit data with moderate spatial resolution from RPC or TGC are used to determine muon candidates at the Sector Logic. These candidates define regions of interest for the MDT trigger processor (MDTTP) to process MDT hits matching the regions in space and time. Those hits are used to form track segments, which are combined to determine the transverse momentum. The MDTTP will also reject low-quality sector logic candidates for which no MDT track segments could be found.

According to simulation studies, the MDTTP is expected to reduce the L0Muon output trigger rate by up to 70%, while keeping the efficiency plateau at 95% for a single muon trigger with a threshold of 20 GeV.

The MDTTP will be implemented using the open-source platform Apollo. An Apollo ATCA blade is comprised of two PCB modules called Service Module (SM) and Command Module (CM). The SM, common to all Apollo applications, provides the required ATCA Intelligent Platform Management Controller (IPMC), power entry and conditioning, a powerful system-on-module (SoM) computer, and flexible clock and communications infrastructure. The application-specific CM provides the processing FPGA, the FireFly transceivers for communication with the other systems inside ATLAS, and a few peripherals.

A pre-production prototype of the MDT trigger processor CM has been produced and is currently under test, featuring one large Xilinx VU13P FPGA and eight 12-channel bidirectional optical transceiver modules, with a link speed up to 25 Gbps. The prototype is based on the first test results of the hardware demonstrator.

In addition to the trigger processing tasks, the MDTTP will also be responsible for configuring and monitoring the MDT Chamber Service Module (CSM) and transmitting MDT hit information to the FELIX system when a L0 acceptance signal is received.

The MDTTP firmware is designed to have a fixed latency of approximately  $1.7\mu\text{s}$  and is divided into Hardware Abstraction Layer (HAL) and User Logic (UL). The HAL firmware implements the low-level interface to Sector Logic, CSM, SM, and FELIX, providing control and data to the UL at 320MHz clock frequency. Results of the first tests interfacing CSM, SM, and FELIX are presented. The UL firmware implements the trigger, data acquisition, control, and monitoring logic. While a reduced version of the firmware has been tested on the demonstrator board with the KU15 FPGA, a full version is currently being implemented targeting the VU13P FPGA. The design fits well in the chosen FPGA, satisfying the latency constraint. The status of the slow control software running on the SM and the integration into the ATLAS Detector Control System infrastructure are also presented.

**Tuesday posters session / 80**

## Upgrade of the ATLAS Level-0 TGC Endcap Muon Trigger

**Author:** Alexander Oh<sup>1</sup>

<sup>1</sup> *University of Manchester (GB)*

**Corresponding Authors:** [chihiro.kawamoto@cern.ch](mailto:chihiro.kawamoto@cern.ch), [alexander.oh@cern.ch](mailto:alexander.oh@cern.ch)

The status of the development of the Level-0 endcap muon trigger system for the ATLAS experiment at the HL-LHC is presented. Integrations of the new trigger algorithms and the implementation with firmware on a new prototype of the trigger board (Sector Logic, SL) are also presented. Results from hardware tests of the SL prototype board and integration tests with the newly developed front-end board are also shown.

**Summary (500 words):**

HL-LHC is planned to start its operations in 2029 with more than 3 times the instantaneous luminosity of the LHC Run 3. To cope with the proton-proton collision rate higher than that of LHC, the trigger and readout system of the ATLAS experiment needs to be replaced. The new Level-0 muon trigger system is required to reconstruct muon candidates with an improved momentum resolution to suppress the trigger rate with keeping the efficiency. That can be achieved by combining the signals from various subdetectors (InnerCoincidence): Resistive Plate Chamber (RPC), Thin Gap Chamber (TGC), New Small Wheel (NSW), Monitored Drift Tube (MDT), and scintillator-steel hadronic calorimeters (TileCal) to form more offline-like tracks.

The Sector Logic (SL) boards play a key role in the new Level-0 muon trigger system. The full system includes 80 SL boards, covering pseudorapidity ( $\eta$ ) range  $|\eta| < 2.4$ . They receive the hit data of RPCs (barrel,  $|\eta| < 1.05$ ) and TGCs (endcap,  $1.05 < |\eta| < 2.4$ ) from the on-detector electronics and reconstruct muon candidates. The signals from NSW and TileCal are combined with the information of the muon candidates reconstructed in RPCs and TGCs to suppress fake trigger from non-collision particles. The selected muon candidates are transferred to the boards dedicated to processing of the MDT hits, where further selection is applied with improved momentum resolution. The SL boards also serve as the readout boards of the RPC and TGC hit data.

Each SL board is designed as an ATCA blade, integrated with Virtex UltraScale+ XCVU13P FPGA, Mercury XU5 MPSoC mezzanine card, and CERN-developed IPMC. FireFly modules provide 120 pairs of transmitters and receivers. Clock is managed with Si5345 chips and fixed latency scheme is employed. Power is supported up to 350 W. The first prototype (attachment 1) of the SL board was produced in Oct. 2021. All the functions of the hardware were demonstrated and confirmed after minor modifications from the first prototype. We are finalizing the design according to these results, and also preparing a test environment utilizing the MPSoC on the board.

The trigger firmware is supposed to be implemented on XCVU13P FPGA. Integration of the algorithms for the track segment reconstruction using TGC hits, InnerCoincidence and track selection is accomplished with realistic resource usage of  $\sim 40\%$  and acceptable total latency of  $\sim 500$  ns.

The performance of the trigger algorithms is evaluated with single muon MC samples overlaid with the pile-up events expected in the possible highest luminosity of HL-LHC ( $\mu=200$ ), and also verified with



a bit-wise simulator.

## Trigger and Timing Distribution / 81

### A full-function Global Common Module (GCM) prototype for ATLAS Phase-II upgrade

Author: Alexander Oh<sup>1</sup>

<sup>1</sup> University of Manchester (GB)

Corresponding Authors: weiming.qian@stfc.ac.uk, alexander.oh@cern.ch

The baseline architecture for the ATLAS Phase-II upgrade has a single-level hardware trigger (Level-0 Trigger) with a maximum rate of 1 MHz and 10  $\mu$ s latency. A full-function Global Common Module (GCM) prototype has been designed and implemented for the core part of the Level-0 Trigger, the Global Trigger. This GCM features two of the latest Adaptive Compute Acceleration Platform (ACAP) devices from Xilinx, the Versal Premium VP1802, plus twenty 12-channel 25.7 Gb/s FireFly optical engines. Presented here is the design process of this full-function GCM prototype hardware, with the focus on the technology choices and simulation results.

#### Summary (500 words):

The High Luminosity Large Hadron Collider (HL-LHC), an upgrade of the LHC, is scheduled to be operational from 2029. It aims to achieve instantaneous luminosities of a factor 5–7.5 larger than the LHC nominal value, thereby enabling physicists to study known mechanisms, such as the Higgs boson, in greater detail, and potentially observe rare new phenomena. However, realizing the physics potential of this much higher luminosity requires an increase in the bandwidth of data processed by ATLAS of an order of magnitude. This presents significant challenges to the design of the Trigger and Data Acquisition systems. A baseline architecture, based on a single-level hardware trigger (Level-0 Trigger) with a maximum rate of 1 MHz and 10  $\mu$ s latency, has been proposed for the ATLAS Phase-II upgrade to meet these challenges. The Level-0 Trigger includes a brand-new subsystem, the Global Trigger, which performs algorithms similar to those used offline at Phase-I (such as Topoclustering) on full-granularity calorimeter data.

The Global Trigger architecture is divided into three layers: the Multiplexer Processor (MUX) layer, the Global Event Processor (GEP) layer, and the Global to Central Trigger Processor interface (gCTPi). The MUX layer collects data from detectors (calorimeter and muon) and legacy Feature Extractor modules, time-multiplexes them bunch-crossing by bunch-crossing and sends full events to the GEP layer in a round-robin fashion. Each GEP node in the GEP layer receives the full event data pertaining to a particular bunch-crossing, executes complex algorithms, and sends the results to the gCTPi, which comprises a single node that selects and resynchronises the results from all GEP nodes before sending them to the CTP.

A common hardware approach has been taken in the Global Trigger to simplify its system design and long-term maintenance, and a full-function Global Common Module (GCM) prototype has been designed and implemented to fulfil the functionalities of MUX, GEP and gCTPi with different firmware loads. Recent firmware study shows that the programmable logic resource requirement of the GEP node is beyond that of the Ultrascale+ device XCVU13P used on previous demonstrators. This GCM prototype features two Xilinx Versal Premium ACAP VP1802, which has double the density of the XCVU13P and includes an integrated SoC with a completely new architecture. All the high-speed I/Os on the GCM are handled with twenty 12-channel 25.7 Gb/s FireFly optical engines. The Global system design has been optimised to limit the GCM power consumption to a maximum of 400 W, which fits within ATLAS ATCA shelf cooling capability. Power design, high-speed signal design and thermal design are the three biggest challenges that the GCM hardware development is faced with. A 26-layer PCB with low-loss material, vias in pads and backdrill technologies has been used for this GCM board. Extensive PCB simulation and thermal simulation have been undertaken to guide its layout design to ensure power integrity, signal integrity and thermal performance.

This talk presents the design process of this full function GCM prototype hardware with the focus on the technology choices and simulation results.

**Thursday posters session / 82****The phase-1 upgrade of the ATLAS level-1 calorimeter trigger****Author:** Alexander Oh<sup>1</sup>**Co-author:** Tigran Mkrtchyan<sup>2</sup><sup>1</sup> *University of Manchester (GB)*<sup>2</sup> *Heidelberg University (DE)***Corresponding Authors:** tigran.mkrtchyan@cern.ch, alexander.oh@cern.ch

The ATLAS level-1 calorimeter trigger is a custom-built hardware system that identifies events containing calorimeter-based physics objects, including electrons, photons, taus, jets, and missing transverse energy. In Run 3, L1Calo has been upgraded to process higher granularity input data. The new trigger, currently running in parallel with the legacy system, comprises several FPGA-based feature extractor modules, which process the new digital information from the calorimeters and execute more sophisticated trigger algorithms. The design of the system will be presented along with an analysis of the improved performance of the upgrade in the increasingly challenging Run-3 LHC pile-up environment.

**Summary (500 words):**

The ATLAS Level-1 Calorimeter provides the bulk of the hardware trigger objects used to make the ATLAS level-1 trigger decision. Being based on information from both the electromagnetic and hadronic layers of the detector, it can identify potential electron, photon, tau and jet candidates, as well as making a partial missing transverse energy assessment. The original design, using over 7000 analogue inputs of coarse granularity calorimeter information, was very successful in the first 10 years of LHC operation, which already provided luminosities beyond design.

However, the expected higher luminosities in future LHC operation will compromise the efficacy of the original hardware, and so an upgrade of the system has been built and installed during the recent LHC shutdown period. The basis of the improvement was to increase the level of detail of information available to the trigger, with more granular information both in longitudinal position, and calorimeter depth. In particular this allows more sophisticated algorithms to be used based on shower shapes, while also aiding energy resolution in a higher pile-up environment.

The higher data rate needed to transmit this additional information (approximately a factor of 10 in the electromagnetic layer) necessitated the use of a new digital trigger signal path which is integrated into the calorimeter outputs, replacing the old analogue path with digital signals transferred on optical links. The algorithmic part of the Level-1 processing is performed on three Feature Extractors (FEX), which specialize in identifying different physics signatures.

The electron feature extractor (eFEX) processes the full granularity information in order to find smaller physics object showers, using the full depth and spatial information to better distinguish, and reject, the dominant jet background. It consists of 24 individual ATCA-based modules running entirely independently and in parallel in order to handle smaller blocks of the central detector coverage. The jet feature extractor (jFEX) does not require the full granular information, and so consists of only 6 similar modules, assessing jet-like objects with a greater flexibility than the original

system for making regional corrections for pile-up effects. They also provide a missing energy measurement. The global feature extractor (gFEX) is a single module processing data from the whole detector at a coarser granularity, also identifying jets and measuring missing energy but, being a single module, has the capability to make full event-level corrections.

The results from these FEX modules are further assessed by a new topological trigger system, which can apply flexible algorithms from simple multiplicity counting up to complex multiple object based topological algorithms. These modules provide readout data via a new custom ROD module and the ATLAS upgrade standard FELIX readout mechanism. This data is required both to validate and monitor the performance of the trigger, and as a seeding mechanism for the ATLAS High Level Trigger.

The trigger is being switched over in stages from legacy to upgrade during 2023, as validation of the correct functioning of the new system is completed. Results on the rates and performance of the upgrade trigger will be presented.

## Production, Testing and Reliability / 84

# Reliability of Power Conversion Card for CMS MTD-BTL

**Author:** Tomasz Gadek<sup>1</sup>

**Co-authors:** Guenther Dissertori<sup>1</sup>; Krzysztof Stachon<sup>1</sup>; Ulrike Grossner<sup>2</sup>; Werner Lustermaun<sup>1</sup>

<sup>1</sup> *ETH Zurich (CH)*

<sup>2</sup> *ETH Zurich*

**Corresponding Author:** tomasz.gadek@cern.ch

The Minimum Ionizing Particle (MIP) Timing Detector (MTD) is introduced in the CMS experiment to measure the time of MIPs. The MTD consists of 432 Readout Units (RUs) in its barrel region (BTL), each powered by two Power Conversion Cards (PCC). PCCs host three radiation and magnetic field tolerant DC-DC converters. More than 1,000 PCCs will be produced to satisfy the assembly needs of BTL with sufficient margins. A reliability study has been conducted on a prototype batch of 80 cards to demonstrate the design and assembly robustness for up to 20 years of operation in BTL's conditions.

### Summary (500 words):

The High Luminosity Large Hadron Collider (HL-LHC) will deliver up to 200 proton-proton interactions per bunch crossing. Interaction points are spread out over a period of  $\sim 190$  ps. With an initial timing resolution of 30-40 ps, the new Minimum Ionizing Particle (MIP) Timing Detector (MTD) will measure the time of MIPs, improving identification and event reconstruction capabilities of the CMS experiment in the increased pile-up conditions. The functional building block of MTD's Barrel Timing Layer (BTL), called Readout Unit (RU), is powered by two Power Conversion Cards (PCC). Design of BTL utilizes 864 PCCs and production plans reach 1,100 units.

The PCCs will operate in a static magnetic field of 3.8 T, while being cooled with liquid CO<sub>2</sub> at -35°C. Estimated radiation levels reach a fluence of  $1.90 \times 10^{14}$  neq/cm<sup>2</sup> and a total dose of  $\sim 32$  kGy. Being a single layer sub-detector, BTL requires high reliability of its components. The reliability goal for PCCs allows for 0.5% failures in 20 years of operation. The forecasted mission profile of the detector assumes at maximum 10 thermal cycles per year of operation including warm runs at +10°C.

A set of 80 PCCs has been produced and tested with a yield of 92.5%. Among defected cards, three had minor and non-critical defects that were easily repairable, one card had a critical failure that was

repairable, and two had critical defects with unidentified root causes. All cards underwent 20 passive thermal cycles between  $-35^{\circ}\text{C}$  and  $+75^{\circ}\text{C}$  and were re-tested yielding identical results. A reliability demonstration test has been performed on 96 DC-DC converters (32 cards) with a 95% confidence level. The test lasted for 1245 thermal cycles with specimen range of temperatures between  $-30^{\circ}\text{C}$  and  $+83^{\circ}\text{C}$ . The cards have been stressed and monitored under different load and powering conditions according to the Design of Experiment principles.

The design of PCC has matured to a production ready state, offering a compact and reliable DC-DC converter solution for high energy physics. 80 cards were produced and assembled according to the production stage design. In this contribution the reliability demonstration test results will be presented together with the plans for the environmental stress screening procedure envisaged for the full-scale production phase of the project.

**Module, PCB and Component Design / 85**

## **The Trigger & Data Acquisition interface module of the Tile Calorimeter for the ATLAS Phase- II Upgrade**

**Author:** Tigran Mkrtchyan<sup>1</sup>

<sup>1</sup> *Heidelberg University (DE)*

**Corresponding Author:** tigran.mkrtyan@cern.ch

For the High Luminosity-Large Hadron Collider (HL-LHC) phase, the ATLAS Tile Calorimeter (Tile-Cal) is undergoing a major upgrade with a complete redesign of the on- and off-detector electronics. In the new readout architecture, the calorimeter signals are digitised every 25 ns directly on-detector and transferred to the off-detector Tile PreProcessor (TilePPr) via high-speed optical links. The TilePPr reconstructs the energies from the digitised samples and transfers them through its Trigger & Data Acquisition interface (TDAQi) module to the ATLAS Trigger & DAQ system via fixed and deterministic high-speed optical links at speeds of 11.2 Gbps.

**Summary (500 words):**

The High Luminosity-Large Hadron Collider (HL-LHC) is a planned upgrade that will increase the instantaneous luminosity by a factor of 5 larger than the LHC's nominal value. To overcome the challenges imposed by the HL-LHC environment and to adapt to the new ATLAS readout architecture, the ATLAS Tile Calorimeter (TileCal) is undergoing a major upgrade with a complete redesign of the on- and off-detector electronics.

In the new readout architecture, the calorimeter signals are digitised every 25 ns directly on-detector and transferred to the off-detector Tile PreProcessor (TilePPr) via high-speed optical links. The TilePPr reconstructs the cell energies from the digitised samples, performs the energy calibration and transfers them to the ATLAS Trigger & DAQ system, all within strict latency requirements.

Within the TilePPr, system, the Tile Trigger & DAQ interface (Tile TDAQi) module receives the reconstructed cell energies and applies summing, sorting and grouping algorithms to build trigger primitives at a rate of 40 MHz. The formatting of the trigger primitives is tailored to the requirements of the various trigger sub-systems of ATLAS.

One of the biggest challenges is the latency minimisation for each step of the processing implementation in the TDAQi. High optimisation is required for delivering the trigger inputs to the electron/photon and jet trigger systems (L0Calo), the muon-based trigger system (L0Muon) and to the ATLAS Global Trigger system.

The TDAQi is an FPGA-based Advanced Telecommunications Computing Architecture (ATCA) Rear Transition Module (RTM), operating under the ATCA framework. Consisting of a 14-layer PCB, the TDAQi is equipped with over 70 high-speed transceivers which operate at speeds up to 11.2 Gbps.

An overview of the TileCal electronics upgrade is given along with the latest implementation of the TDAQi prototype. The recent hardware and integration tests results are discussed as well as the next steps.

## Thursday posters session / 86

## Performance of a novel charge sensor on the ion detection for the development of a high-pressure avalancheless ion TPC

**Authors:** Dongliang Zhang<sup>1</sup>; Hulin Wang<sup>None</sup>; Kai Chen<sup>2</sup>; Tianyu Liang<sup>2</sup>

**Co-authors:** Feng Liu<sup>2</sup>; Jun Liu<sup>1</sup>; Le Xiao; Ling Liu<sup>2</sup>; Yichen Yang<sup>3</sup>; bihui you; chaosong gao; xiangming sun<sup>2</sup>

<sup>1</sup> Central China Normal University CCNU (CN)

<sup>2</sup> Central China Normal University

<sup>3</sup> Institute of modern physics, Chinese Academy of Sciences

**Corresponding Author:** tianu.liang@mails.ccnu.edu.cn

We will report the performance of Topmetal-S chip, a charge sensor specifically designed to directly sense ions for the high-pressure ion TPC of  $N\nu$ DEX experiment for neutrinoless double-beta decay search. The signal waveforms were investigated with various experiments and chip configurations. The equivalent noise charge of Topmetal-S is measured to be  $120 e^-$ . Different ions species, both with negative or positive charges, could be detected by the sensor. The mobilities of majority ion charge carriers are measured for negative (positive) species in air and  $SF_6$  respectively. The expected precision of the drift distance reconstruction using different velocities of ion species are discussed for  $N\nu$ DEX experiment.

### Summary (500 words):

**The chip.** Topmetal-S is a chip designed for  $N\nu$ DEX experiment, the goal of which is to search for the neutrinoless double beta decay signal of Se-82 using high-pressure gaseous TPC. The choice of using  $SF_6$  as the working gas means ion drift detection. The topmetal technique, thanks to its low noise, makes this possible while keeping high energy resolution. The chip now is in its second version and the test results look promising.

The classic single-end folded cascode structure is used in the chip. The bias voltages could be provided either from the internal DAC or from the external voltage sources. The discharge is controlled by an nMOS. The routing of each bias is surrounded by the shielded metal layers just as the coaxial-cable to reduce the interference.

**The waveform.** Due to the small drift velocity, the waveform of the ion signal should be long enough. In the chip design, the decay time could be adjusted by tuning the bias voltage of the discharge nMOS. The rise time could be tuned in the range from 0.08 to 3.3 ms, and the falling time in the range from 8 ms to 1.6 s, making it also work for high rate events.

**The ENC.** The equivalent noise charge is measured using a test pulse injected from the guard ring, and it's found to be 120e. The dynamic range of the chip is 400 - 52000e. And it shows good linearity in this range. The ENC is also constant in this range. As a cross-check, an external capacitor is connected to the topmetal and by injecting reversed pulse from the external capacitor we can verify the capacitance of the guard ring.

**Ion drift.** A small TPC is used to test the ion drift detection both in Air and Argon. A  $^{241}Am$  alpha source is placed on the side of the field cage to provide the ions. With the drift E field from 200 to 800 V/cm, both positively and negatively charged ions in air are detected. Using a scintillator to provide the ionization time, the drift velocity of positively charged Argon ion is measured in the various pressures in the range 1-3 AMT. The measured mobilities are consistent with the numbers in literature.

**Impact to the experiment.** The successful ion detection and good energy resolution provide a proof-of-the-concept for the  $N\nu$ DEX experiment. Further development of the chip is ongoing. In the next version, a module providing network readout will be added. And further tests using the chip to measure the mobility of the  $SF_6$  gas are planned. Multiple species of the ions provide a unique way to measure the Z coordinate of the decay position, which is important to verify the 3D tracking capability for the  $N\nu$ DEX experiment.

Thanks to the good energy resolution and ion detection, we can foresee that there are wide applications for this type of chip, although the chip is not suitable for very high-rate events.

**Production, Testing and Reliability / 87****Reliability Run and Data Analysis of the Accelerated Aging of Present and Future Electrolytic Capacitors Installed in the Protection Systems of Superconducting Magnets of the Large Hadron Collider at CERN****Authors:** David Carrillo<sup>1</sup>; Enrique De Nicolas Lumbreras<sup>1</sup>; Josep Guasch Martinez<sup>1</sup>**Co-authors:** Edward Nowak<sup>1</sup>; Erik Hildre Bjorkhaug<sup>1</sup>; Felix Rodriguez Mateos<sup>1</sup>; Mirko Pojer<sup>1</sup><sup>1</sup> CERN**Corresponding Author:** josep.guasch.martinez@cern.ch

This study evaluates the lifetime and aging process of the aluminium electrolytic capacitors to be used in the new protection systems of the High Luminosity LHC superconducting magnets. The accelerated testing and analysis of several groups of capacitors aged for more than one year provided insights into their expected lifespan and aging process. The results obtained have practical implications for maintenance and replacement schedules, as well as for selection and acceptance of capacitors for new Heater Discharge power Supplies (HDS) equipment. The knowledge gained from this study ensures the safety and reliability of the LHC and its electronic components.

**Summary (500 words):**

The Large Hadron Collider (LHC) at CERN is a long-term scientific project that requires periodic, preventive, and corrective maintenance of its electronic components. Among these components, aluminium electrolytic capacitors are an essential part of the protection systems of the high-field superconducting magnets being developed for the HL (High Luminosity) LHC project. More than 36,000 of these capacitors, rated for 500 V and 4.7 mF, are installed in the LHC tunnel and are operational since the collider's start-up phases in 2007. Failure of these capacitors could cause significant damage to the superconducting magnets, delaying operation and running into very costly repairs, which is why it is crucial to evaluate their lifetime and aging process.

To achieve this, representative samples from the global population were aged in test beds and ovens, enabling the accelerated evaluation of their lifespan. Regular measurements of capacitance, equivalent series resistance, leakage current, and weight -to calculate electrolyte loss- were conducted throughout the aging process to evaluate the capacitors' performance. The conclusive results obtained from the analysis of several groups of capacitors aged at 85°C and 70°C for more than one year indicated that aging processes are consistent, and the results provide valuable insights into the capacitors' expected lifetime.

The knowledge gained from the lifetime studies of a subset of capacitor after LHC runs 1 and 2 has been applied to qualify different candidates for the new production of Heater Discharge power Supplies (HDS) equipment to be installed for the HL-LHC, including a new family rated for 105 °C. After careful consideration, a candidate was chosen, and a few capacitors from the distinct production batches received were put to age for one year. The results obtained from the analysis of these batches allow for the extrapolation of their reliability and electrical behaviour throughout their expected lifetime.

The findings of this study have practical implications for the maintenance and replacement of the LHC's and HL-LHC electronic components. By understanding the capacitors' aging process, it is possible to identify which variables are better indicators for final use evolution across different families and manufacturers, and provide an expected margin of error given the input data used.

In conclusion, this study provides a comprehensive analysis of the aging process of the aluminium electrolytic capacitors to be used in the new HL-LHC protection systems for high-field superconducting magnets. The accelerated testing and evaluation of the capacitors' performance provided valuable insights into their aging process and expected lifetime, and allows for more confident selection and preliminary evaluation of new candidates for similar use cases ensuring the safety and reliability of the

LHC.

Tuesday posters session / 88

## Design of the OBELIX monolithic CMOS pixel sensor for an upgrade of the Belle II vertex detector

Author: Thanh Hung Pham<sup>1</sup>

<sup>1</sup> Centre National de la Recherche Scientifique (FR) - Université de Strasbourg

Corresponding Author: thanh.hung.pham@cern.ch

The Belle II collaboration has initiated a program to upgrade its detector in order to address the challenges set by the increase of the SuperKEKB collider luminosity, targeting  $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ . A monolithic CMOS pixel sensor named OBELIX (Optimized BELLe II pIXel) is proposed to equip 5 detection layers upgrading the current vertex detector. Based on the existing TJ-Monopix2, OBELIX is currently designed in a CMOS 180 nm process. This new sensor introduces an extended pixel matrix, power regulators, fast hitOR information as inputs to the trigger system and a powerful readout logic matching the Belle II requirements.

### Summary (500 words):

The Belle II experiment aims to collect data from the SuperKEKB collider located in Japan, at very high instantaneous luminosity, up to  $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ . Beam conditions required at such luminosities generate large and continuous rate of background particles and sets strong challenges to the vertex detector, for which Belle II has initiated an upgrade program. The VTX project proposes to use a depleted monolithic pixel sensor for this upgrade, the OBELIX chip, in order to reach excellent granularity in space (pitch below  $40 \mu\text{m}$ ) and time (integration below 100 ns).

The sensor occupies an area of about  $19 \times 30 \text{ mm}^2$  and includes a  $464 \times 896$  pixel array with  $33.04 \times 33.04 \mu\text{m}^2$  pixel pitch, as well as peripheral circuitry for power regulation, bias generation, digital control and data processing. The OBELIX pixel matrix scheme remains identical to TJ-Monopix2, which was originally developed for the ATLAS inner tracker, in order to benefit from the detection performance already assessed [Bespín, 2022]. Besides the fired pixel address, the column-drain readout provides 50 ns timing precision (relaxed from the original 25 ns) with 7 bits of arrival time and 7 bits of ToT.

The main differences between OBELIX and TJ-Monopix2 lies in the chip periphery with new powering scheme and digital processing.

To reduce the non-active area and the large number of side pads dedicated to power distribution of the matrix, as well as to facilitate the power cabling to sensors, a distributed low-dropout regulator is implemented, requiring only 5 groups of power pads per matrix side.

The new digital processing consists of four parts: Trigger Logic Unit (TLU), Transmission Unit (TXU), Synchronisation unit (SCU) and Control Unit (CTU). The TLU implementation allows to handle a maximum hit rate of  $120 \text{ MHz/cm}^2$  with a 30 kHz trigger rate and  $10 \mu\text{s}$  trigger latency. Data from 4 double columns are merged via a round-robin arbiter before being sent to a two-stage buffer. The first stage of the buffer is a FIFO and acts as a pre-memory whose size allows it to hold the event information between two triggers. The second stage is the main trigger memory, where its logic allows to associate hit data and trigger information before sending them to the TXU. The TXU frames the data with 8b/10b encoding and sends it to the 320 MHz serial LVDS output. The SCU and CTU inherit from the TJ-Monopix2 design. They conform to the RD53 interface and guaranty the control and configuration of different sensor parameters.

The overall chip is designed so that the power consumption is less than  $200 \text{ mW/cm}^2$  at an average 60 MHz hit rate and with 50 ns time-stamping.

This presentation will review the overall design of the OBELIX sensor, which is scheduled for submission in Q4 2023. We will specifically focus on the new features introduced over the TJ-Monopix2 prototype and on the design methodology approaching digital-on-top flow..

Bespín, C. (2022). Charge collection and efficiency measurements of the TJ-Monopix2 DMAPS in 180 nm CMOS technology. Pixel2022. Santa Fe, New Mexico, USA: Proceeding of Science.

Thursday posters session / 89

## Development of the data transmission architecture of the stitched sensor prototype towards the ALICE ITS3 upgrade

**Author:** Piotr Andrzej Dorosz<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** piotr.dorosz@cern.ch

The ALICE experiment at the CERN LHC will replace the three innermost layers of the Inner Tracker System (ITS) with an innovative vertexing detector. A single-die stitched monolithic pixel detector of 1.8 cm x 26 cm designed in 65 nm CMOS imaging technology will be used to build these layers. The data communication is done via the 1.8 cm edge of the detector. This contribution will focus on the architecture, challenges and techniques used to aggregate and send off chip up to 46 Gb/s of data flux.

### Summary (500 words):

The prototype single-die stitched monolithic pixel detector of 1.8 cm x 26 cm designed in 65 nm CMOS imaging technology is the second iteration of the stitched sensor for ALICE Inner Tracker System and will be submitted in 2024. The chip has two endcaps and a repeating frame which is replicated 12 times to fill the 26 cm length. Each repeating frame is subdivided into six independent sensor units. Each sensor unit can be considered as a self-contained pixel detector, with its own power domain, pixel matrix, biasing, slow control and readout unit. This segmentation granularity allows to switch off each sensor unit independently in case of manufacturing defects.

The data communication is done only through the left endcap (Fig. 1), which can be considered as a self-contained architecture within the stitched sensor design. The endcap receives data from all sensor units and sends it off-chip. Every sensor unit is connected to it with an independent on-chip data line. There are 144 data lines toggling at maximum 320 Mbit/s per line. The 144 on-chip data transmitters are distributed along the detector and generate a total data flux of 46.08 Gb/s. This data flux is aggregated and encoded in the endcap and sent off-chip via six 10.24 Gb/s high-speed serializers. The lpGBT-link protocol is used as a transport layer. The protocol itself increases the demand for the off-chip communication bandwidth. The requirement comes from the lpGBT encoding logic that contains cyclic redundancy check (CRC) and forward error correction (FEC). The use of high-speed serializers is necessary to meet the bandwidth requirements and to cope with a limited number of pads allocated to off-chip data transmission on the 1.8 cm edge of the detector.

The distance between each sensor unit and the endcap varies along the 26 cm sensor length. To maintain the logic levels of transmitted data, rebuffering has to be implemented at least twice per each repeated frame. The buffers are adding jitter to the signal which makes up to 3.6 ns for the longest data line leaving only 40% of the eye opening. The different line lengths make the phase of the data vary from around 1 ns to several dozen nanosecond. This variation depends on the data line length, number of rebuffering stages, voltage and temperature. The adopted solution to account for the jitter and phase delay is to implement a phase aligner per data line, that tracks the correct phase and samples the data in the middle of the eye opening.

This contribution discusses the techniques and solutions, including simulation and implementation details, adopted during the development of the left endcap architecture to address the challenges of aggregating a total of 46.08 Gb/s of data on 144 on-chip data lines with varying phase and jitter of each line. It also presents how the data is encoded and sent off-chip via six 10.24 Gb/s serializers to meet the data bandwidth requirements.

Tuesday posters session / 90



## 28 nm front-end channels for the readout of pixel sensors in future high-rate applications

**Author:** Luigi Gaioni<sup>1</sup>

**Co-authors:** Andrea Galliani<sup>1</sup>; Lodovico Ratti<sup>2</sup>; Valerio Re<sup>3</sup>; Gianluca Traversi<sup>4</sup>

<sup>1</sup> *University of Bergamo and INFN Pavia (IT)*

<sup>2</sup> *University of Pavia*

<sup>3</sup> *INFN*

<sup>4</sup> *University of Bergamo*

**Corresponding Author:** luigi.gaioni@unibg.it

This work is concerned with the design and the characterization of front-end channels, developed in a 28 nm CMOS technology, conceived for the readout of pixel sensors in future, high-rate applications at the next generation of large particle accelerators.

Two front-end architectures are discussed. In the first one, an in-pixel flash ADC is exploited for the digitization of the signal, whereas the second one features a Time-over-Threshold (ToT) conversion. A prototype including the ADC-based front-end has been submitted and the characterization of the chip is discussed in the conference paper. Simulation results relevant to the ToT-based architecture are reported.

### Summary (500 words):

State-of-the-art readout channels for pixel detectors in high energy physics (HEP) experiments are being developed, in a 65 nm CMOS technology, by the RD53 collaboration, established at CERN in 2013. The RD53 efforts led to the submission of three families of readout chips optimized for the high luminosity (HL) upgrades of the ATLAS and CMS experiments. The RD53 chips have been extensively characterized, and proved to be able to withstand total ionizing doses (TIDs) up to 1 Grad(SiO<sub>2</sub>), while preserving the main performance parameters.

The HEP designers' community is now generally migrating to the 28 nm process for the development of new circuits. The 28 nm node is the major commercial successor of the 65 nm one, bringing along some interesting features. In particular, a number of test campaigns with TIDs in the Grad regime did show that properly sized 28 nm transistors can be operated with limited performance losses. Moreover, the scaling-down process intrinsically improves speed and density of digital circuits, allowing the designers to develop very compact pixel cells and fast readout logic and I/O circuits. This makes the 28 nm technology an ideal candidate for the design of next generation, high data rate readout chips to be operated in extremely harsh radiation environments.

This work discusses the design of two front-end circuits being developed in the framework of the INFN Falaphel project, aiming at the integration of silicon photonics modulators with high speed, rad-hard electronics in a 28 nm CMOS technology. The Falaphel project was conceived having in mind the challenging requirements set by the tracker of the hadronic Future Circular Collider. Nonetheless, the outcome of the project can be of interest for a potential replacement of the innermost pixel layers of the HL-LHC experiments after 2030.

The two architectures described in this work implement different digitization techniques. The first one relies on an in-pixel flash ADC, whereas the second one leverages the Time-over-Threshold method. Both the front-end channels include a charge sensitive amplifier (CSA) with detector leakage compensation. The CSA feedback includes two independent loops. A fast one, featuring a MOS device operated as a constant current source, provides a linear discharge of the CSA feedback capacitance. A slow loop was instead devised to compensate for the sensor leakage current. In the flash ADC-based channel, a set of three autozeroed comparators are connected to the preamplifier, providing a 2-bit resolution analog-to-digital conversion. On the other hand, in the ToT-based processor, the comparator is DC coupled to the CSA, and a digital counter is activated by the signal generated at the discriminator output.

A prototype including a matrix of 8x4 ADC-based channels has been submitted and the characterization of the chip will be discussed in the conference paper. Simulation results relevant to the ToT-based architecture, whose submission is foreseen for October 2023, will be reported.

## CMS ECAL Upgrade Front End card. Design and performance.

**Authors:** Alexander Singovski<sup>1</sup>; Alexandre Dolgoplov<sup>1</sup>; Colin Jessop<sup>1</sup>; Giacomo Cucciati<sup>1</sup>; Marc Dejardin<sup>2</sup>; Nikitas Loukas<sup>1</sup>; Tomasz Gadek<sup>3</sup>; Werner Luster<sup>3</sup>

<sup>1</sup> *University of Notre Dame (US)*

<sup>2</sup> *Université Paris-Saclay (FR)*

<sup>3</sup> *ETH Zurich (CH)*

**Corresponding Author:** alexander.singovski@cern.ch

Upgraded version of the CMS electromagnetic calorimeter (ECAL) Front-End (FE) card is designed to provide the lossless data streaming and reliable control and synchronization of the on-detector Very-Front-End (VFE) units.

The initial card design, validated in the beam tests in 2018-2019, was significantly modified to support the fast and reliable access to the VFE cards components for initialization, calibration and optimization of the data flow. Details of this updated design, performance of the final version of the card as well as the quality control and quality assurance plane for the mass production stage will be discussed.

### Summary (500 words):

The CMS ECAL detector readout unit is the Readout Tower: matrix of 5x5 calorimeter cells signals from which are digitized by five Very-Front-End cards, each serving five cells. One Front-End card collect data from five VFE cards and send via fast optical links off-detector to the Barrel Calorimeter Processor (BCP).

The calorimeter cell signal is digitized by the custom ASIC (CATIA) on the VFE board by 12-bit ADC at 160MHz sampling rate. The high sampling rate is required by the design time resolution. The data from one cell can be transmitted by one e-link at 1.28Gb/s rate thanks to the lossless data compression implemented by the custom data transmission and concentration ASIC (LiteDTU). 25 data e-links are handled by four CERN custom gigabit transceivers (lpGBT).

One of lpGBTs is working in transmitter mode (Master) to provide clock distribution and control functions, while three others –in receiver only mode (Slaves).

Both data conversion ASICs, CATIA and LiteDTU are quiet fancy devices with multiple functions like special calibration and test regimes, data alignment etc. and require significant slow control resources for initialization, calibration, and control via custom I2C interfaces. The limited slow control capacity of the Master lpGBT is not sufficient for 25 readout channels, hence slow control functions of Slave lpGBTs are also used. In addition, CERN custom GBT-SCA ASIC is used to extend the ADC and GPIO capabilities.

The initial design of the FE card with I2C control via Master-Slave I2C chain, although functioning well, was too slow for the ECAL application. That led to the Readout Tower initialization time of more than 10 minutes.

The final design of the slow control chain includes the Master-Slave lpGBT communication via fast EC link and Master lpGBT –GBT-SCA communication via EC link simulation by up- and down- e-links.

Details of the FE card design and final performance evaluated via system test of the full ECAL readout chain: VFE-FE-BCP in the laboratory conditions at the beam tests will be presented.

The quality assurance (QA) and quality control (QC) of the FE cards during the mass production will be performed via several procedures:

☒ Short ageing of all produced cards in the Oven followed by the full functional test at the custom Test Stand

☒ Long ageing of randomly selected fraction of cards to the about full life cycle of the boards

☒ Irradiation in the hadron beam a small randomly selected set of cards followed by the full functional test

Details of the testing procedure and QA/QC procedures will be presented.

## Model and analysis of the data readout architecture for the ITS3 ALICE Inner Tracker System

**Author:** Manuel Viqueira Rodriguez<sup>1</sup>

<sup>1</sup> *Universidad Politecnica de Madrid (ES)*

**Corresponding Author:** manuel.viqueira.rodriguez@cern.ch

The ALICE collaboration is developing the new Inner Tracker System 3 (ITS3), a novel detector that exploits the stitching technique to construct single-die monolithic pixel sensors of up-to 266 mm x 93 mm. ITS3 requires all hits from a particle flux of 4.4 MHz/cm<sup>2</sup> to be transmitted on-chip to one of the sensor edges. This on-chip readout is limited by a power budget of 20 mW/cm<sup>2</sup>, a readout inefficiency of  $<2.5 \times 10^{-3}$  and  $\leq 10\%$  dead area. The model of ITS3 on-chip readout architecture will be presented, used to optimize the data flow implementation limited by physical and power budget constraints.

### Summary (500 words):

The ALICE collaboration is developing the Inner Tracker System 3 (ITS3), a new detector that aims to replace the three innermost layers of the tracking system during LHC's Long Shutdown 3. The detector consists of three cylindrical layers, with each half-cylinder made of a single-die monolithic pixel sensor bent towards the beam pipe. They are developed using a commercial 65 nm CMOS Imaging technology with dimensions up-to 266 mm x 93 mm. This can be achieved by profiting from the stitching technique, which allows the manufacturing of modular chips larger than the design reticle.

The expected Pb-Pb interaction rate is 100 kHz, which generates a particle flux in the innermost layer of 4.4 MHz/cm<sup>2</sup>. With a pixel pitch of  $\sim 20 \mu\text{m}$ , up to 4 pixels per incident particle are hit, yielding an occupancy of  $8 \times 10^{-4}$ . The shipment of these hits follows a continuous trigger-less solution, where all hits detected during a pre-defined integration period of 2  $\mu\text{s}$ , 5  $\mu\text{s}$ , or 10  $\mu\text{s}$  are read together in frame packets. If the number of pixel hits during the integration period is too high, the readout frame is assembled incomplete. The fraction of incomplete frames define the performance of the readout architecture. This readout architecture must achieve a fraction of incomplete frames below  $2.5 \times 10^{-3}$ , a power density below 20 mW/cm<sup>2</sup>, and a dead area lower than 10%.

To optimize the readout architecture and buffer sizes, a behavioral model was designed in System Verilog. This module emulates the components and requirements of the ITS3 readout. Each ITS3 sensor is composed of independent Stitched Units. These Stitched Units are made abutting 12 Repeated Sensor Units (RSU), and 2 end-caps (Figure 1). The RSUs contain the sensitive area of the chip. Each RSU contains 12 power units with independent readout architectures. These readout architectures read in parallel different regions of the sensitive area into on-chip memories to cope with particle fluctuations (Figure 2). The hits stored in these memories are sent in frame packets to the left end-cap, which hosts the only off-chip data connection. The model was tested using random data and physics data extracted from LHC behavior. This data takes into consideration the centrality of the collisions, the pile-up of different collisions in one integration period, the QED electrons generated from electromagnetic interactions, and different cluster sizes.

This submission will explain in detail the methodology, results, and learnings obtained from using the model. The optimized Stitched Unit requires 144 links of 160 Mbit/s, 432 on-chip memories with 15-bit width, and 128-word depth. Apart from these definitions, this study provides key learnings for the readout architecture implementation such as the correlation between losses and collisions pile-up, or the best ordering for reading the memories inside the power units.

Tuesday posters session / 94

## Radiation Tolerance Tests for SFP+ Transceivers

**Authors:** Akira Taniike<sup>1</sup>; Arisa Wada<sup>2</sup>; Atsuhiko Ochi<sup>1</sup>; Daisuke Hashimoto<sup>2</sup>; Erika Yamashita<sup>3</sup>; Haruka Asada<sup>2</sup>; Makoto Tomoto<sup>4</sup>; Masaya Ishino<sup>3</sup>; Ren Nagasaka<sup>3</sup>; Takumi Aoki<sup>3</sup>; Yasuyuki Horii<sup>2</sup>; Yasuyuki Okumura<sup>3</sup>; Yoshifumi

Narukawa<sup>3</sup>; Yuki Mitsumori<sup>2</sup>; Yuya Ohsumi<sup>2</sup>

<sup>1</sup> *Kobe University (JP)*

<sup>2</sup> *Nagoya University (JP)*

<sup>3</sup> *University of Tokyo (JP)*

<sup>4</sup> *High Energy Accelerator Research Organization (JP)*

**Corresponding Author:** dhashimoto@hepl.phys.nagoya-u.ac.jp

Results are presented for gamma and neutron irradiation tests for SFP+ transceivers. The radiation tolerance of the electronics components used in the detector area is a key of the electronics systems at high energy physics experiments. We tested four types of SFP+ transceivers from Ficer. Gamma rays were irradiated up to O(100) Gy at the Cobalt-60 facility of Nagoya University. Neutrons were irradiated up to O( $10^{12}$ ) cm<sup>-2</sup> using the tandem accelerator at Kobe University. The results can be referred to in selecting the SFP+ transceivers for high energy physics experiments.

**Summary (500 words):**

The radiation tolerance of the electronics components used in the detector area is a key of the electronics systems at the LHC experiments. For example, the total ionising dose and the 1-MeV neutron equivalent flux estimated for the frontend electronics of the thin gap chamber of the ATLAS experiment are 14 Gy and  $4 \times 10^{11}$  cm<sup>-2</sup> for an integrated luminosity of 4000 fb<sup>-1</sup>.

We tested four types of SFP+ transceivers from Ficer: FSPP-H7-M85-X3D, FSPP-H7-M85-X3Di, FSPP-H7-M85-X3DM, and FSPP-H7-M85-X3DMi. Different data transfer rates and temperature ranges are supported by these types of SFP+. The performances of the SFP+ transceivers were tested by measuring the light intensity from the transmitter and the bit error ratio (BER) during the loopback data transfer. The light intensity was measured using Photom MiNi 211B from Graytechnos. The BER was measured using the integrated bit error ratio tester from Xilinx with KC705 evaluation kit. The transfer rates employed for the BER measurements were 2.56 Gbps, 8.0 Gbps, and 10.24 Gbps. A reference clock of 160 MHz was used for all the transfer rates.

Gamma rays were irradiated up to O(100) Gy at the Cobalt-60 facility of Nagoya University. A dedicated electronics board was prepared for supplying power to the SFP+ transceivers during the gamma ray irradiation.

Neutrons were irradiated up to O( $10^{12}$ ) cm<sup>-2</sup> using the tandem accelerator at Kobe University. The neutrons were produced from a beryllium target bombarded with deuterons with the energy in the range 2.6-2.8 MeV depending on the operation period. The produced neutrons have an energy distribution with the peak at around 2 MeV. Non-ionising energy loss was targeted to be studied, and thus no power was supplied to the SFP+ transceivers during the neutron irradiation.

A positive result was obtained for the use in the thin gap chamber electronics of the ATLAS experiment at HL-LHC. The result can be referred to in selecting the SFP+ transceivers for high energy physics experiments.

## System Design, Description and Operation / 95

### A readout system based on SiPM for the dRICH detector at the EIC

**Author:** Luigi Pio Rignanes<sup>1</sup>

<sup>1</sup> *INFN-BO*

**Corresponding Author:** rignanes@bo.infn.it

The ePIC experiment at the future Electron-Ion Collider aims to use silicon photomultipliers as the photodetector technology for the dual-radiator ring-imaging Cherenkov detector (d-RICH). Despite

their advantages for this low light application in high magnetic fields, SiPMs are sensitive to radiation and require rigorous testing to ensure that their single-photon counting capabilities and dark count rate are kept under control over the years. The presented results show the successful use of a complete prototype readout chain based on the ALCOR chip for SiPM characterization measurements and test-beam measurements using the d-RICH prototype.

#### Summary (500 words):

Silicon Photomultipliers (SiPMs) are the main candidates for instrumenting the optical readout of the dual-radiator ring-imaging Cherenkov detector (d-RICH) for the particle identification of the ePIC experiment at the Brookhaven National Laboratory. In this talk we will present a full detector prototype made by coupling several vendors SiPMs with an ASIC based readout. The 32 channels ASIC, called ALCOR developed by INFN Torino, includes a regulated common-gate transimpedance amplifier frontend and 4 TDCs per channel allowing both single-photon counting and Time-over-Threshold modes, with a time resolution of 50 ps and an event rate capability of up to 5 MHz per channel. It works in a triggerless configuration, meaning that the ASIC produces a continuous stream of data that is then acquired by the data acquisition with a maximum rate of 300 kHz per channel for 300 thousands channels in the configuration of the final detector.

SiPMs represent the best solution in this low light application thanks to the high photodetection efficiency and insensitivity to magnetic fields (1 T for the d-RICH in ePIC). However, the detector will be placed in a radioactive environment with an expected dose for the entire life of the experiment of  $10^{11}$  1-MeV neq/cm<sup>2</sup>. Radiation damages, for the expected dose, result in an increase of the dark current, reflected by an increase in the Dark Count Rate (DCR) of a factor 10000. This affects the single-photon counting capability due to pileup and readout saturation. To reduce the DCR, sensors are cooled to -30° C, which lowers it by a factor of  $\approx 20$  with respect to room temperature. The behaviour of  $\approx 200$  irradiated sensors was studied by exposing  $3 \times 3$  mm<sup>2</sup> SiPMs from different vendors and cell sizes to increasing doses of radiation. The Hamamatsu S13650-50 SiPM was found to have the lowest brand new and after irradiation DCR, but it still reaches  $\approx 10$  MHz at  $10^{11}$  1-MeV neq/cm<sup>2</sup> at -30° C, which is beyond the capacity of the front-end ASIC and DAQ data rate. One can find in literature that by heating up the sensors it's possible to induce an annealing of the radiation induced defects leading to a reduction of the DCR. Thus, we studied two annealing methods to partially recover the DCR performance: an oven annealing at 150° C and direct/reverse current annealing at 175° C. Both the methods lead to DCR reduction of a factor 100, with the oven reaching it after 200 hours while the current annealing takes 1/10 of the time. A clear advantage of the latter is in the possibility to perform in-situ annealing without dismantling the detector.

Four sensor matrices irradiated up to  $10^{10}$  neq/cm<sup>2</sup> that underwent the oven annealing were integrated in the d-RICH prototype and tested at CERN PS. The detector can acquire Cherenkov rings within a 10 ns time window reaching a time resolution of 350 ps. After showing the results of this test beam, the new design of the prototype towards the implementation of the final detector integration will be shown.

#### Tuesday posters session / 96

## A prototype 4D-tracking demonstrator based on the TimeSPOT developments.

**Authors:** Adriano Lai<sup>1</sup>; Alberto Stabile<sup>2</sup>; Alessandro Cardini<sup>3</sup>; Andrea Lampis<sup>1</sup>; Angelo Loi<sup>None</sup>; Davide Brundu<sup>1</sup>; Gian Matteo Cossu<sup>4</sup>; Giovanni Passaleva<sup>5</sup>; Lorenzo Piccolo<sup>None</sup>; Lucio Anderlini<sup>6</sup>; Matt Addison<sup>7</sup>; Michela Garau<sup>1</sup>; Michele Veltri<sup>6</sup>; Sandro Cadeddu<sup>1</sup>; Valentino Liberali<sup>8</sup>

<sup>1</sup> *Universita e INFN, Cagliari (IT)*

<sup>2</sup> *Università degli studi di Milano*

<sup>3</sup> *INFN Cagliari, Italy*

<sup>4</sup> *INFN, Cagliari (IT)*

<sup>5</sup> *INFN Florence (IT)*

<sup>6</sup> *Universita e INFN, Firenze (IT)*

<sup>7</sup> *University of Manchester (GB)*

<sup>8</sup> *Università degli Studi di Milano*

**Corresponding Authors:** angelo.loi@cern.ch, adriano.lai@ca.infn.it, angelo.loi@ca.infn.it

We present first results obtained with a prototype 4D-tracking demonstrator, using sensors and electronics developed within the TimeSPOT project, and tested on a positive charged pion beam at CERN SPS. The setup consists of six small tracking layers in a row, having area of about 3 mm squared each, three of which equipped with 3D-trench silicon sensors and three with 3D-column diamond sensors. The six layers are then read-out by a KC705 Xilinx board on a PC. We describe the demonstrator structure and operation and illustrate results on its tracking capabilities.

**Summary (500 words):**

The TimeSPOT 4D-tracking demonstrator has been tested on a positive charged 180 GeV/c pion beam at CERN SPS. The tracking setup consists of up to six small sensing layers in a row, having area of about 3 mm squared each. Three of the layers are equipped with 3D-trench silicon sensors and three with 3D-column diamond sensors. In previous tests, TimeSPOT 3D-trench pixels have been demonstrated being capable of an intrinsic time resolution below 10 ps, while 3D-column diamond pixels have intrinsic resolution below 80 ps.

The tracking layers are matrices of 32x32 pixels with 55  $\mu\text{m}$  pitch, hybridized with and read-out by the Timespot1 ASIC, implemented in CMOS 28-nm technology. The hybrids are assembled on stations, based on dedicated PCBs. Each of the 1024 pixels of the ASIC integrate one fast Analog Front End and one high-time-resolution TDC. The TDC is capable of a time resolution of 20 ps rms, while the AFE has about 60 ps rms in average, with a spread in performance from about 20 ps to 100 ps, due to a well-known design problem in the offset compensation technique of the discriminator.

The six stations are configured using an I2C interface. Data link are output using LVDS cables (8 cables of 1.28 Gbps each per each layer). All the links are sent to a data-concentrating board (named Mezzanine), which is plugged on a KC705 Xilinx board. The Xilinx board formats and temporarily stores data on internal registers. Data are finally readout on a PC using an Ethernet protocol. The system clocks are distributed by one COTS clock-managing Si5341 board from Silicon Labs, configurable by means of an I2C interface.

In order to help the beam-alignment procedure, two mono-pixel layers are placed at the beginning and at the end of the tracking row. The mono-pixels can be read-out by dedicated single channel analog boards and an oscilloscope, acquired during the alignment procedure, before data-taking. The tracking stations are mounted on movable mechanical supports on an orientable rail, whose angle in the plane where the stations are placed can be adjusted to match the beam direction. All the stations are placed inside a metal box, which acts as an EMI shield. The DAQ system and the clock distributor Si5341 PCB are placed outside the same metal box. Pictures of the demonstrator can be found in the attachment files.

After beam alignment, data have been acquired and analyzed concerning the timing and tracking performance of the system. First results are presented in the paper.

**Thursday posters session / 98**

## **Data acquisition system of the PANDA Micro-Vertex Detector (MVD)**

**Authors:** Michele Caselle<sup>1</sup>; Olena Manzhura<sup>2</sup>

**Co-authors:** Andreas Kopmann<sup>2</sup>; Daniela Calvo<sup>3</sup>; Fabio Cossio<sup>4</sup>; Francesca Lenta<sup>5</sup>; Gianni Mazza<sup>6</sup>; Hans-Georg Zaunick<sup>7</sup>; Jürgen Becker<sup>2</sup>; Kai Lukas Unger<sup>2</sup>; Kai-Thomas Brinkmann<sup>7</sup>; Lukas Tomasek<sup>8</sup>; Pavel Stanek<sup>8</sup>; Peter Marvin<sup>7</sup>; Timo Dritschler<sup>2</sup>; Tobias Stockmanns<sup>9</sup>; Tröll Nils<sup>7</sup>; Vladimir Sidorenko<sup>2</sup>

<sup>1</sup> KIT - Karlsruhe Institute of Technology (DE)

<sup>2</sup> KIT - Karlsruhe Institute of Technology (DE)

<sup>3</sup> Istituto Nazionale di Fisica Nucleare, Sezione di Torino (IT)

<sup>4</sup> INFN Torino (IT)

<sup>5</sup> Politecnico di Torino (IT) and Istituto Nazionale di Fisica Nucleare, Sezione di Torino (IT)

<sup>6</sup> Universita e INFN Torino (IT)

<sup>7</sup> Justus-Liebig-Universitaet Giessen (DE)

<sup>8</sup> *Czech Technical University in Prague (CZ)*

<sup>9</sup> *Jülich Forschungszentrum (DE)*

**Corresponding Author:** olena.manzhura@kit.edu

The Micro Vertex Detector is a key component of the PANDA experiment at FAIR. This contribution focuses on the development of the Module Data Concentrator (MDC) ASIC for the configuration, time distribution and readout of the silicon microstrip subdetector system of the PANDA Micro-Vertex Detector (MVD). A first version of the MDC architecture has been developed on FPGA and integrated with the microstrip sensor and the front-end ASIC. The detector module has been integrated into the DAQ framework. The overall description of the MDC and the data acquisition system is presented and the first test results are discussed.

#### Summary (500 words):

The PANDA (antiProton ANnihilation at DArmstadt) experiment will study the strong interaction in annihilation reactions between an antiproton beam and a stationary cluster jet target. The detector will comprise different sub-detectors for tracking, particle identification and calorimetry. The Micro-Vertex Detector (MVD) is the innermost part of the tracking system and is designed for precise tracking and detection of secondary vertices. It is equipped with silicon pixel and strip sensors and custom front-end electronics. For the readout of the double-sided silicon strip sensors, an ASIC called ToAst (Torino Asic for Strip readout) is being developed in 0.11  $\mu\text{m}$  CMOS technology by INFN Turin. The ASIC employs the Time-over-Threshold (ToT) technique for digitization and provides the Time of Arrival (ToA) of the crossing particle with a time resolution given by the clock frequency. To sustain the readout of the double-sided microstrip detector, a Module Data Concentrator (MDC) ASIC is under development at KIT. It will multiplex and process the data stream from the ToAst front-end and send it to back-end electronics, so called MVD Multiplexer Board (MMB). Up to 8 ToAst front-end chips of one detector module are controlled and read out by one MDC. The MMB board is under development at KIT, it will collect and process the data coming from several MDC chips and transfer the results via multiple optical links to the computing nodes for global event building. The second prototype of the ToAst ASIC with 64 active channels has been produced by UMC. This ToAst chip has been integrated with the FPGA implementation of the MDC to form the first fully functional detector module. Beam tests have been performed at COSY (Cooler Synchrotron) facility located at Jülich. This paper focuses on the design of MDC ASIC and MMB board, the integration with the ToAst and sensor and the first preliminary test results.

#### Tuesday posters session / 99

## Prototype of a 10.24Gbps Data Serializer and Wireline Transmitter for the readout of the ALICE ITS3 detector.

**Author:** Vladimir Gromov<sup>1</sup>

**Co-authors:** Arseniy Vitkovskiy<sup>2</sup>; Marcel Rossewij<sup>3</sup>; Noa Aarts<sup>3</sup>

<sup>1</sup> *Nikhef National institute for subatomic physics (NL)*

<sup>2</sup> *Nikhef ( the Dutch National Institute for Subatomic Physics )*

<sup>3</sup> *Utrecht University*

**Corresponding Authors:** arseniy.vitkovskiy@cern.ch, vgromov@nikhef.nl, m.j.rossewij@uu.nl, a.vitkovskiy@nikhef.nl

A new silicon tracker detector (ITS3) will be installed in ALICE Inner Tracking System during the LHC long shutdown 3. We develop a 10.24Gbps Data Serializer and Wireline Transmitter (GWT-PSI) circuit for the readout of the detector. A 16-to-1 multiplexer architecture achieves low power consumption (28mW) and avoids high-frequency (> 640MHz) clock signals in the circuit. A clock-cleaning PLL and power-supply cleaning LDO will be built into the circuit making it immune to the noisy operation environment. A prototype has been submitted in the ER1 production run in the TPSCo 65nm ISC CMOS imaging technology.

**Summary (500 words):**

The ITS3 detector will comprise 6 stitched wafer-scale chips (280 mm long). Each chip is a pixelized Monolithic Active Pixel Sensor (MAPS). 6 high-speed data transmission links will be implemented per chip to read out up to 46Gb/s per chip. The data transmission link serializer will convert multi-bit data packets into a single-bit stream for the transmission over a wireline cable.

Currently, we are designing a serializer adapted to the operating conditions of the ITS3 detector. This version abbreviated as GWT-PSI (Gigabit Wireline Transmitter Power Supply Immune) will run at 10.24Gbps data rate. The ITS3 requires that the GWT-PSI circuit will operate connected to the noisy (chip-level) power supply bus.

To mitigate the power supply noise effect a low-dropout regulator (LDO) circuit has been included in the GWT-PSI block. The LDO circuit is an external-capacitor-less type regulator generating stable and fluctuation-free output voltage to power critical blocks. The LDO provides a -50 dB PSRR (power supply rejection ratio) at low frequency (<1MHz) with the deterioration to a -32dB level at the worst point at the frequency of 110MHz. The LDO consumes only 0.74mW of power.

For reliable operation of a 10.24Gbps serializer a low-time-jitter (rms  $\approx$  6ps) clock signal is required. No such quality reference clock will be provided in the ITS3. That is why we included a PLL (phase-locked loop) circuit in the GWT-PSI. The PLL (charge pump topology with an RC ring-oscillator VCO) generates a 640MHz clean output clock. The power consumption of the PLL is 1.6mW (1.2V x 1.3mA).

The GWT-PSI consists of a digital core and an analog core. The digital core includes a dual port asynchronous FIFO needed to transfer 32-bit data packets from a 320MHz noisy clock domain into 16-bit output packets to a 640MHz clean clock domain. The output data packet is stored in an 8-bit register driven by the positive edge of the clock and an 8-bit register driven by the negative edge of the clock. In the analog core, a 16-phase round-robin multiplexer is used to transmit the data from the registers to the inputs of the line driver bit-by-bit in an interleaved manner. A multi-phase delay-locked loop (DLL) generates 16 phases evenly spaced (97ps) in the period (1.56ns) of a 640MHz clock. The edge-combiner block converts the phase signals into the selection signals for the multiplexer.

We use a voltage-mode source-series terminated (SST) differential line driver to transmit large swing ( $\pm 0.6V$ ) signals over a 100 $\Omega$  cable. The power of the line driver is 7.2mW (6mA x 1.2V)

This work reports on the prototypes submitted in the ER1 production run, which include the analog core block of the GWT-PSI, the PLL circuit and the LDO circuit. A dedicated measurement system has been developed for testing radiation effects on the circuits. The experimental results from the first test might become available at the time of the workshop and will be included.

ASIC / 100

## Performance of H2GCROC3, the readout ASIC of SiPMs for the back hadronic sections of the CMS High Granularity Calorimeter.

**Author:** Jose David Gonzalez Martinez<sup>1</sup>

<sup>1</sup> OMEGA (FR)

**Corresponding Author:** jose.david.gonzalez.martinez@cern.ch

H2GCROC is the 130nm CMOS ASIC designed to read out the SiPMs coupled to the scintillating tiles of the back hadronic sections of CMS HGAL (High Granularity Calorimeter). Each of its 72 channels is composed of a current conveyor, a high-gain preamplifier, a shaper, and ADC to read the energy, with two discriminators connected to TDCs for time-of-arrival and time-over-threshold information, respectively. This work presents the ASIC architecture and its characterization in lab and test beam, proving good adaptability in calibration, radiation tolerance, capacity to measure SiPM SPS (single-photon-spectrum), MIP's time and energy with high resolution.

**Summary (500 words):**

H2GCROC is a radiation-hardened 130 nm CMOS chip developed by OMEGA, AGH, CEA, and CERN to read the energy and time of the SiPM-on-tile detectors of CMS HGAL. It has 78 channels and dissipates 15 mW per channel.

Each channel contains a current conveyor, a low-noise preamplifier, and a shaper connected to a 10-bit



40 MHz SAR-ADC, allowing charge measurement over the preamplifier's linear range. A discriminator and a TDC provide charge information from time-over-threshold (ToT) over a 200 ns dynamic range in the preamplifier's saturation zone. Additionally, a fast discriminator and TDC produce timing information with an accuracy of 25 ps. The ASIC uses a DRAM memory to store charge and timing data and performs the data processing to select and compress the meaningful data to send. It is configurable with an I2C protocol for slow control and fast commands at 320 MHz.

The main challenge in the design of this ASIC was on the adaptability to read the MIP signal with a high dynamic range of charge measurement (160 fC to 320 pC) and at the same time be able to calibrate and quantify the SiPM-on-tile performance using the SPS (single-photon-spectrum) technique without sacrificing a lot in precision and time resolution. Furthermore, the ASIC needs to have a good radiation tolerance and be able to compensate for the SiPM radiation damage during the entire lifetime of HGCAL. The tiles of HGCAL will use different sizes of SiPM up to 9mm<sup>2</sup>. Therefore, the design and calibration process considered the effects of capacitance, rising, and falling time of different SiPM sensors.

The gain of each block of the Front-end design can be calibrated for the MIP to have good linearity and to adapt to the dynamic range. In addition, the channel's dispersion can be compensated with internal DACs considering the breakdown voltage variations of SiPMs, temperature changes, and production tolerances. Also, the ASIC includes a calibration circuit that injects up to 200 pC of charge internally into each channel.

The chip was extensively tested in the lab and test beam and has proved its good performance in fulfilling the requirements for reading the SiPM-on-tile of HGCAL. This work examines the ASIC front-end design and its performance with different SiPM detectors. After full calibration, two chip configurations are proposed, one for in-situ calibration after installation of HGCAL and a configuration for HGCAL operation.

The two plots attached to this summary prove in Figure 1 the capability of the ASIC to perform SPS measurements, whereas Figure 2 displays the energy and time-of-arrival (ToA) measurements for small charge injection. The tests performed with the third fabricated version of the ASIC are encouraging. Only minor corrections will be needed for the final version to be ready for the CMS experiment.

**Thursday posters session / 101**

## A Radiation Hardened IP Development Programme for 28nm CMOS Technology

**Authors:** Alex Steven<sup>None</sup>; Alicja Michalowska-Forsyth<sup>None</sup>; Mark Lyndon Prydderch<sup>1</sup>; Oliver Bowett<sup>None</sup>; Stephen Bell<sup>2</sup>; Thomas Gardiner<sup>None</sup>

<sup>1</sup> *Science and Technology Facilities Council STFC (GB)*

<sup>2</sup> *Science and Technology Facilities Council*

**Corresponding Authors:** thomas.gardiner@stfc.ac.uk, oliver.bowett@stfc.ac.uk, stephen.bell@stfc.ac.uk

The ASIC Design Group at RAL has commenced a three-year programme developing radiation-hardened 28nm circuits intended to provide verified building blocks for future projects. The aim of this programme is to complement and add to the CERN common IP library for 28nm. Our programme includes a range of utility circuits such as high precision amplifiers, a low power 12bit ADC for housekeeping, bandgaps, reference drivers, DACs, a 1Gbps Serializer for low-complexity read-out, and more. To explore the benefits of the 28nm technology, a high-resolution LGAD front-end including a 20ps resolution TDC is also under development.

### Summary (500 words):

We will present the programme and the expected performance of completed 28nm circuits scheduled to be fabricated in October 2023.

28nm CMOS is a key technology for designing operational ASICs for future experiments in HL-LHC, this is due to the need of superior radiation tolerance in comparison to older technologies. The ASIC Design Group at Rutherford Appleton Laboratory has commenced a three-year programme developing radiation-hardened 28nm circuits intended to provide verified building blocks for future projects. Target radiation hardness for these circuits is 1Grad Total Ionization Dose (TID).

The aim of this programme is to complement and add to the CERN common IP library for 28nm CMOS. The CERN common IP library has specification standards for our IP to be accepted; this operational

process-voltage-temperature variations, limited transistor flavours and maximum number of routing layers. All our designed IP has this requirement built into the specification.

Our programme includes a range of utility circuits such as high precision amplifiers, a low power 12bit ADC for housekeeping, bandgaps, reference drivers, DACs, a 1Gbps Serializer for low-complexity read-out, and more. To explore the benefits of the 28nm technology, a high-resolution LGAD front-end including a 20ps resolution TDC is also under development.

This submission will present the goals and milestones of the programme and highlight the completed 28nm circuits which are designed to be radiation hardened and meet the CERN common IP library requirements.

**Thursday posters session / 102**

## **Digital processing and BLMASIC control prototype for the Beam Loss Monitor system in the SPS at CERN.**

**Author:** Mathieu Saccani<sup>1</sup>

**Co-authors:** Christos Zamantzas<sup>1</sup>; Ewald Effinger<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** mathieu.saccani@cern.ch

The Beam Loss Monitoring system plays a crucial role in the CERN's Super Proton Synchrotron beam monitoring and machine protection. With the upcoming renovation of the system, the acquisition electronics can be based on an innovative ASIC designed by CERN. This paper presents the development of the control and digital processing electronics for this BLMASIC, reviews the architecture and design choices, discusses implementation details, including the controls and redundancy schemes, and highlights some preliminary results. The conclusion outlines the future development steps, and emphasises the interest of this simple and robust architecture using LpGBT and VTRx for critical systems.

**Summary (500 words):**

**Introduction:**

This study presents the development of a prototype for the control and digital processing electronics of the BLMASIC for the renovation of the Beam Loss Monitoring (BLM) system of the Super Proton Synchrotron (SPS) during the LHC Long Shutdown 3 (LS3) at CERN.

**Background:**

The current BLM system has already had several decades of successful operation in beam monitoring and machine protection. As spare components are becoming rare and obsolete, a complete renovation is planned during LHC Long Shutdown 3 (LS3). The new specification of the system meets both the SPS and LHC needs, as the same hardware will be deployed at the LHC during LS4. Enhanced capabilities of this newly designed system will include 1 kGy radiation tolerant electronics, 8-order dynamic range, 10  $\mu$ s acquisition period and flexible real-time digital processing.

**BLMASIC overview:**

The core of the new acquisition electronics of the future BLM SPS system can be the BLMASIC. This current measurement ASIC, developed by CERN, is the result of a choice between two versions: ADC delta-sigma and current-frequency conversion. The characterisation of the two topologies is described, and the radiation tests of the selected version are detailed.

**Remote control:**

The BLMASIC control and processing electronics are based on the standard VFC-HD platform of CERN's Beam Instrumentation (BI). This backend VME platform uses remote configuration capabilities via optical links and local I2C links to control the acquisition electronics placed in the tunnel. The remote control of the 4 BLMASICs via 2 LpGBTs and 2 VTRxs is explained. Redundancy in the system is also discussed, including the selection of the active link and the recovery sequence in case of link failure.

**Digital processing:**

The digital electronics architecture and FPGA-based implementation used in the prototype, including the implementation of running sums, raw data buffers and threshold comparison, are discussed in this section. Several improvements are also proposed for the development of the final operational system.

**Prototype testing:**

The prototype BLMASIC digital processing and control electronics was tested in the laboratory with a current source and installed in the SPS in 2023. Some preliminary results are presented in this section. Measurements with beam should provide valuable data for further analysis.

**Future implementation:**

This section presents the complete picture of the new system, including the detectors, the acquisition and processing box, and the software and databases. The benefits of using BLMASIC are highlighted, including reduced component count, increased radiation tolerance, additional redundancy and diagnostics. Integration with other SPS control systems, such as timing configuration, fieldbus network communication, is also discussed, as well as the potential for reuse of the hardware in the LHC during LS4.

**Conclusion:**

The development of a control and processing electronics prototype for BLMASIC was presented. The results of the study are summarised and future development steps, including further testing, integration and potential reuse, are described. The implications of this development for engineers involved in the use of LpGBT and VTRx are highlighted, providing an example of a simple and robust control system architecture for critical systems.

**Programmable Logic, Design and Verification Tools and Methods / 103****Integrating lpGBT into the Common Readout Units (CRU) of the ALICE Experiment**

**Author:** Erno David<sup>1</sup>

<sup>1</sup> *Wigner Research Centre for Physics (Wigner RCP) (HU)*

**Corresponding Author:** [erno.david@cern.ch](mailto:erno.david@cern.ch)

In the ALICE read-out and trigger system, the present GBT and CRU based solution will also serve for Run4 without major modifications. By now, the GBT protocol has been superseded by lpGBT, and the GBT ASIC is not available for new productions. Extensions of the ALICE system (e.g. the planned FoCal detector) will therefore require to use lpGBT while keeping the compatibility with the existing system. In this presentation we show the implementation and testing of a possible integration of the lpGBT-FPGA IP into the CRU firmware, allowing the extension of the present system, keeping it more versatile and future-proof.

**Summary (500 words):**

The present integration and testing work of lpGBT in ALICE CRUs will cover the following points:

**Downlink:** Interfacing the ALICE Trigger and Timing Subsystem and the lpGBT downlink is constrained by the given clock frequencies at the two sides. In ALICE, the clock and trigger are delivered to the CRU via 9.6 Gb/s 10GPON links. The CRU firmware exploited the advantage that this speed was just the double of the 4.8 Gb/s GBT downlink speed. This allowed that the 240 MHz clock recovered in the 10GPON receiver block could be used directly as the reference clock for the GBT downlink transmitters resulting a stable and deterministic clock and trigger transition from the 10GPON to the GBT. However, in the 2.56 Gb/s lpGBT downlink, the transmitter reference clock is 160 MHz resulting that we have to divide the recovered 240 MHz clock of the 10GPON by three and multiply by two. This clock division introduces new phase uncertainty which can be fixed by an additional phase alignment block which will recognize the position of certain unique header bits in the data. In new front-end developments it also has to be considered that the lpGBT downlink transfers less trigger data (64-bits instead of 120-bits) in every clock cycle.

**Uplink:** The lpGBT uplink supports 5.12 and 10.24 Gb/s speeds. The CRU hardware, the FPGA and the transceivers, all support 10 Gb/s, but the internal interfaces in the CRU firmware need to be modified to suit the lpGBT communication. Instead of the 120-bit GBT payload at 240 MHz, the link will now provide 128-bit or 256-bit data for the User Logic at 160 MHz. The new User Logic will have to run from this new interface clock. On the other side, the interface to the PCIe DMA engine will remain the same,

feeding the dual-port FIFOs with 2x256 bits but with the new User Logic clock. The CRU driver, the low-level read-out software, and the O2 software stack will remain intact.

**Slow Control:** The lpGBT protocol still supports the 80 Mb/s control channels from the CRU to the front-end electronics. In lack of the GBT-SCA peripheral controller ASIC the front-end card designers can make use of the built-in controllers of the new lpGBT chip. The implementation of these control channels through the CRU firmware is transparent, thus the access of the of target devices on the new front-end cards needs only software development in the host computer of the CRU (FLP) and the detector control system (DCS).

**Testing:** The implementation will be tested with an VLDB+ eval board hosting a VL+ optical transceiver, the lpGBT ASIC, and an e-links interface through FMC connectors. For uplink testing the built-in packet generator of the ASIC will be used. Downwards, we will test the phase coherent clock and data recovery by an oscilloscope at the VLDB+ clock and e-link connectors. It is also possible to loop-back e-links at the FMC connectors and/or testing the communication with prototype front-end cards as soon as they get available.

ASIC / 105

## NAPA-P1: NANOSECOND TIMING PIXEL FOR LARGE AREA SENSORS

**Authors:** Alexandre Habib<sup>None</sup>; James Brau<sup>None</sup>; Martin Breidenbach<sup>1</sup>; Lorenzo Rota<sup>None</sup>; Caterina Vernieri<sup>2</sup>; Angelo Dragone<sup>2</sup>

<sup>1</sup> SLAC

<sup>2</sup> SLAC National Accelerator Laboratory (US)

**Corresponding Author:** alexhab@stanford.edu

NAPA-p1 is a prototype Monolithic Active Pixel Sensor designed in 65 nm CMOS imaging technology, developed to meet requirements for future e+e- colliders. The prototype has dimensions of 1.5 mm × 1.5 mm with a pixel pitch of 25 μm. In nominal conditions, simulations show a pixel jitter of 350 ps-rms and an Equivalent Noise Charge (ENC) of 12 e-rms. The prototype will be characterized this summer, and the results shall be available soon. A discussion will be presented on future strategies to allow the scalability of this design into a large-scale sensor of 10 cm × 10 cm.

### Summary (500 words):

The detectors at future e+e- linear colliders will need unprecedented precision on Higgs physics measurements. These ambitious physics goals translate into very challenging detector requirements on tracking and calorimetry. To develop the next generation of ultralight trackers, a further reduction of dead material can be obtained by employing Monolithic Active Pixel Sensor (MAPS) technology.

Future e+e- Colliders require fast detectors with O(ns) timing tagging. This is feasible at the cost of a relatively high-power consumption that could not be compatible with large area constraints. Today some commercial imaging technologies offer the possibility to produce large, stitched sensors (with a rectangle area ~30 cm × 10 cm). Such large sensors are very interesting from a physics point of view, but they are very challenging from an engineering point of view.

A first MAPS prototype 'NAPA-p1' is designed by SLAC in CMOS Imaging 65 nm technology. The prototype has dimensions of 1.5 mm × 1.5 mm with a pixel pitch of 25 μm. This work benefits from our collaboration with CERN, capitalizing on the improved sensor's performance after a decade of optimizations. This prototype will set the baseline for the sensor and the electronics performance which will serve future developments.

In the pixel, many design choices were motivated by the large-scale compatibility. The pixel is designed with auto-calibration schemes, thus avoiding the distribution of global signal, which would represent a high failure risk. The power consumption is kept to a minimum of 720 nW/pixel, which will be scaled down by a factor of 100 or more for low duty cycle e+e- machines.

Simulations show that to achieve our goal of 1 ns-rms jitter, the sensor capacitance has to be lower than

10 fF, and the Equivalent Noise Charge (ENC) lower than 25 e-rms. The nominal operating conditions correspond to a total current of 600 nA per pixel. In this case, the time resolution is 350 ps-rms and the ENC is 12 e-rms.

The prototype chip will be characterized this summer, and the results shall be available for presentation soon. Moreover, a discussion will be presented about the design strategies to allow the scalability of this design into a large-area stitched sensor of 10 cm × 10 cm, with specifications compatible with future e+e- colliders.

**Acknowledgment:**

We would like to acknowledge the efforts of the CERN's EP R&D WP1.2 on monolithic sensors as well as the ALICE experiment as a significant effort was provided by their groups.

**Thursday posters session / 106**

## **SAQRADC: An on-demand, low-power, minimal footprint, 10-bit resolution charge-redistribution ADC with internal clock generation**

**Authors:** Grzegorz Deptuch<sup>1</sup>; Nicholas St. John<sup>1</sup>; Soumyajit Mandal<sup>1</sup>

<sup>1</sup> Brookhaven National Laboratory

**Corresponding Author:** nstjohn@bnl.gov

A charge-redistribution ADC with 10-bit resolution is implemented in the TPSCo 65nm CMOS process. The design is intended for flexible on-demand monitoring of vital system signals, such as temperature, in MAPS detectors. The successive approximation principle is implemented using only two matched capacitors and a trimming DAC, while an internal clock generator and digital sequencer are used to generate control signals for stepping through the conversion phases. The clock generator has a programmable output frequency, allowing sampling rates of 50–500 kS/s. Layout area is minimized by optimizing the transistor count within the sequencer as well as careful full-custom layout.

**Summary (500 words):**

The measurement of environmental signals within an ASIC, such as temperature and bias currents/voltages, is vital to optimize system performance and longevity. While important, these signals do not need to be monitored continuously due to their slowly changing nature, therefore an on-demand ADC is of interest. Ideally, this ADC would also have a small footprint and require minimal conversion energy. To meet this requirement, a two-capacitor, charge-redistribution ADC with 10-bit resolution utilizing the successive approximation principle was implemented in the pixel sensor-optimized TPSCo 65nm CMOS process. A block diagram illustrating the SAQRADC is shown in Fig. 1. Capacitor C2 is either charged to Vref or discharged to ground based on the CHG/DCHG logic signals. Simultaneously, C1, which is precisely matched to C2 via a trimming DAC, is discharged to ground. The charge is then redistributed between C1 and C2 to obtain an output voltage that is compared to the input via a comparator fed by zero-input capacitance source followers. This charge redistribution process is performed k times, where k is the stage number (ranging from 1 to N, where N = 10 is the total number of bits). Since each stage requires 2k clock cycles to complete, a total of N(N+1) cycles are required per conversion. This relatively long conversion time is a consequence of the fact that the algorithm only uses two capacitors to eliminate the usual feedback DAC and simplify the control logic. Layout area is minimized by implementing the capacitors above the transistor circuitry as MOM structures on the upper metal layers while limiting signal routing to only the two bottom metal layers. Careful full-custom layout is used to minimize layout area while ensuring that all recommended DFM rules are followed. An example of the resulting constrained layout is shown in Fig. 2.

All the digital control signals for the ADC are generated by an internal sequence generator, whose functional block diagram is shown in Fig. 3. An internal clock generator with a tunable frequency ranging from 5 –50 MHz outputs the system clock once triggered via the ADC\_START input signal. This circuit

is based on a ring oscillator implemented using Schmitt triggers with digitally adjustable hysteresis, thus eliminating the need for analog tuning. The clock generator feeds two walking-1 counters, one of which generates the DAC control signals and the other defines which bit is being computed. Since the number of cycles required for charge redistribution in the DAC is proportional to the bit number, the two walking-1 counters effectively work in tandem as a nested for-loop, as illustrated in the sequencer output waveforms shown in Fig. 4. Each counter, which is implemented as a twisted-ring (Johnson) counter, only requires 5 flip-flops for 10-bit counting. All combinational and sequential logic blocks are custom designed to minimize the total number of transistors; the final implementation only requires 731 transistors to generate all internal digital signals, including the system clock. The simulated characteristics of the ADC, along with the estimated layout area, are summarized in Table 1.

#### Thursday posters session / 108

## An FPGA-based Data Aggregator for ATLAS ITK Pixel DCS System

**Authors:** Ahmed Qamesh<sup>1</sup>; Christian Zeitnitz<sup>1</sup>; Lucas Schreiter<sup>2</sup>

**Co-authors:** Felix Nitz; Michael Karagounis<sup>3</sup>; Peter Kind<sup>1</sup>; Rizwan Ahmad<sup>1</sup>; Susanne Kersten<sup>1</sup>; Tobias Krawutschke<sup>4</sup>

<sup>1</sup> *Bergische Universitaet Wuppertal (DE)*

<sup>2</sup> *FH Dortmund*

<sup>3</sup> *Fachhochschule Dortmund Univ. of Applied Sciences and Arts (DE)*

<sup>4</sup> *TH Köln*

**Corresponding Author:** ahmed.qamesh@cern.ch

During the ATLAS phase II upgrade, the tracking system of the ATLAS experiment will be replaced by an all-silicon detector called the inner tracker (ITK) with a pixel detector as the most inner part. The monitoring data of the new system will be aggregated from an on-detector ASIC called Monitoring Of Pixel System (MOPS) and sent to the Detector Control System (DCS) using a new interface called MOPS-HUB.

The hardware implementation and experimental results of the MOPS-HUB will be presented. In addition, mitigation techniques including Single-Event Upset (SEU) and Single-Event Transients (SET) for the new system will be introduced.

#### Summary (500 words):

The ATLAS experiment will get a new inner tracker (ITk) during the phase II upgrade. The innermost part will be a pixel detector. After the upgrade, the pixel detector will have 5 times more modules than the present state. The ATLAS pixel detector will use a serial powering scheme to reduce the number of services inside the detector volume, therefore a new Detector Control System (DCS) is being developed at the University of Wuppertal to fulfill the control and monitoring requirements of the new pixel detector. The new DCS has an on-detector ASIC called Monitoring Of Pixel System (MOPS) to monitor the voltages and temperatures of the detector modules and other sub-detector components.

A system integration plan of the MOPS chip that includes powering and communication has been proposed with MOPS-HUB as the central unit. The MOPS-HUB is an FPGA based interface. Its main task is the aggregation of monitoring data between the MOPS chips (installed at the vicinity of the detector modules) and the DCS computer.

Beside that, the MOPS-HUB will monitor information per CAN bus (voltage/current) and send it to the DCS computer as part of the data stream. In addition, it will have a full power control over the connected Controller Area Network (CAN).

`\begin{figure}[htp]`

`\centering`

`\includegraphics[width=0.85\textwidth]{figs/PhD_Designs.png}`

`\caption{\label{fig:construction} The complete MOPS-HUB network.}`

`\end{figure}`

The core unit of the MOPS-HUB will be the MOPS-HUB FPGA. The Firmware design of the MOPS-HUB

FPGA will allow the communication with the MOPS chips over CAN bus using an integrated CAN controller and a physical layer. In addition, the data aggregated between the MOPS-HUB FPGA and the DCS will go through different stages. First, the MOPS-HUB FPGA will communicate with an Embedded Monitoring and Control Interface (EMCI) through low power differential signals called elinks. Second, the EMCI will serve as a bidirectional channel interface that will transmit the data through a high-speed optical link to an Embedded Monitoring Processor (EMP), which is placed in a non-radiation environment (see Figure<sup>1</sup>). The EMP will deliver the data to the DCS by means of an Ethernet connection.

Some special requirements on the design and firmware is also considered (e.g TMR and re-configuration) since MOPS-HUB will be placed in a radiation environment.

The hardware implementation and experimental results of the MOPS-HUB and its integration plan will be presented. In addition, mitigation techniques including Single-Event Upset (SEU) and Single-Event Transients (SET) for the new system will be introduced.

**Tuesday posters session / 109**

## **Electrical / piezo-resistive effects in bend Alpide - Monolithic Active Pixel (MAP) sensors**

**Author:** Marcus Johannes Rossewij<sup>1</sup>

**Co-authors:** Else Okkinga ; Haadi Naqvi<sup>2</sup>; Rene Georges Ernst Barthel<sup>1</sup>; Stijn Alving<sup>2</sup>

<sup>1</sup> *Nikhef National institute for subatomic physics (NL)*

<sup>2</sup> *Utrecht University*

**Corresponding Author:** m.j.rossewij@uu.nl

Upcoming upgrade of the ALICE Inner Tracking System (ITS3) foresees the use of wafer-scale MAPs bent into a cylindrical shape. Test beams employing the current ALICE Alpide chips, bent to foreseen ITS3 radii, showed that MAPs remain fully functional. However, some electrical effects, like (PS) power supply current changes and voltage shifts, were observed. The results suggest that these are caused by “piezo resistive effect” and FET threshold shifts, probably occurring in the pixel transistors. Some design architectures showed to be less susceptible to these effects and detailed investigations could help in design optimization. This contribution discusses latest test results.

### **Summary (500 words):**

The ITS3 design foresees the replacement of the three innermost layers of the current ALICE tracker (ITS2) with wafer-scale stitched MAP sensors (65 nm) bent to truly cylindrical shapes. Multiple (beam) tests with the existing ITS2 MAP (=Alpide chip, 180 nm) in bent state showed that the Alpide remains fully functional and performance is mostly unaffected.

However, compared to the strain ( $\approx 0.1\%$ ) induced by bending, there was a relative large ( $\approx 10\%$ ) change in analog PS current, corresponding to a gauge factor (fractional resistance change / strain) of  $\approx +83$  bend along the long axis and  $\approx -46$  bend along the short axis. Observations can be explained by the “piezo resistive effect”. The gauge factor size and sign reversal are indeed compatible with the known piezo resistive coefficients for N-silicon. It is shown how piezo resistance depends on strain, current and lattice orientation which could eventually be used for design optimization.

The analog PS current change is more dominant than the digital current change, probably originating from the repetitive pixel structure. As the analog pixel section PS current strongly depends on its (transistor) operation point which is set by bias currents and voltages generated by an on-chip DAC, the question arises if the PS current changes originate from changes in the on-chip DAC outputs or occur in the pixel transistors themselves. As the Alpide allows forwarding the output signal of a selected DAC to an analog monitoring pin, it can be measured directly how the DAC output is affected by bending and if these changes are responsible for the PS current changes.

A dedicated measurement setup with monitoring pin access was built allowing convex and concave bending over long and short axis. Convex uses a plastic sheet for bending the Alpide over a mandril with

curvature radii of 18, 24 and 30 mm as foreseen in ITS3. Concave bending employs porous aluminum profiles where vacuum keeps the Alpipe in a bent state.

The DAC outputs indeed change when bent, but this explains only 25% of observed PS current change. Therefore, the main part should occur in the pixel transistors themselves. Bent Alpipes also show a small pixel threshold shift. The measured DAC outputs even change in the reverse direction, so also here the pixel transistors are likely responsible for the pixel threshold shifts.

The Alpipe has 3 types of DACs showing different behavior when bent:

- 1) Voltage DAC with opamp: No change measured ( $\ll 1\%$ ). Unaffected as the resistor ladder divides out changes in individual resistors. The opamp feedback corrects errors in the output stage.
- 2) Voltage DAC with source follower: Small shift ( $< 1\%$ ). Assuming resistor ladder remains unaffected again, the source follower stage should introduce this shift, which differs from what is expected from the piezo-resistive effect. It seems that another physical mechanism is responsible, i.e. FET threshold shift. Literature reports FET threshold shifts of similar size.
- 3) Current DAC: Changes  $\approx 2\%$ . No correction mechanism is present.

For the future ITS3 development, additional tests with 65nm test structures are foreseen.

ASIC / 111

## Performance of the COLUTA ADC ASIC for the ATLAS HL-LHC Liquid Argon Calorimeter Readout

**Authors:** Michael Himmelsbach<sup>1</sup>; Michael Himmelsbach<sup>1</sup>; Timothy Robert Andeen<sup>1</sup>

<sup>1</sup> *University of Texas at Austin (US)*

**Corresponding Authors:** [himmelsm@utexas.edu](mailto:himmelsm@utexas.edu), [michael.scott.himmelsbach@cern.ch](mailto:michael.scott.himmelsbach@cern.ch)

The COLUTA ASIC is an 8-channel 15-bit 40 MSPS ADC fabricated in 65 nm CMOS for the upgrade of the readout of the ATLAS LAr calorimeter for the high luminosity LHC. The ADC architecture couples a 3.5-bit Multiplying-DAC (MDAC) stage to a successive approximation register (SAR) ADC with a digital back-end that outputs sample data continuously via 640 Mbps serial LVDS. The analog performance and radiation tolerance tests and measurements of the production COLUTA ADC will be presented, along with the robotic multi-chip test setup and procedures developed for the verification of 80,000 COLUTA ADC ASICs.

### Summary (500 words):

To meet new physics challenges and withstand the expected radiation doses at the high-luminosity LHC (HL-LHC), the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded. The triangular calorimeter signals are amplified and shaped by analog electronics over a dynamic range of 16 bits, with low noise and excellent linearity. In order to digitize the analog signals on two overlapping gain scales after shaping, the radiation-hard, low-power 40 MHz 15-bit COLUTA ADC was developed.

The COLUTA ADC ASIC is a custom 8-channel 15-bit 40 MSPS ASIC fabricated in 65nm CMOS. The ADC architecture couples a 3.5-bit Multiplying-DAC (MDAC) stage to a successive approximation register (SAR) ADC with an on-chip Digital Data Processing Unit (DDPU) that determines and applies the MDAC and SAR calibration constants and formats the output data. The sample data and frame are continuously output via 640 Mbps serial LVDS to CERN Low Power Gigabit Transceiver (lpGBT) ASICs.

Measurements of the production version of the COLUTA ADC verify the sampling performance above specification of  $>11.5$ -bit ENOB at the characteristic frequencies of the LAr signals. The design and development of the ADC will be presented, along with performance measurements. The ADC was tested in a proton beam to confirm the radiation tolerance. The results of this testing, including the Single Event Effects (SEE) cross section measurement, will also be presented.

In order to test the 80,000 COLUTA ADCs for the LAr upgrade, a robotic multi-chip test setup has been prepared. The design of this setup, along with initial yield measurements, with a particular emphasis



on the process-related spread of key ASIC parameters related to qualification, will be discussed.

## Radiation-Tolerant Components and Systems / 112

# Characteristics and total ionizing dose response of 22nm Fully Depleted Silicon-on-Insulator

**Authors:** Gennaro Termo<sup>1</sup>; Giulio Borghello<sup>2</sup>; Federico Faccio<sup>2</sup>; Kostas Kloukinas<sup>2</sup>; Michele Caselle<sup>3</sup>; Alexander Friedrich Elsenhans<sup>4</sup>; Ahmet Cagri Ulusoy<sup>4</sup>; Adil Koukab<sup>1</sup>; Jean Michel Salles<sup>1</sup>

<sup>1</sup> *École Polytechnique Fédérale de Lausanne (EPFL)*

<sup>2</sup> *CERN*

<sup>3</sup> *KIT - Karlsruhe Institute of Technology (DE)*

<sup>4</sup> *KIT-Karlsruhe Institute of Technology*

**Corresponding Author:** gennaro.termo@cern.ch

The radiation hardness of transistors in a 22nm Fully Depleted Silicon-On-Insulator (FDSOI) technology exposed to ultra-high total ionizing dose (TID) was investigated. Custom structures including n- and p-channel devices with different sizes and threshold voltage flavours were irradiated with X-rays up to a TID of 100 Mrad(SiO<sub>2</sub>) with different back-gate bias configurations, up to 2 V. The investigation revealed that the performance is significantly affected by TID with their radiation response being dominated by the charge trapped in the buried oxide. Interestingly, the application of a back-bias of 2 V was not enough to compensate the TID-induced damage.

### Summary (500 words):

Single Event Effects (SEEs) are a major cause of failure for Application Specific Integrated Circuits (ASICs) operating in harsh radiation environments, such as space or particle accelerators. A particle with large Linear Energy Transfer (LET), like an energetic ion, crossing the substrate of a semiconductor device creates an ionization tail of electron-hole pairs. In a bulk technology, this charge can be collected relatively deep in the substrate and originate current pulses at active nodes of the circuit, giving origin to SEU (upsets), SET (transient) or SEL (latchup).

In Silicon-On-Insulator (SOI) technologies, the thin silicon film that forms the channel overlays a thick buried oxide (BOX) that isolates it from the bulk substrate. The presence of the BOX limits the extension of the charge collection region and makes these technologies intrinsically more tolerant to SEE. Moreover, it allows the possibility of tuning the electrical characteristics of individual transistors by the application of individual (or grouped) body or back-gate bias. However, the BOX is typically tens of nanometers thick and therefore prone to trap a large amount of charge when exposed to ionizing dose. In view of possible application in HEP, where doses can be orders of magnitude higher than those typically reached in space applications, it is interesting to study the Total Ionizing Dose (TID) response of commercial SOI technologies and if/how it can be improved by dedicated biasing techniques.

In this work, the characteristics of n- and p-channel transistors with different sizes and threshold voltage flavors in a 22nm Fully Depleted SOI (FDSOI) technology were evaluated before irradiation and after exposure to X-rays up to a TID of 100 Mrad(SiO<sub>2</sub>). Preliminary data showed that both nMOS and pMOS are severely affected by TID. A TID of 1 Mrad(SiO<sub>2</sub>) is sufficient to cause a ~70% degradation of the on-current in pMOS devices, regardless the width of the transistor. The size independence is a strong indication that performance degradation is primarily caused by the charge trapped in the BOX. In both nMOS and pMOS the variations of the on-current can be explained by the threshold voltage shift induced by the trapped charge. The observed rebound in the response of nMOS devices is related to the late formation of negatively charged interface traps, which compensate the charge trapped in the oxide, a mechanism similar to that observed in other bulk CMOS transistors.

The compensation of radiation effects by changing the body or back-gate bias was explored. It is possible to compensate the effects only for TID < 1 Mrad. Unfortunately, the bias to be applied for the same dose is different between nMOS and pMOS transistors. In our presentation we will additionally show results of an on-going study about the impact of the back-gate bias during high-temperature annealing and of back-bias voltages higher than the maximum V<sub>dd</sub> of the technology (2V). The aim is to enhance electron tunneling from the substrate to compensate for the charge trapped in the BOX and improve the radiation response.

ASIC / 113

## Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers

**Authors:** Aldo Pena Perez<sup>1</sup>; Angelo Dragone<sup>2</sup>; Ariel Gustavo Schwartzman<sup>2</sup>; Bojan Markovic<sup>2</sup>; Caterina Vernieri<sup>2</sup>; Dong Su<sup>2</sup>; Larry Lou Jr Ruckman<sup>2</sup>; Lorenzo Rota<sup>None</sup>; Valentina Cairo<sup>3</sup>; aseemg Gupta<sup>None</sup>

<sup>1</sup> SLAC National Accelerator Laboratory

<sup>2</sup> SLAC National Accelerator Laboratory (US)

<sup>3</sup> CERN

**Corresponding Authors:** larry.lou.jr.ruckman@cern.ch, bojan.markovic@cern.ch

4D tracking with  $\sim 10$ ps timing is crucial for reducing the combinatorial challenge of track reconstruction at high pileup densities, it offers completely new handles to detect and trigger on LLP and enables particle-ID capabilities at low transverse momentum. At the Muon Collider, the timing information will be essential for reduction of BIB. A high-precision TDC is a critical block necessary for enabling 4D tracking. We present the design and characterization of a 4-channel sub-10ps TDC ASIC in 28nm CMOS technology. The developed TDC is based on a novel 2D Vernier ring-oscillator structure with embedded sliding-scale technique for conversion linearity improvement.

### Summary (500 words):

4D trackers with  $\sim 10$ ps timing will be transformative at future collider experiments. Timing is crucial for reducing the combinatorial challenge of track reconstruction at extremely high pileup densities, it offers completely new handles to detect and trigger on long-lived particles (LLP), expands the reach to search for new phenomena, and enables particle-ID capabilities at low transverse momentum. At the Muon Collider, the timing information will be essential for reduction of the beam-induced background (BIB).

CERN's EP-R&D-WP5 survey has promoted the selection of 28nm CMOS node as the next step in microelectronics scaling for HEP designs. As one of the critical blocks necessary to enable 4D operation in trackers, we present the design and characterization of a 4-channel sub-10ps Time-to-Digital Converter (TDC) ASIC in the 28nm node. The developed TDC is based on a novel 2D Vernier ring-oscillator structure with embedded sliding-scale technique for conversion linearity improvement that will simplify calibration of the TDCs, especially useful in high-channel count implementations such as 4D trackers. The core of the TDC architecture is composed of differential voltage-controlled delay cells set at 50ps propagation delay and assembled in a 4-cell ring-oscillator with enable/disable function with programmable starting state. The ring-oscillator, enabled with a START trigger, coupled with a counter and a series of flip-flops that sample the oscillator's state at a STOP-trigger, is capable of performing time-interval quantization with 50ps time-steps and a range of 1.6ns. The feature of having the oscillator starting condition programmable, coupled with pseudo-random selection of the starting point at each measurement cycle, performs the sliding-scale function thus improving the conversion linearity beyond the limits set by mismatches between the delay cells of the ring-oscillator. To reach a sub-10ps resolution, the 50ps time-step of the previous structure is interpolated by a factor of 8 using a second ring-oscillator with delay cells set to 56.25ps propagation delay and enabled by a second STOP signal. Each step of the first ring-oscillator is sampled in correspondence of both rising and falling edges of the second ring-oscillator by a 2D array of flip-flops. This 2D Vernier structure reaches a resolution equal to the difference of propagation delays of cells in the two oscillators, i.e. 6.25ps. Compared to a traditional Vernier TDC, the 2D configuration allows faster conversion times and longer measurement range. Both ring-oscillators implement the programmable starting state, i.e. sliding-scale, thus improving the linearity of the overall conversion.

The schematic and layout of a TDC channel is shown in Fig. 1. Each channel receives one START and two STOP signals, simultaneously performing a 6.25ps and a 50ps measurements of the two time-intervals, for example a time-of-arrival (TOA) and a time-over-threshold (TOT) measurement. The 1.6ns measurement range of the prototype can easily be extended in future iterations by simple addition of a flip-flop to the counter. The 4-channel ASIC is shown in Fig. 2. The ASIC was submitted at the end of January and the characterization is expected to start in May. Both the design and characterization will be presented at the workshop.

**Thursday posters session / 114****Development of FABulous: An Embedded FPGA Framework in 28nm CMOS****Author:** Larry Lou Jr Ruckman<sup>1</sup>**Co-authors:** Hyunjoon Kim <sup>2</sup>; Lorenzo Rota ; aseemg Gupta<sup>1</sup> *SLAC National Accelerator Laboratory (US)*<sup>2</sup> *SLAC National Accelerator Laboratory (US)***Corresponding Author:** larry.lou.jr.ruckman@cern.ch

FABulous is an open-source eFPGA framework developed by the University of Manchester, enabling programmable digital logic to be integrated into ASIC designs. In 2023, our team plans to submit a 28nm CMOS ASIC and explore flatten versus hierarchical design using HVT devices for radiation hardening. This 28nm eFPGA design will use SUGOI and PGPv4 to program and move data in and out of the eFPGA. Post-PnR simulation results will be presented, along with full chip co-simulation with firmware/software for pre-tape out validation results.

**Summary (500 words):**

With the push for future high energy physics detectors to move more processing to the edge in the effort to reduce data volumes at the earliest possible stage, the ability to use programmable digital logic further up the digital signal processing chain becomes more important. While embedded Field Programmable Gate Array (eFPGA) that is built into Application-Specific Integrated Circuit (ASIC) is nothing new, these frameworks were not free and were not open source. In recent years several popular FPGA architectures have become 20+ years old, which means that original patents have expired. In 2021 University of Manchester started a project called FABulous, which is an open-source eFPGA Framework.

FABulous has demonstrated eFPGA designs in 180nm CMOS and 130nm CMOS by the University of Manchester. In 2022 SLAC demonstrated an eFPGA design using FABulous in 130nm CMOS Multi-Process Wafer (MPW). For 2023 we plan to tape out a 28nm CMOS MPW in July 2023 and expect to receive the ASIC back in November 2023. The goal of using 28nm is to determine what programmable logic area density can be achieved while using HVT devices for radiation hardening.

This 28nm eFPGA design will use SLAC Ultimate Gateway Operational Interface (SUGOI), which is a lightweight 8B10B based serial protocol for register access, to load the eFPGA bitstream. Pretty Good Protocol Version 4 (PGPv4), which is a 64B66B based serial protocol design for Trigger Data Acquisition (TDAQ) systems, will be used to move data in and out of the eFPGA.

Our team is exploring the use of flatten versus hierarchical design in the same digital ASIC tape out and will compare the programmable logic area density results before ASIC tape out. Since we will receive the ASIC design after this conference, we plan to present the results of the physical implementation and any post Place and Route (PnR) simulations at proceedings. Finally, we will discuss the full chip co-simulation with firmware/software for pre-tape out validation prior to the tape-out.

**Radiation-Tolerant Components and Systems / 116****CRATEBO: A High-speed, Radiation-Tolerant and Versatile Testing Platform for FPGA Radiation Qualification for High-Energy Particle Accelerator applications****Author:** Antonio Scialdone<sup>1</sup>**Co-authors:** Rudy Ferraro <sup>2</sup>; Panagiotis Gkountoumis <sup>3</sup>; Salvatore Danzeca <sup>2</sup>; Luigi Dilillo <sup>4</sup>; frederic saigne ; Jerome Boch ; Alessandro Masi <sup>2</sup>

<sup>1</sup> *Universite Montpellier II (FR)*

<sup>2</sup> *CERN*

<sup>3</sup> *Boston University (US)*

<sup>4</sup> *LIRMM/CNRS/Université de Montpellier*

**Corresponding Author:** antonio.scialdone@cern.ch

The CHARM Radiation Tolerant Tester Board (CRATEBO) is a testing platform for the CERN High-energy Accelerator (CHARM) irradiation facility. It is meant to ease the radiation testing of FPGA-based systems by providing users with a radiation-tolerant carrier card for the Device Under Test (DUT). It provides a high-speed communication interface, a flexible power supply, and DUT connections via a System-On-Module socket and an HPC-FMC connector. It is a permanent installation in the CHARM facility at CERN that gives the possibility to users to perform radiation tests of their system with minimum development effort on the test setup.

**Summary (500 words):**

Field-Programmable Gate Arrays (FPGAs) are widely used in electronic systems due to their high performance, flexibility, and cost-effectiveness. At CERN, many systems involving FPGAs are used in the Large Hadron Collider (LHC) radiation environment, therefore their qualification is crucial to ensure a reliable operation.

Our previous work involved benchmark circuits to test FPGAs, which in addition to the classical element testing improved the qualification process enabling comparisons between different FPGA technologies. However, retrieving the failure rate of actual FPGA-based designs, especially in complex systems like detector electronics, is still a challenging task.

To address these challenges, the CHARM Radiation Tolerant Tester Board (CRATEBO) was developed. It is designed to ease the radiation testing process for FPGAs and other systems. It is intended for permanent installation in the CERN High-energy Accelerator (CHARM) irradiation facility offering the opportunity to test and qualify systems in a mixed-radiation field that replicates real radiation environments.

CRATEBO provides all the features essential to conduct radiation testing, i.e. DUT interfaces, communication link, and power supply. These features have a great degree of flexibility to accommodate many kinds of tests.

The board implements a System-On-Module socket to host FPGAs. Currently, several FPGAs SOMs have been developed and tested using CRATEBO. Other international collaborations are underway to test new FPGA applications. The board also includes a standard HPC-FMC connector, which has two main advantages. First, it is particularly useful when testing systems based on FPGAs and connected to a front-end electronic card, like detector electronics. In these cases, CRATEBO allows to perform a radiation test of the full application with minimal development on the test setup. Secondly, the compliance with the FMC standard enables testing of any other commercial module like RF Transceiver and high-speed ADCs.

Concerning the communication interface, CRATEBO implements a high-speed bidirectional link, up to 4.8 GB/s, based on the radiation tolerant Giga Bit Transceiver ASIC (GBTx). Its advantages are threefold. It enables reliable communication with the DUT, preventing corruption of experimental data. It gives the possibility to test challenging designs that involve high-data rate processing. Additionally, it allows testing of actual designs made at CERN, since they use the same communication interface. However, other communication interfaces can be used if necessary. Wireless modules are being developed in this perspective.

The board features a flexible power scheme that can be adapted to the voltage requirements of the DUTs or FPGAs. It uses radiation-tolerant power modules that come with either the radiation-hardened ASICs developed at CERN or with radiation-qualified Commercial Off-The-Shelf (COTS) components. In the latter case, the modules can be replaced before reaching their Total Ionizing Dose (TID) threshold. The front-end FMC connectors have a separate supply to avoid potential Single Event Latch-up (SEL) on the FMC DUT from propagating to the carrier board.

In summary, CRATEBO significantly reduces the user's burden in the test setup and installation for FPGA-based applications. Its flexibility in communication, power supply and DUT interface, coupled with its radiation tolerance, make it a suitable platform to test FPGAs and other systems.

## The LHCb VELO Upgrade II: design and development of the read-out electronics

**Authors:** Kazuyoshi Carvalho Akiba<sup>1</sup>; Stefano De Capua<sup>2</sup>; Victor Coco<sup>3</sup>

<sup>1</sup> *Nikhef*

<sup>2</sup> *University of Manchester (GB)*

<sup>3</sup> *CERN*

**Corresponding Authors:** antonio.fernandez.prieto@cern.ch, sdecapua@cern.ch

The the LHCb collaboration proposes a Phase-II Upgrade of the detector, to be installed during the LHC Long Shutdown 4. Currently, the VELO collaboration is exploring new sensor technologies, and the benefits that would derive from adding a time stamp to the track reconstruction. The most recent advances in this field, and the potential candidates that can meet the VELO Upgrade-II requirements, will be presented. In particular, the current state-of-the-art prototypes in the development of ASICs with TDC-per-pixel architecture, the PicoPix ASIC (which is an evolution of the Timepix4 design) and the TIMESPOT ASIC, will be discussed.

### Summary (500 words):

In order to fully exploit the High-Luminosity LHC potential in flavour physics, the LHCb collaboration proposes a Phase-II Upgrade of the detector, to be installed during the LHC Long Shutdown 4 (2032-2034). Operating in the HL-LHC environment poses significant challenges to the design of the upgraded detector, and in particular to its tracking system. The primary and secondary vertices reconstruction will become more difficult due to the increase, by a factor 8, of the average number of interactions per bunch crossing (pile-up). Similarly, the track reconstruction will become more challenging, as well as time-consuming, because of the large increase in the track multiplicity. Finally, the much harsher radiation environment will make the design of the sub-systems quite challenging, with the radiation damage expected to be more severe for most detectors. In particular, the performance of the VERtex LOcator (VELO), which is the tracking detector surrounding the interaction region, is essential to the success of this Phase-II Upgrade. Data rates are especially critical for the LHCb full software trigger, and with the expected higher particle flux, the VELO Upgrade-II detector will have to tolerate a dramatically increased data rate: assuming the same hybrid pixel design and detector geometry, the front-end electronics (ASICs) of the VELO Upgrade-II will have to cope with rates as high as 8 Ghits/s, with the hottest pixels reaching up to 500 khits/s. With this input rate, the data output from the VELO will exceed 30 Tbit/s, with potentially a further increase if more information is added to the read-out. The VELO collaboration is currently exploring new sensor technologies, and the benefits that would derive from adding a time stamp to the track reconstruction, such that interactions in the same bunch crossing can be more effectively disentangled. Recently, the implementation of precise (~50 ps) time measurement in combination with excellent spatial resolution has become technologically possible. Moreover, the VELO case is extremely challenging, as the high granularity required for the spatial measurement severely limits the area in each pixel of the ASIC where the time-stamping circuitry can be implemented. Achieving a hit resolution of 50 ps per pixel is considered possible within the timescale of the Phase-II Upgrade. With such resolution, each VELO track would have multiple time measurements from the traversed pixels, which will lead to a precise estimation of the production time of charged particles. Moreover, at the hit level, a precise timing information will also help reducing the number of possible combinations to be considered for the track reconstruction, thus improving its quality. The most recent advances in this field, and the potential candidates that can meet the VELO Upgrade-II requirements, will be presented. In particular, the current state-of-the-art prototypes in the development of ASICs with TDC-per-pixel architecture, the PicoPix ASIC (which is an evolution of the Timepix4 design [3]) and the TIMESPOT ASIC [4], will be discussed. The most recent studies carried out on these two candidates will be presented, as well as the last results from simulations.

Tuesday posters session / 118

## On-beam system test of the new readout electronics for the CMS Electromagnetic Calorimeter upgrade

**Author:** CMS ECAL Collaboration<sup>None</sup>

**Corresponding Author:** mattia.campana@cern.ch

The High-Luminosity phase of the CERN Large Hadron Collider will pose new challenges for the detectors. The Electromagnetic Calorimeter (ECAL) of the CMS experiment will be equipped with a completely new readout electronics to cope with increase in the number of pp collisions per bunch crossing, as high as 200, and higher noise induced by radiation. Two on-beam vertical integration tests were performed at the CERN H4 facility using near-final components, installed in an ECAL Supermodule identical to the 36 Supermodules the barrel is made of. The data acquisition chain and the results of the test beam will be presented.

**Summary (500 words):**

The CMS Electromagnetic Calorimeter is composed, in the barrel region, of 61200 PbWO<sub>4</sub> scintillating crystals read by avalanche photodetectors (APD).

The new ECAL readout electronics for HL-LHC is composed of a front-end and a back-end system. The former is made of the VFE card, serving 5 crystals, and FE card, connected to the 5 VFE cards that compose the “readout tower” alongside the LVR card for power supply. On the VFE card, the signal from the APD is amplified by the CATIA transimpedance amplifier ASIC via two independent gain channels and sampled by the LiTE-DTU ASIC at 160 MHz. The digitised samples, after compression and digital gain selection, are sent via optical connection to the backend through the FE, which comprises 4 lpGBT chips. The lpGBT ASIC (Low Power GigaBit Transceiver) is a new 65nm-CMOS radiation tolerant serialiser/deserialiser device designed for HL-LHC applications. On the backend, the custom-designed Barrel Calorimeter Processor (BCP) cards implements trigger and readout algorithm by use of large FPGAs.

The use of lossless compression algorithms, needed to optimise bandwidth allocation, poses non-trivial channel synchronisation and alignment problems. To ease this task, the LiTE-DTU can receive a start-of-orbit signal (BC0) and tag the corresponding sample. The BC0-marked sample can then be used by the BCP to align the channels. We have studied the problem extensively using pulse injection from an external signal generator and by use of the monitoring system that injects laser light in the ECAL crystals.

Numerous link stability studies were conducted. In particular, the LiTE-DTU implements the PLL block from the lpGBT chip to generate the 1.28 GHz clock that underlies the transmission. Error transmission rates were studied as a function of the PLL capacitor setting.

The ECAL barrel is composed of 36 supermodules of 1700 channels. A spare supermodule was equipped with 200 channels of near-production electronics, while a first version of the BCP provided back-end readout. This system was used for the tests above and for two test-beam campaigns at the CERN H4 facility in November 2022 and July 2023. Electron beams of 20 to 200 GeV permitted a full assessment of the performances in terms of electronics ( noise, error rate, functionality) and physics (energy and time resolution). A detailed analysis of the data acquired in these campaigns will be presented.

**Tuesday posters session / 119**

## **32-channels mixed-signal processor for the tracking system of the GAPS dark matter experiment**

**Author:** Elisa RICEPUTI<sup>None</sup>

**Co-authors:** Gianluigi Zampa ; Lodovico Ratti <sup>1</sup>; Lorenzo Fabris ; Luca Ghislotti <sup>2</sup>; Massimo Manghisoni <sup>3</sup>; Mirko Boezio <sup>4</sup>; Paolo Lazzaroni <sup>5</sup>; Valerio Re <sup>6</sup>

<sup>1</sup> *University of Pavia*

<sup>2</sup> *University of Bergamo*

<sup>3</sup> *Università di Bergamo - Italy*

<sup>4</sup> *Università e INFN, Trieste (IT)*

<sup>5</sup> *University of Bergamo & INFN Pavia*

<sup>6</sup> *INFN*

**Corresponding Author:** elisa.riceputi@unibg.it

This work aims to describe the experimental performance of a module consisting of four Lithium-drifted Silicon (Si(Li)) detectors and their readout electronics, which is the main component of a tracker in an upcoming balloon experiment. The activity is carried out within the GAPS (General AntiParticle Spectrometer) collaboration, whose scientific objective is the indirect detection of dark matter, through the detection of antiparticles present in low-energy cosmic-rays. The balloon flight is expected from McMurdo station in Antarctica in 2024. The main object of this study is the analysis of the readout electronic performance, with particular focus on the noise.

**Summary (500 words):**

The GAPS experiment aims to detect indirect signatures of dark matter through the identification of cosmic antimatter particles. The instrument is composed of two structures. One is the silicon tracker, which acts both as a stopping material for the incident particle and as of X-ray spectrometer and charged particle tracker for the interaction products. The other one is the Time-of-Flight system which provides the energy scale and the instrument trigger. The tracker of the first flight is composed by 10 layers of two different types. The upper 7 layers are made by 6x6 modules. Every module consists of four 8-strip Si(Li) detectors, a readout ASIC and a FrontEnd Board (FEB), which electrically connects the detectors with the ASIC and powers them. Each tracker layer is organized in rows: a row is made up of 6 modules in cascade connection via Flex-Rigid PCBs which allows the transmission of both the signals to and from the ASICs, and the low voltage power supplies. The lower 3 layers are composed by 6x6 dummy modules. The latter emulate the presence of a real module: they consist of 4 disks having the same size and weight as the detectors and a FEB populated only by passive components which emulate the power consumption of the readout electronics. The readout ASIC designed for the Si(Li) detectors is called SLIDER32 (32-channels Si(LI) DETector Readout) and was fabricated in a 180nm CMOS technology. It includes 32 analog readout channels and integrates, as a first stage, a charge preamplifier with dynamic signal compression to cover the wide detection range required by the experiment (20 keV - 100MeV). The second stage of the channel is a unipolar semi-Gaussian time-invariant filter with 8 selectable peaking times, ranging from 300 ns to 1.8  $\mu$ s. 600 ASICs were fabricated and individually tested to select the 300 with the best performance. During the selection, particular emphasis has been paid to the electronic noise. The goal is to obtain an energy resolution below 4 keV FWHM, for low energy signals (up to a few tens of keV) in order to be able to distinguish X-rays of interest for the experiment. The characterization included a 40 pF capacitor at each input to account for the detector capacitance. After the production of the boards, a second characterization phase was carried out to assess that mounting SLIDER32 onto the FEB did not affect its performance. A power consumption of 7.2mW per channel has been obtained. A chain of 6 FEBs in cascade was also characterised in order to emulate a full single row. All the electronics, i.e. FEBs, dummy FEBs and FRB, underwent one thermal cycle in a climate chamber (from -40 °C to 60 °C). A very high yield was obtained on all the tested PCBs (from 86% to 100 %).

**Thursday posters session / 120**

## **Two HVCMOS active pixel ASIC designs for the Measuring GCR and SEP with a combined dynamic range of >80dB**

**Authors:** Alexandros Papangelis<sup>1</sup>; Charalambos Lambropoulos<sup>1</sup>; Elena Papadomanolaki<sup>2</sup>; Gerasimos Theodoratos<sup>2</sup>; Ioannis Glykiotos<sup>2</sup>; Michalis Torris<sup>2</sup>

<sup>1</sup> National kapodistrian University of Athens, Aerospace and Technology Department

<sup>2</sup> ADVEOS Microelectronic Systems P.C.

**Corresponding Author:** e.papadomanolaki@adveos.com

The design of HVCMOS pixel detectors for measuring Galactic Cosmic Rays (GCR) and Solar Energetic Particles (SEP) in space is presented. The design goals are: (a) cover a very wide dynamic range (from ~0.5fC to pC) and (b) minimize the power consumption. Two pixel designs were implemented, one tailored to the measurement of high energy depositions due to impinging ions and one with high gain for the low energy depositions resulting from minimum ionizing particles. Both designs have been fabricated in the LFoundry 0.15 $\mu$ m technology. The design choices are backed by simulation results and preliminary measurements.

**Summary (500 words):**

Fully depleted Si monolithic active pixel sensors (called HVCMOS or DMAPS) have been studied and introduced in high energy physics experiments for measuring minimum ionizing particles. However, for measuring GRC and SEP events in space, the sensor should be able to process charges with a dynamic range >80dB. Additionally, the specification for power consumption should be as low as possible. With these requirements in mind, we mean to respond to the demand for miniaturized instruments which could increase the crew autonomy for operational decisions related to radiation hazards and to the science opportunities resulting from the boost of planetary exploration.

To efficiently process the charge dynamic range, two sensor designs, one 'low gain' and one 'high gain' were implemented. Fig. 1. shows the block diagrams of the two pixels.

The low gain pixel does not contain a charge amplifier. The sensor cathode is held at the reset voltage due to the negative feedback of a buffer which also provides the path of the sensor's leakage current. When a particle traverses the sensor, the negative transition of the cathode voltage forces a comparator to quickly flip and disconnect the in-pixel sampling capacitor from the reset voltage and connect it to the sensor cathode instead. The capacitor voltage is proportional to the charge collected and is transferred to the array periphery to be digitized by a successive approximation ADC. Thus, a drastically reduced current consumption is achieved (35nA/pixel when idle).

For the high gain pixel, a diode connected NMOS is used to bias the sensing diode. The sensing diode capacitance required in this case should be of the order of 500fF for a 100  $\mu\text{m}$  pitch pixel. A charge sensitive amplifier integrates the input charge signal on a 40fF feedback capacitor, along with a current source feedback for discharging. The CSA is decoupled for the sensor leakage path with capacitor CC. The subsequent ac coupled comparator produces the time over threshold pulse whose duration is not measured digitally in the pixel. Instead, it drives a time to voltage converter, whose output is transferred to the array periphery and digitized in the same way as the low gain version. The high gain pixel power consumption is approximately 8 $\mu\text{A}$  when idle, with the option of increasing/decreasing this number according to requirements.

The arrays designed and fabricated are 16 x 16 for the low gain and 32 x 32 for the high gain. The low gain array consists of pixels with dimensions 200 x 200  $\mu\text{m}^2$  and it can process signals in the range from 40 fC to 9 pC. The high gain array has pixels with 100  $\mu\text{m}$  pitch and it can process signals from 0.5 fC up to 50 fC. The gains of the two pixels are shown as a function of the dynamic range in Fig. 2.

ASIC / 121

## Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

**Author:** Chiara Ferrero<sup>1</sup>

<sup>1</sup> *Universita e INFN Torino (IT)*

**Corresponding Author:** chiara.ferrero@cern.ch

During the next LHC Long Shutdown, the innermost three layers of the ALICE Inner Tracking System will be replaced by a new vertex detector composed of curved ultra-thin monolithic silicon sensors. The R&D initiative on monolithic sensors of the CERN Experimental Physics Department, in synergy with ALICE ITS3 upgrade project, prepared the first submission of chip designs in the TPSCo 65 nm technology, called MLR1. It contains four different test structures: CE-65, DPTS, APTS-SF and APTS-OPAMP, with different process splits and pixel designs. This work illustrates the validation of the technology in terms of pixel performance and radiation hardness.

**Summary (500 words):**

Monolithic Active Pixel Sensors (MAPS) embed integrated front-end electronics in the same silicon volume that constitutes the sensing substrate. A new vertex detector composed of curved,  $\leq 50 \mu\text{m}$  thin monolithic silicon sensors will be installed during the LHC LS3 to replace the innermost three layers of the ALICE Inner Tracking System at CERN.

In particular, the MLR1 (Multi Layer per Reticle) submission foresees to validate the Tower Partner Semiconductor Co. 65 nm ISC technology, in which the same principles of process optimization as in 180 nm technology have been applied. Three main pixel designs have been implemented: standard, modified (B) and modified with gap (P). In particular, the P-type combines the advantages of a small collection



electrode, as a few fF sensor capacitance, with a fully depleted epitaxial layer, thanks to a low dose deep n-type implant, placed below the wells containing the circuitry. Four different pixel test structures, all measuring 1.5 mm by 1.5 mm were designed to validate the sensor technology: Circuit Exploratoire 65 (CE65), consisting of 64x32/48x32 matrices featuring pixel pitches of 15 and 25  $\mu\text{m}$  respectively, Digital Pixel Test Structure (DPTS), a matrix of 32x32 pixels with 15  $\mu\text{m}$  pitch, including a full digital front-end within each pixel, Analogue Pixel Test Structure - Source Follower (APTS-SF) and Analogue Pixel Test Structure - Operational Amplifier (APTS-OPAMP).

The APTS consists of a 6x6 pixel matrix, of which only the central 4x4 pixels are read out. It features two types of output buffers: source follower or a high speed Operational Amplifier (OPAMP), the latter providing a better timing performance. The pixel pitches range from 10 to 25  $\mu\text{m}$ .

In this talk, the main results of the test structures characterisation from the MLR1 submission will be presented. In particular, testbeam results on the CE-65 have shown that, as expected, in the modified process all the charge is mostly collected by a single pixel.

Subsequently, the effect of different irradiation levels on the DPTS chip detection efficiency, on the sensor spatial resolution and average cluster size will be illustrated. In-beam measurements have demonstrated the 99% detection efficiency for a chip irradiated up to  $10^{15}$  1 MeV  $\text{neq cm}^{-2}$  and 100 kGy at +20 °C, while preserving a low fake-hit rate of  $< 10 \text{ pixel}^{-1} \text{ s}^{-1}$ , thus reaching the goals of detection efficiency and non-ionising and ionising radiation hardness up to the expected levels for ALICE ITS3, below  $1 \times 10^{13}$  1 MeV  $\text{neq cm}^{-2}$  (NIEL) and 10 kGy (TID).

Finally, the major results obtained on the OPAMP test structure will be explored: an intensive characterization with a 55Fe source has demonstrated promising performance in terms of charge collection for the optimized sensor, with suppression of slow events with respect to the standard one and from the testbeam, a time resolution of  $77 \pm 5$  ps has been measured.

To conclude, the characterisation of the test structures from the MLR1 submission has been carried out in various laboratories and testbeam facilities and has revealed the excellent performance of the R&D campaign.

## Programmable Logic, Design and Verification Tools and Methods / 123

### SystemC framework for architecture modelling of electronic systems in future particle detectors

**Authors:** Adithya Pulli<sup>1</sup>; Davide Ceresa<sup>1</sup>; Francesco Enrico Brambilla<sup>2</sup>; Jashandeep Dhaliwal<sup>1</sup>; Kostas Kloukinas<sup>1</sup>; Stefano Esposito<sup>1</sup>; Xavi Llopart Cudie<sup>1</sup>

<sup>1</sup> CERN

<sup>2</sup> EPFL - Ecole Polytechnique Federale Lausanne (CH)

**Corresponding Author:** [davide.ceresa@cern.ch](mailto:davide.ceresa@cern.ch)

The prototyping cost in advanced technology nodes and the complexity of future detectors require the adoption of a system design approach common in industry: design space exploration through high-level architectural studies to achieve clear and optimized specifications.

This contribution proposes a configurable SystemC framework to simulate the readout chain from the front-end chips to the detector back-end. The model is transaction accurate, includes an event generator and interfaces with real physics events, and provides metrics such as readout efficiency, latency, and average queue occupancy.

This contribution details the structure of the framework and describes a case study based on Velopix2.

#### Summary (500 words):

The CERN EP department has launched a strategic R&D programme on technologies for future experiments. In this context, the IC technology work package, namely WP5, is working on the development of a simulation framework for architectural modelling of future particle detectors.

This work focuses on the modelling of pixel-based detector from front-end to back-end at a high level of abstraction to perform architectural studies. The objective is to study the readout network efficiency as well as to provide the metrics to compare different solutions to satisfy functional and non-functional requirements, such as data throughput, data quality, downlink material cost, and other parameters both

detector-wise and at ASIC level. At the same time, it can provide a reference model for HDL code design and verification. For this reason, an important feature is support for co-simulation of the high-level architectural model and the RTL model.

The framework proposed in this contribution is built in SystemC, a system-level specification and design language based on C++ classes that has been widely adopted in industry for high-levels of abstraction modelling, such as system-level simulations. The SystemC language is open-source, supports TLM2.0 standard, allows RTL co-simulation and can be integrated with UVM-based verification environments, and is developed by a wide consortium of companies in several industrial domains, most prominently computer aided design (CAD) companies.

The framework provides two main component modules: a layer and a network. The layer module contains the processing logic, whereas the network module instantiates the connectivity among different layer modules. This structure enables code re-use while writing models for different systems. Information transmission is modelled via packet transfer, where a packet represents the data that the system is processing. An example would be hit data transferred in a pixel chip. Packet transfers are based on TLM2.0 sockets providing different abstraction levels depending on the needs of the project. The stimuli can be internally generated with full control on event occupancy, cluster size and shape, and any other data characteristic, therefore allowing parametrized studies. On the other hand, the framework also provides methods to interface with externally generated events to assess performance with data deriving from physics-level detector simulations.

The first study case for the proposed framework was the Velopix2 LHCb detector. In this context, the front-end chip design team is developing a chip architecture able to cope with pixel rates up to 350 kHz/pixel. The initially proposed architecture has been modelled and simulated with physics data proving that the readout architecture was unable to provide sufficient readout efficiency. The framework enabled collection of metrics to be used in a per-layer bottleneck analysis based on average queue occupancy and packet transfer rate. Such analysis revealed the limitations of the initially proposed architecture and how to revise it.

In conclusion, the proposed framework provides a tool for early architectural analysis, helping both front-end chips designers and system developers to have a comprehensive view of the performance of the detector under development as well as a consistent reference model for the RTL development and verification.

#### Thursday posters session / 124

### FastRICH: a readout ASIC with precise time stamping for the LHCb RICH detector

**Author:** Andrea Paterno<sup>1</sup>

**Co-authors:** Adithya Pulli<sup>1</sup>; Carmelo D'Ambrosio<sup>1</sup>; David Gascon<sup>2</sup>; Floris Keizer<sup>1</sup>; Franco Nahuel Bandi<sup>1</sup>; Jan Kaplon<sup>1</sup>; Joan Mauricio<sup>2</sup>; Michael Campbell<sup>1</sup>; Rafael Ballabriga Sune<sup>1</sup>; Rafel Manera Escalero<sup>2</sup>; Sergio Gomez Fernandez<sup>2</sup>

<sup>1</sup> CERN

<sup>2</sup> University of Barcelona (ES)

**Corresponding Author:** andrea.paterno@cern.ch

The FastRICH is a readout chip designed by CERN and the University of Barcelona for the LS3 enhancements and the Upgrade II of the LHCb RICH detector. The 16-channel radiation-hard FastRICH will be capable of reading out MAPMTs, MCPs, and SiPMs, with peak hit rates up to 40MHz. The low-power readout, with 4 lpGBT/VTRx-compatible 1.28GHz SLVS output links, is optimized for bandwidth reduction, allowed by the use of a Constant Fraction Discriminator for timewalk compensation, a programmable hardware shutter, and a custom readout protocol. Preliminary simulations show ~7ps timing resolution, with a total power consumption of <10mW per channel.

#### Summary (500 words):

The FastRICH is a readout chip that is being designed in the framework of the upgrade of the LHCb RICH detector to be installed during the LHC LS3. As the arrival of the Cherenkov photons to the photodetectors in the system can be predicted highly accurately, a fast timestamp of the hit improves

accordingly the signal-to-noise ratio, pattern recognition, and particle identification performance, which would be critical in the foreseen  $10^{34}\text{cm}^{-2}\text{s}^{-1}$  luminosity and high detector occupancy resulting from multiple primary vertices.

FastRICH builds on the experience of the design of the FastIC ASIC, designed by CERN and the University of Barcelona: an 8-channel generic detector readout ASIC that provides accurate timestamping and linear energy measurements of detected particles, and that is currently under an extensive campaign of measurements in order to evaluate its performance under the foreseen LHCb RICH conditions, with average hit rates ranging from 0.1MHz to 12.5MHz/channel.

FastRICH contains 16 channels designed with radiation-hardened electronics. The analog circuit is based on the analog front end of FastIC and will be capable of reading out MAPMTs during LHC Run4. Additionally, the ASIC will be able to read out candidate detectors for operation in Run 5, such as SiPMs and MCP-based sensors, with peak single-photon hit rates of up to 40MHz/channel. The FastRICH analog channel includes a Constant Fraction Discriminator to compensate for timewalk, which eliminates the need for off-chip post-processing, and consequently of measuring and sending out the energy information of the signals. Preliminary simulation results including the front-end and CFD circuit show an electronics jitter  $<40$  ps rms for detector signals above 50uA, with a CFD residual timewalk of  $<150$ ps peak-to-peak for signals over the full 30uA-2mA range, which gets significantly reduced for signals over a smaller range.

The Time-of-Arrival (ToA) of incident photons will be measured with a  $\sim 25$ ps time bin Time-to-Digital Converter (TDC), which can be programmed in a  $\sim 50$ ps time bin mode. In normal operation, FastRICH will send only timewalk-corrected ToA information. A special mode with the leading-edge comparator ToA and high-resolution Time-over-Threshold (ToT) will also be supported, in order to debug and characterize the system performance.

Out-of-time background and sensor noise are filtered by a programmable hardware shutter, which allows selecting the signals of interest in a timing window that is foreseen to be in the order of a few ns per Bunch Crossing (BX), thus reducing the output data bandwidth. Data at a given BX is zero-suppressed and encoded in variable-length packets, which will in turn be transmitted by lpGBT/VTRx-compatible SLVS output links, which provide the chip a total maximum output bandwidth of up to 5.12Gbps. A framing protocol ensures DC balancing and link self-recovery in case of readout errors. The number of active output links is configurable so that the chip can be optimized to operate in regions in the experiment with different occupancy.

The purpose of this presentation is to present a detailed description of the FastRICH chip architecture, design status, and expected performance.

**Tuesday posters session / 125**

## **The status of the Back-end card for the JUNO experiment**

**Author:** Feng Gao<sup>1</sup>

**Co-authors:** Barbara Clerbaux<sup>1</sup>; Marta COLOMER<sup>1</sup>; Pierre-Alexandre Petitjean<sup>1</sup>; Yifan Yang<sup>2</sup>; Yifan Yang<sup>1</sup>

<sup>1</sup> *iihe, ULB*

<sup>2</sup> *Universite Libre de Bruxelles (BE)*

**Corresponding Authors:** yifan.yang@cern.ch, feng.gao@ulb.be

The Jiangmen Underground Neutrino Observatory (JUNO) aims to determine the neutrino mass hierarchy by detecting antineutrinos from nuclear reactors using a large liquid scintillator volume. The detector uses around 20,000 20-inch photomultiplier tubes powered and read out by two electronics readout systems: underwater and above water. The back-end card (BEC) is a crucial component of the latter and links 7,000 underwater electronics boxes to the trigger system. 180 BECs have been installed and tested at the JUNO site, including self-tests and combined tests. This presentation reports on the current status of the BEC and on the various test results.

**Summary (500 words):**

The Jiangmen Underground Neutrino Observatory (JUNO) is currently under construction in a 700 m deep underground laboratory in Guangdong province, China. Its main goal is to determine the mass hierarchy of neutrinos using electron antineutrinos from two nuclear power plants (8 reactor cores). With a target mass of 20 kt of liquid scintillator, JUNO will also be able to detect neutrinos from various other sources such as the Earth, the Sun, the atmosphere, and supernovae.

To achieve these physics goals, JUNO employs a system of 17612 20-inch PMTs and 25600 3-inch PMTs to detect light produced when particles deposit energy in the liquid scintillator. The PMT electronics can be divided into two parts: the front-end electronics system performing analog signal processing under water (UW), and the back-end electronics system which consists of the DAQ and the trigger sitting outside water.

A scheme of the Large-PMT readout electronics is presented. The back-end card (BEC) is a crucial component of JUNO's back-end electronics system and plays an important role in the trigger and clock system. It functions as a concentrator to collect and compensate incoming trigger request signals. A Trigger/Timing Interface Mezzanine (TTIM) handles all the trigger request signals, and the hit signals from the various BECs are sent to Reorganize & Multiplex Unit (RMU) cards. The sum of the signals is then forwarded to the Central Trigger Unit (CTU), which makes the trigger decision based on the trigger logic and sends it to the Global Control Unit (GCU) via the RMU and the BEC.

160 BECs are needed for the JUNO main detector, and 2 BEC for the sub-system: The Online Scintillator Internal Radioactivity Investigation System (OSIRIS) and the Taishan Antineutrino Observatory (JUNO-TAO). All BECs have been tested and installed at the JUNO site. This presentation reports on the BEC current status and the various test results including both direct and indirect tests. A transmission error mass test was completed in Kunshan after production, and an underground test was done after installation. All BECs passed the tests. A long-term monitoring of all BECs was conducted to check their work status, with each run taking 48 hours and lasting a period of 1 month. After the partial installation of PMTs and UW boxes, a joint test with LPMT/sPMT + electronics + trigger + DAQ + DCS was performed using a BEC-level trigger, which provided a good result for the trigger system and data acquisition system.

ASIC / 126

## Design and Characterization of a precision tunable time delay integrated circuit.

**Author:** Yahya Tousi<sup>None</sup>

**Co-authors:** Akshay Naik ; Diba Dehmeshki <sup>1</sup>; Erich Frahm <sup>2</sup>; Roger Rusack <sup>3</sup>; Rohith Saradhy <sup>3</sup>

<sup>1</sup> *The University of Minnesota*

<sup>2</sup> *University of Minnesota*

<sup>3</sup> *University of Minnesota (US)*

**Corresponding Author:** ymtousi@umn.edu

Authors:

Akshay Naik, Erich Frahm, Roger Rusack, Diba Dehmeshki, Rohith Saradhy, Yahya Tousi

We present a design of a time delay circuit that we have developed for future applications in particle physics experiments. Our circuit has a dynamic range of 250 ps achieved in steps of 270 fs. The chip was fabricated in TSMC's 65 nm LP process and consists of an array of planar waveguides for fine control and LC lumped circuits for large scale delays. We will report on detailed characterization of the device including some recent results from radiation tests.

**Summary (500 words):**

Precision timing measurements is and will be a major tool at the HL-LHC and at future high energy facilities. The requirement of precision clock distribution and stabilization will be a major challenge as we extend our physics requirements to the picosecond or sub-picosecond levels. We have developed an integrated dual channel digitally controlled phase shifter circuit with a step size of  $\sim 270$  fs and a dynamic range of  $\sim 250$  picoseconds. The concept we use in this design is based on tunable delay-line phase shifters first used for developing accurate beam control in large scale arrays for 5G mm-wave base stations. In this work we have adopted this core technique and transformed it into an architecture that fits the needs of precision time delay. Fine delay precision and large dynamic range are typically at odds as one requires fine unit cells and stacking a large number of them for dynamic range comes at the cost of unbearable signal attenuation and area. To address this trade-off we incorporate a two-tier tuning mechanism that enables both high precision and large dynamic range. First, a coarse set of delay cells biases the delay within the range close to the target delay value. Next, a set of transmission line-based delay lines fine-tune this delay with sub-picosecond delay steps and produces the target delay within  $< 270$  fs of accuracy. We designed and fabricated a prototype of this tunable delay line in the TSMC 65nm LP process. The chip area is  $1\text{mm} \times 1.9\text{mm}$  and consists of two tunable delay lines and a radiation tolerant I2C interface for digital control of the delay cells. The passive construction of the delay line creates delay values that primarily depend on the physical distances between metal structures on chip. Such distances can be accurately fabricated with nano-scale accuracy resulting in reliable and accurate delay values. The passive nature of this delay line also has the benefit of zero DC power. There is good agreement between EM simulation results of the delays and board level delay measurements of the fabricated chip. We will report on results obtained with this device, that include linearity, signal quality, dispersion, and radiation tolerance. The attached image shows our measurements of the fine delay steps.

**Tuesday posters session / 127**

## **DC Power Circuit Evaluation for the Development of the Barrel Calorimeter Processor V2**

**Author:** Stephen Goadhouse<sup>1</sup>

**Co-author:** Nikitas Loukas<sup>2</sup>

<sup>1</sup> *University of Virginia (US)*

<sup>2</sup> *University of Notre Dame (US)*

**Corresponding Author:** [stephen.david.goadhouse@cern.ch](mailto:stephen.david.goadhouse@cern.ch)

The development of the CMS Barrel Calorimeter Processor (BCP) for the high-luminosity LHC poses a challenge due to strict power requirements. To minimize the risk of performance degradations or component damage, a project-specific and inexpensive evaluation board has been designed with multiple DC power circuits to safely test and evaluate them outside of the expensive BCP. The planned tests will verify several operating parameters of the power circuits, including output voltage, ripple voltage, and transient load. We will report on the results of these tests along with any roadblocks, their solutions, and lessons learned from this investigation.

### **Summary (500 words):**

For the high-luminosity LHC (HL-LHC), a new back-end electronic board, the Barrel Calorimeter Processor (BCP), is being developed to support the CMS barrel calorimeters. The BCP is an ATCA-based board with very challenging power requirements, including a FPGA core voltage of 0.85V with a strict valid range of  $\pm 25\text{mV}$  while supporting up to 160A of current, and voltages for the FPGA multi-gigabit transceivers (MGT) of 0.9V, 1.2V and 1.8V with a maximum allowable noise of 10 mVpp. Additionally, the multiple optical transceivers, or FireFly, require 1.8V, 3.3V and 3.75V with maximum low noise requirements of either 30 mVpp or 50 mVpp depending on the model. Failure to meet these power requirements threatens performance degradations and could even damage expensive components such as the FPGA and FireFly which would be a costly outcome in both time and money.

To minimize the risk, we propose creating a project-specific evaluation board that includes the chosen DC power circuits and uses layout techniques required by the BCP design. This evaluation board will

include multiple circuits to also evaluate any possible negative interactions such as thermal or input voltage noise that negatively impact performance. This approach is more accurate than using a manufacturer's evaluation board because those are often designed and optimized for trade-offs that benefit the manufacturer and may not be suitable for our application.

Several tests are planned for the circuits on the custom evaluation board, including verifying the output voltage range under typical and maximum loads and verifying that the ripple voltage remains under 75% of the maximum specification. A transient load test will be performed to verify that the output voltage remains within the specified ranges during transients. A voltage ramp test will confirm that the FPGA voltages all rise to 95% of the nominal voltage within 0.2 to 40 ms. An integration test will load all circuits to verify that the circuits remain under thermal limits and that there are no negative impacts between circuits that may increase ripple voltage on the common input voltage.

Based on the results of the tests, circuit modifications may be performed if there are failing circuits, and then the modified circuits will be retested. In the case of multiple circuits for a single supply, the circuit that best meets specifications will be selected. The presentation will describe the power circuits and discuss the test results, comparing them against the specifications. Any problems encountered, along with circuit modifications and other solutions, will also be examined. This approach will ensure that the BCP meets the challenging power requirements for the HL-LHC and avoids any performance degradations or expensive loss of time or money.

**Tuesday posters session / 128**

## **Integration of EDWARD readout architecture in full-field fluorescence imaging detector**

**Authors:** Dominik Gorni<sup>1</sup>; Gabriella Carini<sup>1</sup>; Grzegorz Deptuch<sup>1</sup>; Anthony Kuczewski<sup>1</sup>; Soumyajit Mandal<sup>1</sup>; Giovanni Pinaroli<sup>1</sup>; Abdul Rumaiz<sup>1</sup>; D. Peter Siddons<sup>1</sup>; Nicholas St. John<sup>1</sup>

<sup>1</sup> *Brookhaven National Laboratory*

**Corresponding Author:** dgorni@bnl.gov

Data bandwidth, timing resolution and resource utilization in readouts of radiation detectors are constantly challenged. Event driven solutions are pushing against well-trenched framed solutions. The idea for an asynchronous readout architecture called EDWARD (Event-Driven With Access and Reset Decoder) was presented at the TWEPP 2021 conference. Here we show the progress of our work which resulted in two chip prototypes. The first one is a full device with analog pixel circuitry suited for full-field fluorescence imaging, and the second one contains digital pulse generators with Poisson-exponential distribution in each pixel for extraction of the performance matrix of EDWARD alone.

**Summary (500 words):**

The EDWARD readout architecture [1], allows efficient readout of data from a chip with multiple data sources e.g., pixelated detectors. The architecture is distinguished by the fact that it works in a fully asynchronous manner i.e. the readout request can occur at any time and the arbitration between requests is devoid of priority [2]. These features eliminate the need to use the frame clock to snapshot the state of the matrix, which would be necessary to avoid switching between channels during a readout. This functionality of the EDWARD architecture is achieved thanks to arbitration based on a binary tree, the basic unit of which is an arbiter based on the Seitz arbiter structure [3]. Other advantage of the EDWARD architecture is automatic synchronization to an external clock provided, for example, by an acquisition module, which allows the chip to send data out using a standard communication protocol. The described architecture has been incorporated into the CTR (Configuration, Testability, Readout) platform and implemented in two different chip prototypes in 65nm CMOS technology. The platform is extremely modular and allows for easy scaling. The first prototype is a radiation detector named 3FI65P1 (Fig. 1.) suited for full-field fluorescence imaging. It is a hybrid 5mm x 5mm detector containing a 32x32 pixel matrix with a 100um pitch. The matrix is built in a modular fashion with 16 groups (4x4), each consisting of 64 pixels (8x8). It has been implemented as Analog-on-Top with digital logic placed between pixels in a group and between groups in the matrix. The main elements of the CTR

platform are located in the group logic space (density  $\sim 84\%$ ), while the space between groups mainly contains part of the arbitration tree between groups (density  $\sim 2\%$ ) and the shared bus. All groups are connected to the shared 14-bit digital data bus, on which the address of the pixel being read out is sent, and 1 analog line, on which the analog value of the peak from the front-end peak detector is sent. The digital data is serialized and sent off-chip. Serialization is performed based on externally supplied clock with a designed frequency of 250MHz. The chip has a built-in clock divider by 14, which acts as the serializer frame clock and determines the time intervals for channel access to shared resources. This gives a maximum pixel data readout rate of 17.86MHz. The divided clock can alternatively be provided from an external source. Such a clock with a variable duty cycle will be used to observe its impact on build-in asynchronous-to-synchronous synchronization. The second prototype is based on the skeleton of the first, maintaining its dimensions. In this prototype analog front-end circuitry is replaced by digital logic (Fig. 2.) containing pulse generator with Poisson-exponential distribution [4]. This structure will allow even better study of the temporal properties of the EDWARD architecture – timing resolution, latency, maximum acceptable rate, and the signal integrity of the received data thanks to the ability to programmatically change the rate at which readout requests are generated.

Thursday posters session / 129

## Mu2e calorimeter readout electronics: design, characterisation, and radiation hardness

Author: Daniele Paesani<sup>1</sup>

<sup>1</sup> LNF-INFN

Corresponding Author: daniele.paesani@lnf.infn.it

The Mu2e CsI crystal calorimeter has high granularity, 10% energy and 500 ps timing resolution for 100 MeV electrons, and will achieve extremely high levels of reliability and stability and in a harsh operating environment. Each crystal is readout by two custom UV-extended SiPMs, with independent readout channels, coupled to custom front-end electronics boards, to provide individually programmable bias voltages, perform signal amplification and shaping, while monitoring currents and temperatures. The FEE design was validated for operation in high-vacuum and under 1T B-field. An extensive radiation-hardness campaign certified the FEE design for ionizing dose, displacement damage dose and single-event effects.

### Summary (500 words):

The Mu2e experiment at Fermi National Accelerator Laboratory will search for charged-lepton flavour violating neutrino-less conversion of negative muons into electrons in the coulomb field of an Al nucleus. The conversion electron has a monoenergetic 104.967 MeV signature slightly below the muon mass and will be identified by a complementary measurement carried out by a high-resolution tracker and an electromagnetic calorimeter (EMC), reaching a single event sensitivity of about  $3 \times 10^{-17}$ , four orders of magnitude beyond the current best limit. The calorimeter, composed of 1348 pure CsI crystals arranged in two annular disks, has high granularity, 10% energy resolution and 500 ps timing resolution for 100 MeV electrons and will need to maintain extremely high levels of reliability and stability and in a harsh operating environment with high vacuum, 1 T B-field and high radiation exposures.

Each crystal is readout by two custom UV-extended SiPMs (Mu2e-SiPM), each one corresponding to a separate readout channel. Each Mu2e-SiPM is coupled to a custom front-end electronics (FEE) board, mounted directly behind the SiPM, which will provide individually programmable bias voltages for each photosensor, perform signal amplification, while monitoring currents and temperatures. Each Mu2e-SiPM is composed of 6 individual cells, wired in two parallel connections of three elements each. Two fast, low-input impedance transimpedance stages combine SiPM pulses and feed them to a buffer stage, which in turn drives a pole-zero compensator, followed by a pulse stretching stage comprising a 3-pole Bessel filter, guaranteeing more than 5 sampled points on the rising edge available to the 250 Msp/s digitizer boards. A final balanced differential driver transmits the signals to the digitizing section. The FEE has selectable gain (2 or 4). A pulsed green laser is distributed via fiber optic to each Mu2e-SiPM to perform gain equalization. Each FEE will also handle all slow control functions via an SPI bus, by

implementing a high-voltage, high stability linear regulator with local DAC, and readout systems for SiPM bias, temperature, and current monitoring.

The FEE design was validated for operation in vacuum and under magnetic fields. An extensive radiation hardness certification campaign, carried out with photons from Co-60, 14 MeV neutron beams, and 200 MeV protons certified the FEE design for doses up to 100 krad, neutron fluences up to 1012 n1MeV/cm<sup>2</sup> and for single-event effects occurrences and correction. Dedicated latchup-safe power supervising circuits were embedded in the design to automatically correct fault conditions.

**Thursday posters session / 130**

## **The Analog Front End for FastRICH: an ASIC for the LHCb RICH Detector Upgrade**

**Authors:** Rafel Manera Escalero<sup>1</sup>; Rafel Manera Escalero<sup>1</sup>

**Co-authors:** Rafael Ballabriga Sune<sup>2</sup>; Joan Mauricio<sup>1</sup>; Jan Kaplon<sup>2</sup>; Andrea Paterno<sup>2</sup>; Franco Nahuel Bandi<sup>2</sup>; Sergio Gomez Fernandez<sup>3</sup>; Adithya Pulli<sup>2</sup>; Sara Portero<sup>4</sup>; Juan J. Silva<sup>4</sup>; Floris Keizer<sup>2</sup>; Carmelo D'Ambrosio<sup>2</sup>; Michael Campbell<sup>2</sup>; David Gascon<sup>1</sup>

<sup>1</sup> *University of Barcelona (ES)*

<sup>2</sup> *CERN*

<sup>3</sup> *Serra Hunter Fellow UPC*

<sup>4</sup> *University of Barcelona (UB)*

**Corresponding Authors:** rafel.manera.escalero@cern.ch, rafelmanera@icc.ub.edu

This work presents the analog circuitry of the FastRICH ASIC, a 16-channel ASIC, developed in a 65 nm CMOS technology specifically designed for the RICH detector at LHCb to readout a wide range of detectors like Photomultiplier Tubes, to be used at the LHC Run 4 or SiPMs, candidates for Run 5. The front-end (FE) stage has an input impedance ( $Z_{in}$ ) below 50  $\Omega$  and an input dynamic range from 5  $\mu$ A to 5 mA with a power consumption of  $\sim$ 5 mW/channel. The chip includes a Constant Fraction Discriminator (CFD) and a Time-to-Digital Converter (TDC) for digitization.

**Summary (500 words):**

The increase in luminosity during HL-LHC Run 5 causes a challenging rise in particle multiplicity and hit occupancy also for the RICH subsystem. The increased irradiation level dictates a shift in the electronics from FPGAs to a more radiation-hard ASIC with a time resolution of better than 100 ps in order to keep the high particle ID performance after the Upgrade II. The FastRICH ASIC is under development in a 65 nm CMOS technology specifically designed for the RICH detector at the LHCb experiment. It builds on the experience with the FastIC ASIC and adds specific characteristics required for the RICH detector such as: (1) a Constant Fraction Discriminator (CFD) to minimize time walk variations and avoid the need to send the time-over-threshold information to correct for pile-up, reducing the amount of output data; (2) a Time-to-Digital Converter (TDC) to digitize the data; (3) a digital zero suppressed readout circuit; and (4) programmable output links for data transmission. The chip is radiation tolerant by design and the power consumption per channel is  $\sim$ 5 mW.

This work presents the analog circuitry of the FastRICH ASIC. The Front-End (FE) stage processes the input signal in current mode with an input impedance ( $Z_{in}$ ) below 50  $\Omega$  and an input dynamic range from 5  $\mu$ A to 5 mA. It is programmable to work with positive or negative input polarity signals delivered by low capacitance sensors with intrinsic amplification, such as Photomultiplier Tubes (PMT), small area (1x1 mm<sup>2</sup>) Silicon Photomultipliers (SiPM), or Microchannel Plates (MCP). Thus, this ASIC is suitable for the readout of MAPMTs in LHC Run 4 and the candidate SiPMs during Run 5. The FE consists of two complementary (positive and negative polarity) input stages based on a high performance unity gain current mirror with two control feedbacks. The Low Frequency Feedback (LFF) adjusts the input DC voltage with a range of adjustment of  $\sim$ 400 mV to compensate for SiPM gain variations locally. A DC Level Shifter allows a larger input voltage adjustment range. The High Frequency Feedback (HFF) maintains  $Z_{in}$  low at high frequencies. The most susceptible analog blocks are designed with Enclosed Layout Transistors (ELT) to improve its radiation tolerance.

Time-of-Arrival measurement is generated through a CFD. In addition, the ASIC will also provide a



nonlinear Time Over Threshold (ToT) energy signal through a Leading-Edge Discriminator (LED) for calibration purposes. Simulations results regarding time walk are  $<150$  ps for the CFD and  $<1.6$  ns for the LED. CFD (and LED, optionally) binary output signal will be digitized on-chip by means of a TDC with adjustable time bin,  $\sim 25$  ps for the high-performance mode or  $\sim 50$  ps for the low-power mode. The digital circuitry will be implemented using Triple Modular Redundancy (TMR) to improve radiation tolerance.

**Tuesday posters session / 135**

## **MIMOSIS2 validations using Cadence Protium platform and its Black Box flow**

**Authors:** Claude Pierre Colledani<sup>1</sup>; Frederic Morel<sup>1</sup>; Gilles Lucien Claus<sup>1</sup>; Gregory Bertolone<sup>1</sup>; Matthieu SPECHT<sup>2</sup>

<sup>1</sup> *Centre National de la Recherche Scientifique (FR)*

<sup>2</sup> *Université de Strasbourg / CNRS / IPHC*

**Corresponding Author:** gregory.bertolone@cern.ch

FPGA prototyping enables hardware acceleration for ASIC verification. Cadence Protium, an FPGA based platform, enables ASIC designers to prototype their RTL code in an easy and automatically way. As the RTL codes stay untouched during the process, the Protium provides a reliable model of the ASIC for early developments of DAQ and control systems. Protium advanced Blackbox flow allows in addition using external FPGA IP and running parts of the design at much higher speeds than what can be achieved by standard Protium flow. Its role in the validation of MIMOSIS2, an ASIC developed for CBM experiment, will be presented.

### **Summary (500 words):**

MIMOSIS2 is a full reticule size ( $31 \times 17$  mm<sup>2</sup>) monolithic pixel sensor prototype developed for the vertex detector of the CBM experiment (FAIR/GSI). It integrates a matrix of over  $\frac{1}{2}$  million pixels with Priority Encoders inside each column and a sparse data readout. The slow control, the steering logic and the clocks trees have been fully triplicated to match the radiation hardness requirement of the experiment (100 kGy). The ASIC control is driven by an I2C module and the data transmission is done by up to height 320 MHz LVDS pads. Compared to MIMOSIS1, a new data clusterisation feature have been implemented.

Cadence Protium is a prototyping solution based on hardware environment (mainly Xilinx Ultrascale VU440 FPGA) with dedicated software. Users do not need neither to adapt their RTL code neither to have FPGA knowhow. The Protium compiler generates scripts, which allow designers to perform automatically the FPGA synthesis and the Place and Route steps. The ASIC verification can be done with test bench running inside the Protium environment hardware or by connecting the prototype to external systems.

MIMOSIS2 digital periphery has been successfully prototyped inside a Protium S1. This implementation enables on the one hand the validation of the ASIC. The correction of a bug found in the MIMOSIS1 I2C watchdog has been checked easily and quickly (less than one hour). On the other hand, the Protium facilitates the early and robust development of the upgrades of MIMOSIS1 data acquisition (DAQ) and control systems, months before the chips comes back from foundry.

To enable an automatically implementation of the ASIC inside the Protium FPGA, the Protium compiler adds an extra hardware overlay to the ASIC RTL code. This introduces a timing limitation on the frequency at which the design will run inside the FPGA and communicate with the outside world. For MIMOSIS2, prototyped inside our Protium with a standard flow, the output data rate drops down to around 10 MHz. It is less than the nominal ASIC data output frequency (320 MHz), but user can perform ASIC functional verification at higher speed than using software simulation. It enables also the functional verification of the dedicated DAQ.

To solve this speed issue, we use the Protium BlackBox methodology. This advanced Protium flow allows splitting the Protium FPGA resources in two parts:

- the ASIC RTL code and the Protium overlay, running at lower frequency (10 MHz for MIMOSIS2);
- a BlackBox module which could be any IP (like PLL, ETHERNET or AXI USB module...) or custom designs (like accelerator modules or FPGA firmware of a DAQ), running at high FPGA frequency.

For MIMOSIS2, a dedicated FIFO was developed and used as a BlackBox. Acting as a gearbox between

the slow clock domain of the MIMOSIS2 Protium model and the fast clock domain of the data acquisition system, this BlackBox allows us to speed up the data transmission within Protium to the nominal ASIC frequency.

Tuesday posters session / 136

## Magnetic resilience studies for power supplies

**Authors:** Alessandro Iovene<sup>1</sup>; Ferdinando Giordano<sup>None</sup>; Simone Ivo Selmi<sup>None</sup>

<sup>1</sup> CAEN SpA

**Corresponding Authors:** [ferdinando.giordano@cern.ch](mailto:ferdinando.giordano@cern.ch), [s.selmi@caen.it](mailto:s.selmi@caen.it), [a.iovene@caen.it](mailto:a.iovene@caen.it)

In this poster we present our approach to design power supplies that are resilient to magnetic field that can reach up to 1 T, we will illustrate the engineering challenge to have a power supply that can safely operate in radiation and magnetic fields. We will summarize the test we have performed starting from basic components like inductors, then sub-parts and complete modules. We will illustrate the use case of the BRIC1 used by ATLAS-NSW as DC-DC intermediate converter stage and summarize its performance.

### Summary (500 words):

It's well known that modern physics experiments require higher LV power to be delivered to the front-end electronics with respect to the past, this is efficiently done by placing the LV power supplies as close as possible to the detector. Unfortunately, this means that they must be robust against radiation and resilient to the magnetic fields often present to measure particles properties.

Experimental caverns place restraints on the design of the power supplies and various standards must be respected, but most important are the functionalities needed to properly operate the detectors during their lifecycle.

Designing a power supply for such specific needs it is not a trivial task, once the contour conditions are well understood the executive design can start, but before even drawing a circuit it is mandatory to decide the design approach to the power supply and what components to use. Since the peculiar environment, the components have to be carefully selected and tested, like measuring the magnetic properties of inductors and how they change according to an external magnetic field.

Once this step is completed and the design has started then some sub-part can be tested, the circuits should efficiently work at  $B = 0$  T and to cope with increasing magnetic fields up to 1 T, to assure this we have performed also tests at this phase. The last phase is, of course, the testing of a whole power supply in an operational environment.

In this work we will explain the engineering challenge to have a power supply that can safely operate in radiation and magnetic fields, and how we have tackled it. We will summarize the results we have obtained during the tests we have performed during the three abovementioned phases, in order to give a complete picture of the development of the CAEN EASY BRIC1, an intermediate convertor now used by ATLAS-NSW to power the front-end electronics with 12 V starting from 300 V.

Radiation-Tolerant Components and Systems / 138

## CERN Radiation Hardness Assurance: Challenges and Solutions for Large-Scale Distributed System Exposed to High-Energy Particle Accelerator Environments

**Authors:** Alessandro Zimmaro<sup>1</sup>; Rudy Ferraro<sup>2</sup>

**Co-authors:** Alessandro Masi<sup>2</sup>; Jerome Boch; Ruben Garcia Alia<sup>2</sup>; Salvatore Danzeca<sup>2</sup>; frederic saigne

<sup>1</sup> *Universite Montpellier II (FR)*

<sup>2</sup> *CERN*

**Corresponding Author:** alessandro.zimmaro@cern.ch

The electronic systems at CERN, exposed to the harsh radiation environments of particle accelerators and experiments, require specific qualification procedures to ensure reliability under radiation. A large number of distributed systems, thermal neutron fluences in shielded areas, and spectra composed mainly of neutrons are some of the unique challenges that the LHC presents. CERN has developed its own radiation hardness assurance procedure that addresses them through specific test methodologies. Based on lessons learned from component and system qualification, this paper presents CERN's system qualification procedure, these test methods, and lessons learned.

**Summary (500 words):**

CERN's electronics systems, both in the accelerator and in experiments, are exposed to the peculiar harsh radiation environments induced by the different particle accelerators. As such, the ability of these systems to withstand the effects of radiation on electronics is crucial to maintaining the smooth operation of the accelerators and achieving the organization's ambitious objectives.

To ensure the reliability of systems exposed to these environments, they must pass a battery of qualification tests in specific conditions described in the CERN Radiation Hardness Assurance procedure. This procedure, much like those used in other fields such as space, provides detailed instructions on how to qualify components and systems. However, due to the unique radiation environments present in accelerator areas, the qualification procedure presents several distinct challenges that have been overcome through the development of dedicated test methodologies that are now integral to the qualification process.

One of the primary challenges in LHC systems is their distributed nature. Unlike many other environments, these systems can be composed of thousands of individual units, which creates two major constraints: Firstly, Commercial Off The Shelf (COTS) components should be used whenever possible to keep costs down. Secondly, systems are exposed to diverse range of radiation environments, imposing different challenges both in terms of source and type of radiation effects, and multiplicity of the conditions to be tested.

Therefore, systems are exposed to all radiation effects possible, including Total Ionizing Dose (TID), Displacement Damage (DD), and Single Event Effect (SEE) together. Unlike space, the accelerator environments are mainly neutron dominated, leading to specific challenges to be assessed. One of the most significant threats to system reliability is the estimation of Displacement Damage on optoelectronics, caused by Non-Ionizing Energy Loss (NIEL) scaling violation between neutrons and other particles typically used for qualification. Optoelectronics are often the most vulnerable components in a system exposed to a neutron environment and a specific qualification methodology was developed to ensure the degradation estimation reliability.

Another challenge is the large predominance of thermal neutrons in shielded areas, as certain technologies can be susceptible to thermal neutron-induced (SEE). A systematic approach must be followed to evaluate this risk as it was shown with FPGAs for instance that in these areas thermal neutrons can be by far the main contributor to the failures and their underestimation can have dramatic consequences. Another unique challenge of the LHC is the fact that components and systems are exposed to a wide variety of TID and DD levels that induces combined TID-DD effects at circuit-level or system-level that can lead to various degradation rate and profiles depending on the TID/DD ratios there are exposed to, and a very careful test process must be followed to assess this issue.

In this work the complete procedure, from component to system level testing with the different challenges, the associated test methodologies, and the lesson learned will be presented in detail with a compilation of actual degradations and failures observed during qualifications, providing a detailed full picture of the CERN System qualification procedure.

**Tuesday posters session / 139**

## **Multi-Channel Radiation-Tolerant Humidity Monitoring System for the CMS Inner Cold Sub-detectors**

**Author:** Amar Kapic<sup>1</sup>

**Co-authors:** Andromachi Tsirou<sup>2</sup>; Piero Giorgio Verdini<sup>3</sup>; Sandro Carrara<sup>4</sup>

<sup>1</sup> EPFL/CERN

<sup>2</sup> CERN

<sup>3</sup> Universita & INFN Pisa (IT)

<sup>4</sup> EPFL

**Corresponding Author:** amar.kapic@cern.ch

In this presentation, we discuss a multi-channel radiation-tolerant and magnetic field-compatible humidity monitoring system developed for the needs of the CMS inner cold sub-detectors. The results of sensor irradiation tests, the tests conducted at different negative temperatures, and tests performed in the strong magnetic field are presented. Furthermore, a multi-channel readout unit has been designed, evaluated, and discussed. The proposed readout unit effectively nullifies both internal sensor parasitic effects and parasitic effects coming from long cables connecting the sensor to the readout electronics.

#### **Summary (500 words):**

In Silicon-based HEP detectors cooling is essential for two main reasons: i) to remove the heat generated by millions of densely packed bias and readout channels, ii) to compensate for the increase in leakage currents. Under such conditions of high-power density and cold operation, monitoring humidity becomes critical. However, selecting a humidity sensor that can survive such a harsh environment is challenging. We have developed a multi-channel radiation-tolerant and magnetic field-compatible humidity monitoring system that can operate in the HEP environment.

Before being compatible for installation in the accelerator/detector complex at CERN, sensing elements must be qualified for radiation tolerance, insensitivity to the strong magnetic field, and operability at temperatures well below 0°C.

The candidate capacitive humidity sensor was tested at the IRRAD facility of CERN up to a fluence of  $3 \times 10^{16}$  protons/cm<sup>2</sup>, equivalent to over ten years of HL-LHC operation for the inner sub-detectors. The tests were done in a temperature- and humidity-controlled environment at a nominal temperature of -20°C, using pre-calibrated gas mixtures to test the sensors' responsiveness. The tests showed a linear dependence of the sensor capacitance on the accumulated fluence which can then be corrected for.

Furthermore, sensor coming from the irradiation campaign, together with one non-irradiated sensor, were tested in the QART lab in a magnetic field of 2T. The sensor capacitance was not affected by the field. Then, the sensors were tested at negative temperatures (-10°C, -20°C, -30°C). While for positive temperatures, the sensor capacitance depends linearly on the relative humidity, for negative temperatures, the change in the sensor's capacitance can be fitted with a second-degree polynomial function.

The high granularity of the Phase-2 CMS cold detector requires the distribution of a large number of humidity sensors across the detector to ensure valid humidity monitoring. Therefore, it is crucial to design a multi-channel readout unit capable of conditioning as many humidity sensors as possible. Here, we present an 8-channel signal conditioning unit with two 4-channel ADC chips and MCU integrated on the same board that has the standard industrial 3U Eurocrate dimensions.

The conditioning is based on the auto-balancing bridge configuration. The bridge output signal contains information on the internal sensor leakage resistance caused by temperature variations, pollution, etc. Thus, the bridge output signal is demodulated by the control signal coming from the quadrature-phase shifter circuit to extract the sensor capacitance. The quadrature-phase shifter circuit is based on the TLV2474 chip and three RC networks. The same chip is used as an internal oscillator to generate the excitation sine wave. As the capacitive-humidity sensor will be read out over long cables, the conditioning circuit must eliminate the cable parasitic effects. This issue is solved using the active shielding technique.

The proposed radiation-tolerant and magnetic field-compatible humidity monitoring system has already been tested in the IRRAD facility and in several other test facilities in preparation for the LS3 sub-detectors. Finally, it will be integrated as a part of the upcoming CMS Cold subdetector DCS system.

Thursday posters session / 141

## **Radiation test of commercial of the shelf (COTS) optical transceivers in the frame of the beam position monitor (BPM) consolidation project for the Large Hadron Collider (LHC)**

**Author:** Manoel Barros Marin<sup>1</sup>

**Co-authors:** Andrea Boccardi<sup>1</sup>; Rudy Ferraro<sup>1</sup>; Salvatore Danzeca<sup>1</sup>; Selim Can Ozdogan<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** manoel.barros.marin@cern.ch

The consolidation of the Large Hadron Collider (LHC) beam position monitor (BPM) requires the deployment of about 5000 single-mode radiation-tolerant optical transmitters, working at 10 Gbps during 20 years of operation. While the use of the custom devices being designed at CERN remains the baseline for the project, 8 commercial of the shelf (COTS) optical transceivers have been evaluated as an alternative. This paper presents the results of the full characterization in radiation of these COTS devices, including cumulative effects and single event effects (SEE), evaluated during both data transmission and reception.

**Summary (500 words):**

The consolidation of the Large Hadron Collider (LHC) beam position monitor (BPM) aims to replace the current BPM system during the Long Shutdown 4 (LS4, i.e. 2032-33). The new BPM system shall reuse the same infrastructure as the current one (i.e. coaxial cables, optical fibres), constraining the digitization of the analogue signals to be performed close to the pick-ups. To cope with the radiation levels expected during High-Luminosity LHC (HL-LHC) operation, the front-end electronics shall be as simple and reliable as possible, whilst the back-end will process the incoming raw data. Following this approach, the analogue signals from each BPM will be digitized in the front-end by a 12-bit analogue-to-digital converter (ADC) at 1.25 Gbps. The digitized data will be directly forwarded in parallel through 4 single-mode optical transmitters working at 10 Gbps. These 4 optical signals will be multiplexed over a single optical fibre towards the back-end. This scheme will require about 5000 optical transmitters. While the baseline for the electro-optical interface in the tunnel side remains a single-mode radiation-tolerant dual transmitter named CWDM SM-VTTx developed at CERN by EP-ESE-BE, an alternative option based on commercial of the shelf (COTS) optical transceivers has been evaluated. To validate the feasibility of the alternative option, a radiation test campaign has been carried out in the COmpact MEDical Therapy cyclotron (COMET) at Paul Scherrer Institute (PSI). This cyclotron provides a proton beam that allows to perform radiation tests at component level, with conditions relevant to CERN applications. To maximize the probability of finding a suitable COTS candidate, 8 devices have been selected from 4 different types (SFP+, SFP28, QSFP+ and QSFP28). To obtain the full characterization in radiation of the devices under test (DUTs), cumulative effects and single event effects (SEE) have been evaluated during both data transmission and reception. On one side, cumulative effects have been evaluated through offline analysis. The aim of this test was to evaluate the impact of cumulative effects on the lifetime, optical power of the transmitter and sensitivity of the receiver by comparing measurements before and after irradiation. On the other side, SEE (e.g. single event latch-up (SEL), single event transient (SET), single event upset (SEU)) have been evaluated through online analysis. The aim of this test was to evaluate the impact of SEE on the bit error rate (BER), loss of lock (LOL) and control registers by monitoring the DUT in real-time. Based on the measurements of the online analysis, SEE cross-sections for the different DUTs have been calculated. This paper presents the results of the radiation test performed to COTS optical transceivers and discuss their impact on the reliability of the BPM consolidation project for the LHC, as well as describes the implementation of the radiation test setup.

**Optoelectronics and Electrical Data Links / 142**

## Test Bench of a 100G Radiation Hardened Link for Future Particle Accelerators

**Authors:** Francesco Martina<sup>1</sup>; Sophie Baron<sup>1</sup>; Paulo Rodrigues Simoes Moreira<sup>1</sup>; Mateusz Karol Baszczyk<sup>1</sup>; Stefan Biereigel<sup>1</sup>; Adam Klekotko<sup>None</sup>; Szymon Kulis<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** francesco.martina@cern.ch

Pioneering physics experiments require increasingly faster data transfers and high-throughput electronics, which drives the research towards a new class of serialisers and optical links. In this framework, the DART28, a 100 *Gbps* radiation tolerant serialiser and driver, has been designed in 28 *nm* CMOS technology and submitted in April 2023. The development has been coupled with an FPGA based emulation, which provided an early assessment of its behaviour, a scalable system-level demonstrator and an effective evaluation tool for compatible commercial solutions. The challenges faced in this research and the architecture of both the hardware setup and the firmware will be described.

**Summary (500 words):**

The most recent activities of the Electronic Systems for Experiments Group at CERN include the engineering of cutting-edge solutions for high-throughput data communication between the experimental area and the readout infrastructure for future detectors (in the framework of the CERN EP R&D programme). Because of the prohibitive conditions imposed by the radiation surrounding the particle beam paths, it is necessary to rely on the development of ASICs resistant to TID above 1MGy and mixed-field fluxes. Such components involve a complex design flow, a detailed verification of the embedded features and standardised post-production testing procedures.

In particular, the DART28 device is being developed in view of the future particle accelerators and it represents a pioneer 28nm CMOS based integrated circuit, delivering a 100G class data transfer over 4 lanes, which operate at 25.6Gb/s each. In the foreseen system, the DART28 will eventually be paired with a radiation-hard optical transmitter based on silicon photonics technology, which will adopt a CWDM technique for the aggregation of the links. This can be easily matched to commercial solutions based on QSFP modules for receiving data in the readout crates.

To enable an effective verification of the logical functionality of the device, a detailed emulation activity, based on modern Xilinx Ultrascale Plus series FPGAs, was initiated prior to submission to the foundry. Such a methodology has involved many challenges concerning the migration of the original customised primitives to FPGA ones and has represented a valuable complement to the development of this category of digital ASICs. In particular, it proved effective for the analysis of the system-level characteristics. In addition, such a platform enabled a realistic reproduction of the device's behaviour before its actual submission, facilitating: the upcoming validation planning, the resolution of potential difficulties that may be encountered in the testing environments and the design of the laboratory testbed. Finally, it paved the way for the engineering of the DART28 back-end counterpart, which represents the core of the validation system and one of the key deployable products for the eventual project commissioning. At this stage, programmable logic devices of the same family were employed for such a component, the architecture of which has been optimised to allow further automation of the device qualification procedures and the scalability of data links under test. The architecture of both the hardware setup and the developed firmware will be described in the present work.

ASIC / 143

## **Chips for calibration of the ATLAS LAr calorimeter**

**Author:** LAr speaker committee<sup>None</sup>

**Corresponding Authors:** ludovic.raux@cern.ch, larspeak@cern.ch

The LHC upgrade requires redoing the LAr calibration system which should provide a 16-bit range signal with 1‰ accuracy while being radiation tolerant. The former operating principle is used: a precise current is stored in an inductor, when it is switched off, a pulse is generated to be injected in the readout electronics. This is achieved by two chips: the first one, in TSMC 130nm, provides the 16-bit DAC as well as the calibration management system; the second one, in XFAB 180nm, embeds switches to generate the pulses. A description of both chips and measurement results will be presented.

**Summary (500 words):**

To calibrate the energy response of the ATLAS liquid argon calorimeter, an electronics calibration board

has been designed. It delivers a signal whose shape is close to the calorimeter ionization current signal with amplitude up to 100mA in 50Ω with 16-bit dynamic range. The amplitude of this signal is designed to be uniform over all calorimeters channels, stable in time and with an integral linearity much better than the electronics readout.

The LHC upgrade at CERN implies an increase in the dynamic range for the electromagnetic Liquid Argon (LAr) calorimeter of the ATLAS detector, a change in the power supply system and an increase of the luminosity and thus of radiation effects on detectors. This requires completely redoing the Liquid Argon calibration system. The new system should provide a 16-bit range current (from 5μA to 320mA) with 1% accuracy while being radiation tolerant.

The general principle of the calibration remains the same. The calibration pulse sent inside the cryostat is an exponential voltage signal built from a precise DC current using an inductor. When this current is switched off, the magnetic energy stored in the inductor is transferred to a resistance and therefore a fast precise pulse is generated to be injected in the readout electronics. For that, two dedicated ASICS have been developed to equip the 122 calibration boards and calibrate the 200,000 calorimeter channels. The first one, LADOC (Link And DAC Of CLAROC), made in TSMC CMOS 130nm technology, provides the 16-bit range current DAC (from 0.625μA to 40mA) as well as the calibration management system compatible with the lpGBT chip. The I2C slow control and commands to obtain pulses are treated by LADOC.

The second chip, CLAROC (Calibration of Liquid Argon Output Chip), made in XFAB HV 180nm technology, embeds four channels. Each channel is made of a current mirror with a gain of 8 in order to amplify the DAC current and to obtain the full required range (up to 320mA). The mirror is followed by a high frequency switch (1GHz) in order to generate the fast pulse for calibration.

Both chips have been extensively measured in laboratory and also under irradiation (X-Ray and protons). The performance obtained illustrated: a dynamic range up to 320mA in three energy scales with an integral linearity better than 0.1% in each of them, a response uniformity better than 0.2% and a stability better than 0.1%

The technological choices, the various R&D phases and most of the difficulties met will be discussed and illustrated by many measurements.

## Radiation-Tolerant Components and Systems / 144

### Prototype measurement results in a 65nm technology and TCAD simulations towards more radiation tolerant monolithic pixel sensors

**Author:** Corentin Lemoine<sup>1</sup>

**Co-authors:** Alex Kluge<sup>2</sup>; Francesca Carnesecchi<sup>2</sup>; Francesco Piro<sup>2</sup>; Gianluca Aglieri Rinella<sup>2</sup>; Giulio Borghello<sup>2</sup>; Hartmut Hillemanns<sup>2</sup>; Isabella Sanna<sup>3</sup>; Jerome Baudot<sup>4</sup>; Magnus Mager<sup>2</sup>; Miljenko Suljic<sup>2</sup>; Pedro Vicente Leitao<sup>2</sup>; Walter Snoeys<sup>2</sup>

<sup>1</sup> CERN / IPHC

<sup>2</sup> CERN

<sup>3</sup> CERN / Technische Universitat Munchen (DE)

<sup>4</sup> IPHC - Strasbourg

**Corresponding Author:** corentin.lemoine@cern.ch

Early measurements on monolithic pixel sensor prototypes in the TPSCo 65nm technology indicate a different response and radiation tolerance (up to  $5 \times 10^{15}$  1MeV n<sub>eq</sub>/cm<sup>2</sup>) for different sensor layout and process variants, illustrating the importance of layout and process in the path towards increased sensor radiation tolerance. Using these measurement results, TCAD simulations provide more insight to link the macroscopic behaviour of specific sensor variants to the details of its structure. With this insight we can propose a new variant combining the advantages of several measured variants as a path to even better radiation tolerance for the next iteration.

#### Summary (500 words):

Monolithic Active Pixel Sensors (MAPS) offer several advantages for particle physics experiments. Their good spatial resolution, often below 5 μm, combined with a low material budget (down to 0.05%X0/layer

in recent developments), makes them good candidates for vertex detectors, where they are located close to the interaction point (<2cm for the innermost layer of the next version of the ALICE inner tracking system, ITS3). While in the short-term development targeting ALICE ITS3 the pixel detector must only sustain a Non-Ionizing Energy Loss (NIEL) fluence of less than  $1e13$  1MeVneqcm<sup>-2</sup>, the environment for vertex detectors in other applications is often much more aggressive, requiring radiation tolerance up to or beyond  $1e16$  1MeVneqcm<sup>-2</sup>.

The evaluation of the TPSCo 65nm technology in the framework of the CERN Experimental Physics Research & Development program and in collaboration with the ALICE ITS3 project led to the production of sensor test structures in different processes and sensor layout variants and their irradiation up to  $1e16$  1MeVneqcm<sup>-2</sup>. In this context, the Analog Pixel Test Structure (APTS), a monolithic sensor prototype containing  $4 \times 4$  pixels featuring analogue output, aims at characterising the signal charge collection properties of the sensor. Early measurements with a Fe-55 source on these APTS chips indicate that the sensor signal and its evolution with NIEL fluence are highly dependent on the process and layout variant. In addition, the results suggest –still to be confirmed with detection efficiency evaluation in test beam –that some sensor variants remain functional even after  $5e15$  1MeVneqcm<sup>-2</sup>. This observation again illustrates the relevance of such process modifications and specific designs for the sensor radiation tolerance.

We would like to capitalize on these results to introduce a new variant combining the advantages of different measured variants as a path towards further increased tolerance to NIEL damage combined with low sensor capacitance. In this effort, technological computer-aided design (TCAD) is a useful tool to provide a greater understanding of observed measurements. It indeed provides a fully self-consistent transient simulation of electric field and carrier concentrations inside the sensor and hence the details of the charge collection.

Benchmarking the tool with existing and measured structures is an initial step which then allows the sensor optimisation with simulation prior to committing to a new cycle of design, manufacture, irradiation and test of the complete sensor. The new sensor variant introduced here remains close to the already fabricated and tested ones, in order to mitigate uncertainties on the radiation damage models and limit the deviations between simulations and experimental results.

Measurement results from the APTS will be presented and interpreted with the help of simulations. For the new proposed variant, only simulation results will be available for the conference: the main outcome of this work so far is the knowledge and insight extracted from the existing measurements using TCAD and the way this knowledge is used to propose a further optimisation. In fact, this presentation focusses mainly on the principle of iterative improvements of MAPS and the potential of TCAD simulations to optimise it.

**Tuesday posters session / 146**

## **Test and performance of the LiTE-DTU ASIC for the HL-LHC upgrade of the CMS ECAL barrel**

**Author:** Fabio Cossio<sup>1</sup>

<sup>1</sup> INFN Torino (IT)

**Corresponding Author:** fabio.cossio@cern.ch

A data conversion and compression ASIC, named LiTE-DTU, has been developed for the upgrade of the CMS electromagnetic calorimeter (ECAL) for the High-Luminosity phase of LHC. The ASIC integrates two 12-bit 160 MS/s ADCs, a data processing unit for gain selection and data compression, and a 1.28 Gb/s serializer.

The ASIC has been extensively tested in laboratory and in beam tests showing excellent yield and performance. The radiation tolerance has been verified with dedicated test campaigns for both total ionizing dose and single event effects. Results from these tests, showing the design readiness for mass production, will be presented.



**Summary (500 words):**

The challenging conditions of the high luminosity upgrade of LHC (HL-LHC) have required a full re-design of the CMS electromagnetic calorimeter (ECAL) front-end electronics. The Very Front-End cards will be equipped with two new ASICs: a fast trans-impedance amplifier (CATIA) and a data conversion and compression ASIC (LiTE-DTU). CATIA is trans-impedance amplifier to read the signals from the APD sensors coupled with the ECAL crystals. It features two differential outputs with different gains to ensure optimal resolution for signals up to 2 TeV. Designed in a commercial CMOS 65 nm technology, the LiTE-DTU ASIC integrates two 12-bit SAR ADCs to sample the CATIA outputs at 160 MHz. A gain selection mechanism and a lossless data compression algorithm allow data to be transmitted using only one 1.28 Gb/s serializer. The low-jitter 1.28 GHz clock, required by the ADCs and the serializer, is generated by an on-chip PLL.

This upgrade will ensure high-precision energy measurements for the HL-LHC phase and the improved time resolution, of about 30 ps for photons and electrons above 50 GeV, will cope with the increased pileup events and enhance the rejection of spike signals produced from direct interaction with the APDs. The LiTE-DTU ASIC has been extensively tested both in laboratory and beam tests and the pre-production version of the ASIC has shown excellent performance. An ADC ENOB of 9.4 has been measured at 50 MHz input frequency. This value, obtained using the internal PLL clock, is slightly lower than the design value of 10.2. Measurements using an external clock source and providing an ENOB of 10.2 indicate that this degradation is due to the PLL clock jitter. The overall performance is already adequate for the system requirements, nevertheless the PLL clock jitter will be improved in the ASIC next version.

Radiation tests have been performed to assess the LiTE-DTU tolerance to total ionizing dose (TID) damage with 10-keV X-rays up to 50 kGy and no variation has been observed in the performance of the ASIC after irradiation. The LiTE-DTU has been tested also for single event upsets (SEU) tolerance with a measured cross section of about  $6.8 \cdot 10^{(-18)} \text{cm}^2/\text{bit}$  for the I2C registers and  $9.4 \cdot 10^{(-13)} \text{cm}^2/\text{chip}$  for the data path, which is significantly higher as the ADC data registers are not SEU-protected. These results are more than adequate for the CMS experiment.

A 600 dies pre-production has been employed to equip a 400 channels ECAL module for large-scale integration tests and measure the performance and stability of the full readout chain. These chips have been tested and validated using an automated procedure with a yield of about 97%. This test setup features a test board with a ZIF socket, a commercial FPGA board, a low-jitter clock generator and two arbitrary waveform generators. All the modules are remotely controlled by a custom DAQ test interface written in Python. This system will be embedded in the automatic test equipment for the test and validation of the LiTE-DTU mass production which will deliver about 100k chips and is foreseen in May 2023.

**Thursday posters session / 147****Novel developments on the OpenIPMC project**

**Authors:** Alp Akpinar<sup>1</sup>; Andre Muller Cascadan<sup>2</sup>; Andrew Peck<sup>1</sup>; André Muller Cascadan<sup>3</sup>; Antonio Vitor Grossi Bassi<sup>2</sup>; Carlos Ruben Dell'Aquila<sup>2</sup>; Dan Gastler<sup>1</sup>; Daniel Edward Gastler<sup>1</sup>; Giacomo Fedi<sup>4</sup>; Luigi Calligaris<sup>2</sup>; Luis Ardila<sup>5</sup>

<sup>1</sup> Boston University (US)

<sup>2</sup> UNESP - Universidade Estadual Paulista (BR)

<sup>3</sup> UNESP

<sup>4</sup> Imperial College (GB)

<sup>5</sup> KIT-IPE

**Corresponding Author:** luigi.calligaris@cern.ch

In this contribution, we present the recent developments in the context of the OpenIPMC project, which proposes a free and open-source Intelligent Platform Management Controller (IPMC) software and an associated controller mezzanine for use in ATCA electronic boards. We discuss our experience in the operation of OpenIPMC on prototype boards designed for the upgrades of particle physics experiments at CERN. We show the addition of new functions and support for new protocols in the controller mezzanine firmware. Finally, the latest changes and improvements to the board design are presented.

**Summary (500 words):**

Over the last three years, the OpenIPMC project has focused on the development of an IPMC for ATCA electronic boards, with the aim of becoming a free, open-source, and highly customizable solution that permits the ATCA board developer to fully customize the device to fit his board's needs and allows independent maintenance and evolution of the firmware over the long-term. The OpenIPMC-HW hardware presents itself as an 8-layer PCB in the JEDEC MO-244 form factor designed around an STM32H7 microcontroller, with the card edge connector matching a commonly agreed-upon pin assignment across CERN experiments and providing a large number of general-purpose signals for board-specific use.

Recent developments on the mezzanine firmware include the addition of support for remote firmware upgrades following the PICMG HPM.1 standard, the YAFFS file system, the Trivial File Transfer Protocol, the Xilinx Virtual Cable service, the Remote Management Control Protocol, the RFC5424/3164 Syslog protocol, the IPMI System Event Log and a number of reliability improvements in the core hardware drivers. Other possible features currently being evaluated for introduction are discussed, such as firmware support for Advanced Mezzanine Cards and ATCA E-Keying. Furthermore, a number of improvements in the hardware design of the mezzanine are discussed, such as the addition of a debug header and changes to the method used to drive certain ATCA standard signals, to make the update and reboot processes of the IPMC not interfere with the running payload.

**Thursday posters session / 148****Digital duty cycle correction system for clock paths in radiation-tolerant high-speed wireline transmitters**

**Author:** Adam Klekotko<sup>None</sup>

**Co-authors:** Filip Tavernier ; Jeffrey Prinzie ; Mateusz Karol Baszczyk<sup>1</sup>; Paulo Rodrigues Simoes Moreira<sup>1</sup>; Stefan Biereigel<sup>1</sup>; Szymon Kulis<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** adam.klekotko@cern.ch

Ongoing developments in the field of radiation-tolerant high-speed transmitters (HST) aim to increase data rates above 25 Gb/s while increasing total ionizing dose (TID) tolerance above 1 Grad. The use of half-rate architecture imposes tight constraints on clock signal quality, in particular its duty cycle. Radiation degradation of transistors in the clock path causes duty cycle distortion (DCD), affecting the output signal quality of the HST. In this contribution, a digitally controlled duty cycle correction system suitable for HST is presented, which compensates for process, voltage, and temperature variation as well as radiation-induced duty cycle distortion of the clock.

**Summary (500 words):**

Radiation-tolerant transmitters targeting data rates above 25 Gb/s have to cope with stringent requirements of clock quality. The parameters of the clocks for such systems are constrained by the output data quality defined in modern communication standards limiting values of the signal distortion or different types of jitter. One of those parameters is Even Odd Jitter (EOJ), which primarily originates from duty cycle distortion in the high-speed clock. In high-energy physics experiments, those transmitters are used in a radiation environment so these circuits should exhibit robustness against high levels of total ionization dose (TID). Prior research has shown that radiation-induced unequal degradation of PMOS and NMOS devices leads to changes in the duty cycle of critical clock signals.

The Demonstrator ASIC for Radiation-Tolerant Transmitter in 28 nm (DART28) developed in the context of the Experimental Physics R&D programme on technologies for future experiments at CERN aims to achieve a data rate of 25.6Gb/s per link and radiation robustness up to 1 Grad. The serializer of that transmitter implements half-rate topology which constrains the highest-speed clock to 12.8 GHz. The half-rate topology also implies that any duty cycle distortion of the high-speed clock will result in additional EOJ at the output. The commercially used communications standards require an EOJ below 0.035 Unit interval peak-peak (UIpp) which in this application is 1.36ps. Without active duty cycle correction,

meeting this specification over PVT and radiation-induced degradation is a very challenging problem in advanced CMOS nodes. To meet this specification over an extended range of TID, the duty cycle correction system of the clock was designed to meet the stringent specification and ensure proper transmitter operation over a wide TID range.

The designed digitally controlled duty cycle correction system consists of two main parts:

- A duty cycle adjustment (DCA) circuit comprises a chain of current-starved inverters with digitally controlled driving strength. In each inverter, the rise and fall times can be controlled independently to counteract radiation-induced changes in the duty cycle.

The implemented DCA circuit provides tunability of  $\pm 6\%$  ( $\pm 4.8$  ps) across PVT corners with a step size better than 400fs.

A random sampling duty cycle measurement (RS-DCM) circuit, based around a sampling flip flop with ultra-low hysteresis ( $<10$ fs) guarantees high precision in distinguishing between low and high states. The flip flop samples the high-speed clock with an uncorrelated low-speed clock. If the clock signal is truly sampled uncorrelated to the sampling rate, the number of acquired relative ones represents the clock's duty cycle if a sufficient amount of samples was taken.

In this paper, the architecture, performance, tunability curves and influence of the duty cycle distortion on the high-speed clock on the output of the HST will be presented. Also, TID-induced degradation will be compared to an uncompensated clock path. TID degradation simulations were performed using device models including TID-related degradation of NMOS and PMOS transistors, accounting for differences in their respective TID sensitivity.

ASIC / 149

## In-pixel AI for lossy data compression at source for X-ray detectors

**Authors:** Adam Quinn<sup>1</sup>; Chris Jacobsen<sup>2</sup>; Danny Noonan<sup>3</sup>; Davide Braga<sup>4</sup>; Farah Fahim<sup>5</sup>; Giuseppe Di Guglielmo<sup>5</sup>; Manuel Valentin<sup>None</sup>; Nhan Tran<sup>3</sup>; Panpan Huang<sup>2</sup>; Priyanka Dilip<sup>6</sup>; Seda Ogren<sup>2</sup>; Thomas Zimmerman<sup>3</sup>

<sup>1</sup> Fermi National Accelerator Laboratory

<sup>2</sup> Northwestern University

<sup>3</sup> Fermi National Accelerator Lab. (US)

<sup>4</sup> FERMILAB

<sup>5</sup> Fermilab

<sup>6</sup> Stanford University / Fermilab

**Corresponding Authors:** gdg@fnal.gov, daniel.christopher.noonan@cern.ch

This work introduces AI-In-Pixel-65, an ROIC test chip designed for pixelated X-ray detectors using a 65nm Low Power CMOS process. The study compares two data compression techniques, Principal Component Analysis (PCA) and AutoEncoder (AE), implemented within the chip's pixelated area to address I/O bottlenecks. Our design methodology utilizes high-level synthesis (HLS) and hls4ml, offering shorter design cycles and similar quality results compared to register-transfer level (RTL) flows. Results show PCA achieves 50-fold compression with a 21% pixel area increase, while AE offers 70-fold compression and similar area increase.

### Summary (500 words):

Integrating data compression neural networks into Read-Out Integrated Circuits (ROICs), specifically within the pixelated front-end, has the potential to significantly decrease off-chip data transfer, thereby overcoming the input/output bottleneck. We have developed an ROIC test chip called AI-In-Pixel-65, which is designed using a 65nm Low Power CMOS process to read pixelated X-ray detectors.

Each pixel in the chip comprises an analog front-end responsible for signal processing and a 10-bit analog-to-digital converter that operates at a speed of 100,000 samples per second (100KSPS). In our study, we have compared two non-reconfigurable techniques for data compression, namely Principal Component Analysis (PCA) and AutoEncoder (AE), which are implemented within the pixelated area of the chip.

Our design methodology leverages high-level synthesis (HLS) and hls4ml to provide a shorter design cycle and similar quality of results compared to register-transfer level (RTL) flows. hls4ml is an open-source framework for the hardware codesign of neural networks. At its core, hls4ml translates machine-learning models from common open-source software frameworks such as TensorFlow into an RTL implementation using HLS tools. In particular, we adopted the industry standard Siemens Catapult HLS. In hls4ml, a designer can trade off the performance and area utilization for a model by varying the parallelization of the algorithm via several configuration parameters. For example, the reuse factor parameter controls how many times each multiplier resource is used in the final hardware implementation: a designer with the goal of low latency will choose a lower RF value.

Additionally, for the model training, we adopted quantization-aware training (QAT) with QKeras. QAT is a machine learning technique to train models optimized for deployment on hardware with low-precision arithmetic. QAT simulates the effects of quantization during the training process, mapping a continuous range of values to a smaller set of discrete values. As a result, the model learns to be more robust to the effects of quantization, which can lead to improved accuracy and reduced memory and computation requirements at inference time.

In our chip, the PCA algorithm demonstrates a 50-fold compression, introduces a latency of one clock cycle, and results in a 21% increase in the pixel area. On the other hand, the AE method achieves a higher compression rate of 70 times, adds a latency of 30 clock cycles, and leads to a similar increase in the pixel area compared to PCA. By evaluating the performance of these two data compression techniques within the pixelated region, our study offers insights into their respective merits and limitations in addressing the I/O bottleneck in ROICs.

**Thursday posters session / 150**

## **Method for extracting the single event upset cross section from error counts in triplicated error-correction code registers**

**Author:** Jon Wilson<sup>1</sup>

<sup>1</sup> *Baylor University (US)*

**Corresponding Author:** jsw@fnal.gov

Digital circuits exposed to radiation, e.g. at HL-LHC, are equipped with radiation-hardening features such as triple modular redundancy and error-correction codes. A method is developed to measure the single-event-upset cross section from error rate measurements in register banks that are protected by both ECC and TMR, taking into account the non-linear relationship between the cross section and the error rate. The method is employed to measure this cross section using data from irradiation tests of the ECON-T, an ASIC developed for the CMS experiment, and then to predict the error rate in the ECON-T during operation on the CMS detector.

**Summary (500 words):**

Prior to installation of the CMS endcap calorimeter upgrade (HGICAL), all of the electronics that will be used on-detector undergo extensive radiation testing. This is done to ensure that the HGICAL electronics will function correctly in the extremely high radiation environment of the high-luminosity LHC. One of the goals of these tests is to predict the rate at which errors will occur throughout the entire HGICAL during HL-LHC operations, and to verify that that error rate is acceptable. Because of the error mitigation techniques employed in the ASIC designs, which include triple modular redundancy and error-correction codes, the error rate is a complicated and non-linear function of the flux of incident particles and of the single-particle cross section to cause some event. Understanding this non-linear function is necessary both to measure the single-particle cross section using the radiation test data and also to predict the HL-LHC error rate using the measured cross section and expected HL-LHC flux. Further complicating matters is the fact that there is more than one cross section for different types of events. We have developed a method, based on a continuous-time Markov chain, to describe this non-linear function at any order of approximation, use it to extract the relevant cross section(s), and extrapolate to the HL-LHC environment. We will first describe the method, and then demonstrate the

use of the method by applying it to the ECON-T radiation test data and predicting the error rate in ECON-T at the HL-LHC.

ASIC / 151

## Dual use driver for high speed links transmitters in the future high energy physics experiments

**Authors:** Mateusz Karol Baszczyk<sup>1</sup>; Stefan Biereigel<sup>1</sup>; Adam Klekotko<sup>None</sup>; Szymon Kulis<sup>1</sup>; Paulo Rodrigues Simoes Moreira<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** mateusz.baszczyk@cern.ch

The paper presents a Dual Use Driver (DUDE) that is a component designed for the “Demonstrator ASIC for Radiation-Tolerant Transmitter” in 28nm (DART28) and is developed in R&D programme on technologies for future experiments. The driver operates at 25.6Gbps and it allows to drive either 100Ω transmission lines and optical ring modulators in a Photonics Integrated Circuit. The driver includes configurable pre-emphasis. The device will allow to demonstrate the feasibility of wavelength division multiplexing optical links operating with bandwidths in excess of 100Gbps per fiber that are capable of sustaining total ionizing radiation doses up to 10MGy.

### Summary (500 words):

The circuit described here is designed in the framework of the Strategic R&D Programme on Technologies for Future Experiments in the Work Package 6 (WP6) - High Speed Links (HSL). The objective of WP6 HSL is to demonstrate the feasibility of wavelength division multiplexing (WDM) optical links operating at bandwidths in excess of 100 Gbps per fiber while being capable of sustaining radiation with Total Ionizing Doses (TID) approaching 10 MGy radiation.

Dual Use Driver (DUDE) is a part of the Demonstrator ASIC for Radiation-Tolerant Transmitter in 28 nm (DART28). The first prototype operates at 25.6 Gbps per lane and uses NRZ signaling. The paper will present a driver prototype which is an intermediary stage between the serializer and the Photonics Integrated Circuit (PIC). PIC includes components as ring modulators, PIN-diodes and waveguides. The whole system is aim to work in the high radiation zone.

DUDE is a multipurpose, modular unit which is capable of driving both 100 Ω transmission lines and ring modulators. This approach allows not only the Silicon Photonics (SiPh) co-integration but it extends the testability of the system especially in a high radiation environment.

The DUDE is a pseudo-differential driver with two symmetric complementary outputs for anode and cathode. The output stage is segmented to enable adjustment of the output current which is desirable in order to compensate Process-Voltage-Temperature variations and to adapt to various loads. The DUDE consists of the 29 segments in total which can be enabled and programmed individually.

Both complementary outputs can be programmed in one of the modes of operation:

- 100 Ω transmission line driver
- reduced swing driver
- full swing CMOS driver

A particular challenge of this design is the driving of the SiPh ring modulator with the low voltages compatible with the supply voltage of the 28 nm CMOS technology. To overcome this limitation (and to maximize the driving amplitude) the ring modulator is driven pseudo-differentially on both the anode and cathode terminals. This, however, might lead to the PN-junction of the ring modulator being forward biased, which must to be avoided. To prevent that, the driver was designed to produce reduced (and programmable) amplitude signal swing on the anode terminal.

The DUDE includes a pre-emphasis circuit which is able to compensate for channel bandwidth limitations in order to minimize intersymbol interference (ISI). Two modes of pre-emphasis are implemented:

- Two-tap Feed-Forward Equalization (bit-level pre-emphasis);

- Edge pre-emphasis.

Feed-Forward Equalization is implemented by the pre- and the post-cursor drivers in both complementary outputs. Their driving strength is individually programmable, allowing for optimal equalization of bandwidth-limited channels. Edge pre-emphasis can be used to additionally improve rise and fall times at the output nodes of the driver by providing increased current to the load during signal transitions. Its strength can be controlled by means of the current impulse duration and the amplitude of additional current supplied.

The paper will present the architecture of the system, implementation details, functionality of the various modes of operations and performance studies.

ASIC / 152

## Characterization of the ATLAS Liquid Argon Front-End ASIC ALFE2 for the HL-LHC upgrade

**Authors:** Dimitrios Matakias<sup>1</sup>; Gabriella Carini<sup>None</sup>; Grzegorz Deptuch<sup>1</sup>; Hao Xu<sup>1</sup>; Hong Ma<sup>1</sup>; Hucheng Chen<sup>1</sup>; James Kierstead<sup>1</sup>; Laurent Duflot<sup>2</sup>; Mietek Dabrowski<sup>1</sup>; Nicolas Morange<sup>3</sup>; Sergio Rescia<sup>None</sup>; Shaochun Tang<sup>1</sup>; Tiankuan Liu<sup>1</sup>

<sup>1</sup> Brookhaven National Laboratory (US)

<sup>2</sup> CNRS (FR)

<sup>3</sup> Université Paris-Saclay (FR)

**Corresponding Author:** dimitrios.matakias@cern.ch

ALFE2 is an ATLAS Liquid Argon Calorimeter (LAr) Front-End ASIC designed for the HL-LHC upgrade. ALFE2 comprises four channels of pre-amplifiers and CR-(RC)2 shapers with adjustable input impedance. ALFE2 features two separate gain outputs to provide 16-bit dynamic-range coverage and an optimum resolution for small signals. ALFE2 is characterized using a Front-End Test Board (FETB) based on a Zynq UltraScale+ MPSoC and two octal-channel 16-bit high-speed ADCs. The test results indicate that ALFE2 fulfills or greatly exceeds all specifications on gain, noise, linearity, uniformity, and radiation tolerance.

### Summary (500 words):

ALFE2 is an ATLAS Liquid Argon Calorimeter (LAr) Front-End ASIC designed for the High Luminosity-Large Hadron Collider (HL-LHC) upgrade. ALFE2 comprises four channels of Pre-Amplifiers (PAs) and CR-(RC)2 shapers (SH) with adjustable input impedance. Each shaper has two separate gain outputs, Low Gain (LG) and High Gain (HG). These outputs can be read out simultaneously to provide 16-bit dynamic-range coverage. ALFE2 includes a Trigger-Sum (TS) output, which has a CR-RC shaper stage with switchable gains between 1 and 3. ALFE2 implements an I2C target block with 16 8-bit internal registers for slow control and configuration purposes. ALFE2 is manufactured in a TSMC 130 nm CMOS process. The die of ALFE2 is 5.00 mm × 4.55 mm packaged in a 196-pin Ball Grid Array (BGA) package with a pitch of 0.8 mm.

ALFE2 is characterized using a Front-End Test Board (FETB), which is a high-speed data-acquisition platform based on a System on a Module (SoM) from Enclustra. The SoM has a Xilinx Zynq UltraScale+ Multiprocessor System on a Chip (MPSoC). The FETB uses two octal-channel 16-bit state-of-the-art ADCs from Texas Instruments. The ADCs sample the output signals of ALFE2 at 40 MHz. The FETB runs Peta-Linux on the embedded ARM processor.

The ALFE2 test results demonstrate that it fulfills or greatly exceeds all specifications for the ATLAS LAr Calorimeter. The measured Equivalent Noise Currents (ENIs) are 170 nA and 50 nA for 25 Ω and 50 Ω input impedances, respectively, about half of the specifications. The measured Integral Non-Linearity (INL) of the HG outputs is below 0.1%, half of the specification of 0.2%. The INL of the LG outputs is below 0.25% (specification 0.5%) in the 80% dynamic range and less than 1% (specification 5%) in the full dynamic range. The Power Supply Rejection Ratio (PSRR) is higher than 20 dB (specification 10 dB) below 1 MHz. Excellent uniformity is measured with a yield of 100% and a large margin observed across 40 ASICs and channels.

Two samples were exposed to 7 kGy and 15 kGy, respectively, in <sup>60</sup>Co gamma ray at the dose rate of 0.028 Gy/s. No measurable change is observed on INL and ENI. No significant change is observed in the

baselines of the LG and HG outputs. The gain of the LG, HG, and TS outputs has about a 0.2% increase. The change in the trigger sum baseline is about 3 mV (below 0.5%).

A Single-Event Upset (SEU) test was conducted on ALFE2 with 226 MeV protons at the Proton Therapy Center of Massachusetts General Hospital. Four chips were irradiated with the auto-refresh mechanism enabled. No SEU errors were detected in any chip. The cross-section was estimated to be lower than  $4.51 \times 10^{-17}$  cm<sup>2</sup>/bit after the results of the four chips are combined. The error rate for the entire HL-LHC ATLAS LAr calorimeter is extrapolated to be less than 2.4 bitflips per day.

The characterization tests have demonstrated that the ALFE2 design meets and exceeds all requirements for the ATLAS LAr Calorimeter in the HL-LHC upgrade.

## System Design, Description and Operation / 153

### SciFi Front-End Electronics: Calibration and Results on detector performance

**Author:** Ulisses de Freitas Carneiro da Graca<sup>1</sup>

**Co-author:** The SciFi Collaboration

<sup>1</sup> CBPF - Brazilian Center for Physics Research (BR)

**Corresponding Author:** u.carneiro@cern.ch

The LHCb Experiment is commissioning its first upgrade to cope with increased luminosities of LHC Run3, being able to improve on many world-best physics measurements. A new tracker based on scintillating fibers (SciFi) replaced Outer and Inner Trackers delivering an improved spatial resolution for the new LHCb trigger-less era, with a readout capable of reading ~524k channels at 40MHz. Fully automated calibration of SciFi Front-End Electronics is based on dedicated software tools and operational procedures, validated during SciFi commissioning. This oral presentation describes the SciFi electronics design, implementation, and calibration and presents results showing the detector's performance after commissioning.

#### Summary (500 words):

The LHCb tracker for Run3 covers an area of 340 m<sup>2</sup> using a novel technology, with more than 10,000 km of a 250 μm diameter blue-emitting scintillating fiber. This Scintillating Fiber Tracker (SciFi) achieves a spatial resolution better than 80 μm, hit efficiency better than 99%, and can handle higher luminosities thanks to its higher granularity and a trigger-less 40 MHz Read-Out. These substantial improvements posed new challenges to the on-detector electronics, which has to process signals from 4096 linear arrays of 128-channel Silicon Photomultipliers (SiPM) each, placed at the fiber ends and cooled to -40 °C. The low photo-electron statistics required a very sensitive digitizer, the high channel density (4 channels per mm) demanded careful PCB design, and possibly most challenging, the sheer data volume required high-speed data transmission and ultimately needed to implement an advanced zero-suppression clustering mechanism in the Front-End Electronics.

A custom-made ASIC (PACIFIC) processes SiPM analog signals, providing signal shaping, charge integration over a time window, and discrimination. The need to reduce the data volume shaped the electronics design at every step and constrained the digitized output of each 250 μm SiPM channel, which consists of only 2 bits encoding the result of signal discrimination over three programmable thresholds. Even so, the throughput of each 2048-channel SciFi Read-Out Box at 40 MHz would be an intractable 164 Gbps. Therefore, significant data reduction was necessary before channeling data to the 4.48 Gbps GBTx serializers. Hit clustering provides such a data reduction, but its complexity, combined with the relatively low radiation doses expected, resulted in the choice to perform digital signal processing and fast control handling in radiation-tolerant flash-based Microsemi Igloo2 FPGAs. A research program validated the usage of such FPGA in our radiation environment, and since last year, SciFi routinely operates for data taking with LHC beam using these devices. PACIFIC ASIC, FPGAs, GBT chipset, and specially designed DC-DC converters have been packed into 256 units called Read-Out Boxes, each of which reading 2048 SiPM channels with a zero suppressed data output rate of up to 71 Gbits/sec, resulting in a total bandwidth of over 18 Tbits/sec.

This complex design requires several re-programmable parameters to accommodate changes in the operational conditions, like fiber signal deterioration and increasing noise on SiPMs. The continuous recalibration of parameters such as clock delays, temperature-dependent bias, threshold settings, and

others is crucial to retain the detector's best performance during its lifetime. A wealth of databases and software tools are required to fully automate the process of taking data, analyzing them to determine the best operational settings, and transferring these to the detector electronics configuration. Developing these tools has been a monumental enterprise starting from the SciFi assembly and pre-commissioning, and automatic calibration procedures have been instrumental for commissioning after installation in 2022, ensuring that SciFi could take LHC collision data and perform as expected. This oral presentation will give an overview of SciFi electronics design and implementation, tools and methods for electronics calibration, and show results on detector performance.

ASIC / 154

## Design and characterization of RD53C production chips for ATLAS and CMS pixel upgrades at HL-LHC

**Author:** Luca Pacher<sup>1</sup>

<sup>1</sup> *Universita e INFN Torino (IT)*

**Corresponding Author:** luca.pacher@cern.ch

The RD53 Collaboration, established in 2013 as a joint effort between ATLAS and CMS pixel ASIC communities on 65nm CMOS technology, is now in the phase of implementing final pixel readout chips, referred to as RD53C revisions, that will be used into upgraded pixel detectors at HL-LHC. The purpose of this work is to provide a comprehensive review of most important architectural design choices, enhancements, implementation details and verification flows adopted to submit final ATLAS and CMS production chips, along with preliminary test results and measurements.

### Summary (500 words):

New hybrid pixel detectors will be installed into ATLAS and CMS experiments to cope with unprecedented data rates and radiation levels foreseen for the High-Luminosity LHC upgrade at CERN. New machine operations will increase the instantaneous luminosity up to  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ , delivering an average of approximately 200 inelastic proton-proton collisions per beam crossing at the 40 MHz bunch-crossing rate.

The RD53 Collaboration was established in 2013 and extended in 2018 with the final goal to develop new pixel readout chips to be installed into ATLAS and CMS pixel detectors at HL-LHC. The chosen implementation technology has been a commercial 65nm CMOS which in the last decade has been extensively qualified and has been demonstrated to be radiation tolerant and able to cope with HL-LHC radiation levels.

A first large scale prototype chip, referred to as RD53A, was fabricated in August 2017. This chip allowed the experiments to evaluate different pixel readout architectural choices and analog front-end solutions fitting a 50  $\mu\text{m}$  x 50  $\mu\text{m}$  pixel size.

Later on a common design environment, referred to as RD53B, as been developed to implement pre-production versions of the ATLAS (ItkPix\_v1) and CMS (CROC\_v1) chips with parameters and IP blocks that can be instantiated into physically different chips by changing parameters. These chips have been submitted in 2020 and 2021 respectively, resulting into two physical instances of the common RD53B environment with different design choices such as pixel-array size and front-end flavour based on specifications driven by the experiment, while keeping all other system-level digital and mixed-signal functionalities in common. Extensive measurements and system characterizations have demonstrated these chips to be able to operate in the extremely harsh radiation environment (1 Grad) with very high hit rate (up to 3 GHz/cm<sup>2</sup>), trigger rates (4 MHz) and a high data rate readout (5 Gb/s) foreseen in the innermost pixelated layers at HL-LHC.

Final production chips, referred to as RD53C revisions and implementing minor fixes for known bugs from previous chips and further enhancements, will operate into ATLAS and CMS pixel detectors. At



the time of writing the final version of the ATLAS pixel chip (ItkPix\_v2) has been submitted in April 2023, while the submission of the final CMS chip (CROC\_v2) is foreseen for July 2023.

The aim of this contribution is to provide a comprehensive review of RD53C production chips, summarising most important architectural features (global floorplan, front-end choice, serial powering, clock data recovering, slow control and configuration, trigger scheme, data processing, readout interface, multi-chip data merging, SEU/SET mitigation strategy) along with details on physical implementation and verification flows adopted by the RD53 Collaboration to design and verify such complex pixel chips. Preliminary test results on submitted chips will be also presented.

ASIC / 155

## Tri-axis 5 $\mu$ m hexagon pixel-strip matrix combining 3\*852 current comparator in a 180nm node

**Authors:** Abreu Aguilar Henso javier<sup>1</sup>; Christine Guo Hu<sup>2</sup>; Claude Pierre Colledani<sup>2</sup>; Edouard Bechetoille<sup>2</sup>; Gilles Lucien Claus<sup>2</sup>; Grégory Bertolone<sup>None</sup>; Guy Doziere<sup>3</sup>; Herve Mathez<sup>2</sup>; Isabelle Valin<sup>None</sup>; Laktineh Laktineh<sup>4</sup>; Liang ZHANG<sup>5</sup>; Thanh Hung PHAM<sup>6</sup>

<sup>1</sup> IP2I

<sup>2</sup> Centre National de la Recherche Scientifique (FR)

<sup>3</sup> IPHC

<sup>4</sup> Universite Claude Bernard-Lyon I (FR)

<sup>5</sup> Shandong University

<sup>6</sup> CNRS

**Corresponding Author:** e.bechetoille@ip2i.in2p3.fr

We present a new kind of sensors made of 5 $\mu$ m pixels using 6-metal TJ 180 nm technology. The pixels are interconnected among themselves to conducting lines with three directions 0°, 120° and -120°. Two neighbouring pixels are connected to different lines with different directions. The lines are connected to readout cells hosting current amplifier with its current comparator, together with the digital readout circuitry. In a 400 ns frame, the circuit can output the address position of up to 16 hits. The sensor of 0.5cm<sup>2</sup> is intended to reduce the number of electronic channels while preserving the spatial resolution.

### Summary (500 words):

The PICMIC project proposes a new detection system allowing the exploitation of the excellent time ( $\sim$ ps) and spatial ( $\sim$  $\mu$ m) resolutions that a MicroChannel Plate (MCP) can provide. This presentation will focus on the position measurement of the PICMIC detection system using a new sensor of 5 $\mu$ m hexagonal pixels that occupy the top metal layer (TML) of a circuit for collecting charge from MCP [Fig.1]. Those collection pixels are interconnected through vias to conducting lines of different orientations in an original way and hence reduce drastically the number of readout channel. In this new scheme, two neighbouring pixels are connected to two different lines of different orientations. The conducting lines of the same orientation are placed in one of the next three metal layers (TML-1, -2, -3). The three orientations are 120°, -120° and 0°. Under the interconnection layers, a readout matrix (RM) is overlaid in the rest available metal layers. To cover a MCP surface of 50mm<sup>2</sup>, the demonstrator, fabricated in TJ180nm technology, features a RM of 53128 readout-cell of 140 $\mu$ m x 50 $\mu$ m size, but only 3852 places are needed to grab the corresponding lines. The Analog part is made of an optional current mirror to reduce the input impedance, followed by a current comparator. The threshold of the current mirror is selectable with an 8-bit common current-DAC from 80nA to 20.48 $\mu$ A. An additional inner-place 3-bit system adjust locally the fixed pattern offset of the array.

The digital array is read by a priority encoder mechanism. Every cell that records a hit, raise a flag. The flag is released once its address position is recorded. This sequencing permits to read 16 positions in a frame of 400ns. The data are sent out in parallel at 40MHz.

A robust i2c protocol is used to set the ASIC's configurations. The maximum overall power consumption of the circuit is  $256\text{mA} \times 1.8\text{V}$ . The application expects triangle-shaped current signals in the range of  $[13\mu\text{A} \times 2\text{ns}]$  and  $[1.8\text{mA} \times 0.4\text{ns}]$ .

Injecting current pulses through a thin probe on top of the die. Several lines are fired. By crossing we were able to successfully determine the injection position. We repeated the injection using two different at the same time and we were able to find the two positions with a resolution of  $5\ \mu\text{m}$  confirming that the new device will be able to efficiently separate nearby particles.

Ongoing study are evaluated to decrease the pitch to  $2.5\mu\text{m}$ , together with the increase of the size of the sensor to  $1\text{cm}^2$ . Additional feature will be implemented to timestamp and memorize more event, as well as increasing the readout speed. In an even further step, changing to a smaller technology node is envisaged.

Meanwhile, the detector setup for the proof of concept of the PICMIC project is almost ready, to take full benefit of the MicroChannel Plate sensors.

Successfully, this amazing Tri-axis pixel-strip circuit had been invented, developed, produced and tested in less than 3 years.

This works had been funded by CNRS-prematuration and IN2P3 R&T program.

## Programmable Logic, Design and Verification Tools and Methods / 156

### The CMS HGCAL trigger data receiver

**Author:** Raghunandan Shukla<sup>1</sup>

**Co-authors:** André David<sup>2</sup>; Milos Vojinovic<sup>1</sup>; Paul Dauncey<sup>1</sup>

<sup>1</sup> Imperial College (GB)

<sup>2</sup> CERN

**Corresponding Author:** raghunandan.atul.shukla@cern.ch

As part of the CMS Phase-2 upgrade, a prototype of the receiver of raw trigger data from the HGCAL endcap has been implemented using the Serenity ATCA platform. The receiver firmware was developed to test the unpacking of data from the front-end endcap trigger concentrator ASIC and measure its performance and stability. The firmware mainly consisted of unpacker blocks to decode ASIC packets, error detection mechanisms and online histogramming capability. The system was successfully used to achieve complete trigger path readout, involving several ASICs, and to test the stability of the system with online and offline monitoring.

#### Summary (500 words):

The CMS HGCAL front-end (FE) system includes several custom radiation-hard ASICs. These consist of a multichannel ADC and TDC (HGCROC) followed by concentrator ASICs (ECON) which aggregate data from multiple HGCROCs. Aggregated data is serialised using a high-speed serializer (LpGBT) and transmitted to the back-end (BE) system using optical transceivers (VTRx+). The HGCAL Trigger Primitive Generator (TPG) will construct calorimeter clusters for the Level 1 trigger decision using "trigger cells" (TC) from the FE chain. BE Stage-1 of the TPG is responsible for decoding the compressed TCs from the trigger concentrator ASIC (ECON-T), filtering the TCs, and sending them to the time-multiplexed Stage-2 of the system. The TPG Stage-1 will be implemented using the Serenity ATCA platform, with each FPGA expected to handle about 300 ECON-Ts. The overall HGCAL electronics system is summarised in Figure 1.

The ECON-T supports different compression algorithms. The variable latency algorithm offers high efficiency but it is complex and resource intensive to decode at the BE. The fixed latency algorithms are much easier to handle and have been shown to offer comparable performance in simulation studies. The unpacker firmware was developed for the variable latency and one of the fixed latency algorithms. The

BE firmware mainly consisted of unpacker blocks to decode ECON-T packets, error detection mechanisms and online data analysis by histogramming different parameters. Status and error counters were periodically read out using an onboard control bus and metrics were displayed using a Grafana web interface.

The prototype Stage-1 system was tested with two versions of HGCAL FE vertical stacks. The earlier version used an emulator for the ECON-T while the latest version used the prototype ECON-T. The BE firmware and the FE ASICs were tested in steps, integrating one ASIC of the chain at a time. Initial tests included configuring the ECON-T with known input data patterns (static and PRBS) and testing the decoding at the BE with different compression algorithms and packet types. Figure 2 shows the result of one such test where the ECON-T was programmed to use PRBS-generated TCs and the variable latency algorithm to package them. A histogram of the number of TCs in each decoded event in the firmware showed the expected packet type selection and truncation behaviour. Ultimately, the challenging task of integrating the complete trigger chain was achieved and we could accurately reproduce (receive) pre-programmed TCs from HGCROC in the BE.

The prototype BE system allowed successful testing and validation of some major BE firmware components and the ECON-T ASIC. It has established a readout of the complete trigger chain. We were also able to test the stability of the system with online and offline monitoring. The BE system is being expanded further to include the DAQ path (HGCROC and ECON-D ASIC) and high-speed readout. We are preparing to test a complete vertical slice in a beam test in summer 2023.

## Trigger and Timing Distribution / 157

# Real time data processing with FPGAs at LHCb

**Authors:** Andrea Contu<sup>1</sup>; Federico Lazzari<sup>2</sup>; Francesco Terzuoli<sup>3</sup>; Giovanni Bassi<sup>4</sup>; Giovanni Punzi<sup>3</sup>; Giulia Tuci<sup>5</sup>; Michael J. Morello<sup>6</sup>; Riccardo Fantechi<sup>3</sup>; Sofia Kotriakhova<sup>7</sup>; Wander Baldini<sup>7</sup>

<sup>1</sup> INFN

<sup>2</sup> Università di Pisa & INFN Pisa (IT)

<sup>3</sup> Università & INFN Pisa (IT)

<sup>4</sup> SNS & INFN Pisa (IT)

<sup>5</sup> Heidelberg University (DE)

<sup>6</sup> SNS and INFN-Pisa (IT)

<sup>7</sup> Università e INFN, Ferrara (IT)

**Corresponding Author:** andrea.contu@cern.ch

During the LHC Run-3 the LHCb software trigger is expected to reconstruct events at an average rate of 30 MHz. In view of future runs at even higher luminosities, LHCb established a testbed for new heterogeneous computing solutions for real-time event reconstruction within the current DAQ infrastructure. The most advanced of these is a highly-parallelized custom tracking processor (“Artificial Retina”), implemented in state of the art FPGA devices connected by fast serial links. We describe the status of the development of a life-size demonstrator system for the reconstruction of pixel tracking detectors, that will run on real data during Run-3.

### Summary (500 words):

With the slowdown of Moore’s law, HEP experiments are looking at heterogeneous computing solutions as a way to face ever-increasing data flows and complexity. LHCb is on the frontier of these developments due to its specific physics needs, calling for the full software reconstruction of events in real-time at the LHC average rate of 30 MHz (40 Tb/s), already in the next physics run that started in 2022. LHCb has already adopted a GPU-based solution for HLT1 for the next run, and is further researching solution for its future Upgrade-II, with a significant increase of luminosity by a factor 5÷10. To this purpose, a coprocessor testbed has been established, to allow parasitical testing of new processing solutions in realistic DAQ conditions during the current run.

One such solution under development is a highly-parallelized custom tracking processor (“Artificial Retina”). The “Artificial Retina” architecture takes advantage of FPGAs parallel computational capabilities, by distributing the processing of each event over an array of FPGA cards, interconnected by a high-bandwidth (~15 Tb/s) optical network. This is expected to allow operation in real-time at the full LHC collision rate, with no need for time-multiplexing or extra buffering thanks to its brief latency (<1  $\mu$ s).

This level of performance has never been attained before in a complex track-reconstruction task, and achieving it opens the door to early reconstruction of track primitives transparently during detector readout. These data can be used as seeds by the High Level Trigger (HLT1/HLT2) to find tracks and perform trigger decisions with much lower computational effort than possible by starting from the raw detector data. This can free an important fraction of computing power of the conventional event-processing farm, allowing more powerful and faster reconstruction at higher luminosities than otherwise possible. Implementation of this technology could enhance the physics potential of LHCb already from the following physics run (Run-4), by expanding its trigger capability with the inclusion of long-lived tracks in the HLT1 decision.

In this talk we describe the results obtained from a realistic demonstrator for a high-throughput reconstruction of tracking detectors, operated parasitically on real LHCb data from Run 3 in a supposedly built testbed facility. This demonstrator is based on an extremely parallel, ‘artificial retina’ architecture, implemented in commercial, PCIe-hosted FPGA cards interconnected by fast optical links, and encompasses a sizable fraction of the LHCb VELO pixel detector. The implications of the results in view of potential applications in HEP are discussed.

## Production, Testing and Reliability / 160

# Overview of the production and qualification tests of the lpGBT

**Author:** Daniel Hernandez Montesinos<sup>1</sup>

**Co-authors:** David Porret<sup>1</sup>; Ken Wyllie<sup>1</sup>; Paulo Rodrigues Simoes Moreira<sup>1</sup>; Pedro Vicente Leitao<sup>1</sup>; Philippa Hazell<sup>1</sup>; Sophie Baron<sup>1</sup>; Stefan Biereigel<sup>1</sup>; Szymon Kulis<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** daniel.hernandez.montesinos@cern.ch

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC used in high-energy physics experiments for multipurpose high-speed bidirectional serial links. Almost 200,000 chips have been tested with a production test system capable of exercising the majority of the ASIC functionality to ensure its correct operation.

Furthermore, specific individual qualification tests were carried out beyond the production tester limits, including radiation, multi-drop bus topology, inter-chip communication through different types of electrical links and jitter characterization.

In this paper, an overview of the production and qualification tests is given together with their results demonstrating the robustness and flexibility of the lpGBT.

### Summary (500 words):

The Low-Power Gigabit Transceiver (lpGBT) is a radiation-tolerant ASIC that is used to implement multipurpose high speed bidirectional optical links for high-energy physics experiments and in particular for the HL-LHC upgrades of ATLAS and CMS. It provides a single bidirectional link to be used simultaneously for data readout, trigger data, timing, experiment control and monitoring.

The lpGBT has many diverse features that must be tested before its delivery to ensure its correct operation. Almost 200'000 chips have been produced and tested in Q4 2022 and Q1 2023, which represents an unprecedented production volume of ASICs for the high-energy physics community. During the production testing, each chip went through an optimised process limited to thirty seconds during which all I/O connectivity and internal functions were tested. This testing process was done at three different

supply voltages and both ambient and cold (-30 °C) temperatures and allowed, in addition, to assign and fuse chip serial numbers and perform analogue calibration of the ASICs.

Nevertheless, a few complex functions could not be included in the test sequence due to the constraints imposed by production testing, in particular time and cost, and the form factor of the test system. For instance, the tester only houses one lpGBT and an FPGA emulating both the back-end and front-end electronics which, in reality, will be extremely diverse.

Hence several additional tests representing the many use-cases were performed on several samples, such as the communication of the lpGBT with other ASICs through different types of available electrical links. The characterisation of the jitter performance of the lpGBT required a relatively complex setup which could not be included in the production tests. Therefore, it was also part of the additional qualification campaign and was performed with different configurations and environments. Finally, the lpGBT has been extensively qualified under various types of radiation over several test campaigns. Complimentary to tests of tolerance to total-ionising-dose, it was also tested stand-alone with heavy ions and as part of an ecosystem (including the VTRx+ transceiver [1] and the bPol2V5 [2] and bPol12V [3] radiation tolerant DCDC convertors) in a neutron beam.

Conclusions from this extensive qualification programme formed the basis of recommendations for the diverse users in the HL-LHC community and these will be presented together with the main results from production testing.

[1] The VTRx+, an Optical Link Module for Data Transmission at HL-LHC, J. Troska et Al., DOI 10.22323/1.313.0048

[2] 2.5V step-down DCDCs: a radiation-hard solution for power conversion, G. Ripamonti et Al., DOI 10.22323/1.370.0071

[3] The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness, F. Faccio et Al., DOI 10.22323/1.370.0070

ASIC / 161

## Digital on Top methodology for Monolithic Active Pixel Sensor, feedback from MIMOSIS sensors for CBM Micro-Vertex Detector

**Authors:** Ali Murteza Altingun<sup>1</sup>; Andrei Dorokhov<sup>2</sup>; Auguste Guillaume Besson<sup>3</sup>; Christian Joachim Schmidt<sup>4</sup>; Christian Peter Muntz<sup>5</sup>; Christine Guo Hu<sup>3</sup>; Claude Pierre Colledani<sup>3</sup>; Frederic Morel<sup>3</sup>; Gilles Lucien Claus<sup>3</sup>; Grégory Bertolone<sup>None</sup>; Guy Doziere<sup>1</sup>; Hasan Darwish<sup>None</sup>; Isabelle Valin<sup>None</sup>; Jan Michel<sup>6</sup>; Jerome Baudot<sup>7</sup>; Joachim Stroth<sup>8</sup>; Joshua Benedict Arnoldi-Meadows<sup>9</sup>; Julio Andary<sup>9</sup>; Kimmo Kalevi JAASKELAINEN<sup>None</sup>; Mathieu Goffe<sup>3</sup>; Matthieu SPECHT<sup>10</sup>; Michael Deveaux<sup>4</sup>; Michal Koziel<sup>5</sup>; Oliver Michael Keller<sup>11</sup>; Roma Bugiel<sup>3</sup>; Thanh Hung PHAM<sup>12</sup>; Ziad El Bitar<sup>3</sup>; abdelkader HIMMI<sup>1</sup>; yue zhao<sup>1</sup>

<sup>1</sup> IPHC

<sup>2</sup> IPHC, Strasbourg

<sup>3</sup> Centre National de la Recherche Scientifique (FR)

<sup>4</sup> GSI - Helmholtzzentrum für Schwerionenforschung GmbH (DE)

<sup>5</sup> Goethe University Frankfurt (DE)

<sup>6</sup> Goethe University Frankfurt

<sup>7</sup> IPHC - Strasbourg

<sup>8</sup> Goethe-University and GSI

<sup>9</sup> GSI

<sup>10</sup> Université de Strasbourg / CNRS / IPHC

<sup>11</sup> CERN, Université de Genève (CH)

<sup>12</sup> CNRS

**Corresponding Author:** frederic.morel@iphc.cnrs.fr

The CMOS Monolithic Active Pixel Sensor MIMOSIS being developed for the CBM experiment at FAIR will combine a spatial resolution of 5  $\mu\text{m}$  with a time stamp of 5  $\mu\text{s}$  and operate at peak rates

of 80 MHz/cm<sup>2</sup>. The full-scale prototype MIMOSIS-1 met these specifications, and the recently submitted MIMOSIS-2 has addressed shortcomings identified during the dense test campaign. Both complex mixed-signal circuits were developed using the Digital on Top methodology. We present the sensor design, introduce our design methodology and discuss the lessons learned during the design process.

**Summary (500 words):**

Compressed Baryonic Matter (CBM) will be one of the core experiments of the future Facility for Antiproton and Ion Research (FAIR) in Darmstadt. The fixed target heavy ion experiment aims to explore the QCD phase diagram in the region of high baryon densities. The mission of its Micro-Vertex Detector (MVD) includes the determination of the secondary decay vertices, the background rejection in dielectron spectroscopy and the reconstruction of weak decays. It will consist of nearly 300 CMOS Monolithic Active Pixel Sensor (MAPS) arranged in 4 double-sided stations operating in the target vacuum of the experiment.

The dedicated CMOS Monolithic Active Pixel Sensor, called MIMOSIS, is being developed at the IPHC Strasbourg, the Goethe University Frankfurt and GSI. It is inspired by the ALPIDE sensor designed for the ALICE-ITS2, but had to be improved by one order of magnitude in terms of rate capability and radiation tolerance to meet the requirements of the CBM experiment. This required a redesign of the internal data acquisition architecture, i.e. the digital data compression and transfer logic, in order to cope with an internal peak data flow of up to 20 Gbits/sec. This flow is averaged out by an elastic buffer that allows the sensor output throughput to be limited to 2.56 Gbps. Despite the high data rate capability of this large sensor with an active area of almost 1x3 cm<sup>2</sup>, the power consumption remains as low as 50 mW/cm<sup>2</sup> at a frame rate of 200 kframe/s. This low power density is required due to the vacuum operation of the detector.

A first full-scale prototype, called MIMOSIS-1, has been developed in the 180 nm CMOS Imaging Sensor process of Tower Semiconductor, taking advantage of the deep p-well feature that allows digital circuitry to be integrated into the sensitive pixel matrix without reducing charge collection efficiency. This process has been modified to achieve full depletion of the epitaxial layer to increase radiation hardness. The sensor meets the main requirements expected from the experiment. A second prototype, MIMOSIS-2, was developed to improve the functionality of the chip and to fix some minor bugs. Although the design of both sensors is based on the Digital on Top methodology, a complete re-foundation of the design flow had to be implemented to overcome the limitations of the first approach (turnaround time, timing closure, full flat verifications, ...). In addition, the second prototype was designed using the Stylus Flowkit, a flow structure that allows users to run all Cadence digital tools. The flow was adapted to allow full flat timing and power verification of the 31.1 x 17.2 mm<sup>2</sup> sensor.

This contribution introduces the design of the sensor and discusses in detail the methods used, their limitations and the lessons learnt in applying them to the design of a reticule-sized CMOS Pixel Sensor.

ASIC / 162

## Lab measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype detector with a large breakdown voltage

**Author:** Chenfan Zhang<sup>1</sup>

**Co-authors:** Benjamin Wade <sup>1</sup>; Eva Vilella Figueras <sup>1</sup>; Jan Patrick Hammerich <sup>1</sup>; Samuel Powell <sup>1</sup>

<sup>1</sup> *University of Liverpool (GB)*

**Corresponding Author:** chenfan.zhang@cern.ch

An HV-CMOS (High-Voltage CMOS) prototype detector for particle detection in high energy physics experiments, named UKRI-MPW0, has been developed. This chip implements a novel sensor cross-section optimised for biasing the chip from the backside only and achieves an unprecedented breakdown voltage (> 600 V). With such a high breakdown voltage, UKRI-MPW0 is expected to achieve much improved radiation tolerance. The chip contains test structures for edge-TCT measurements and a array of monolithic pixels with integrated readout electronics. The design and detailed lab measurements of its pixel matrix after irradiation is presented in this contribution.

**Summary (500 words):**

The industry standard High-Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments that have extreme requirements, such as the Mu3e experiment, future upgrades of the Large Hadron Collider (LHC) and the Circular Electron Positron Collider (CEPC). As opposed to traditional hybrid silicon sensors that require bump-bonding assembly, the HV-CMOS pixel sensors integrate sensing elements and readout electronics into single pieces of silicon, thus making this technology efficient in material, production time and cost. The sensor substrate is biased to high voltages, which brings the benefits of fast charge collection by drift and high radiation tolerance up to a few  $10^{15}$  1 MeV neq/cm<sup>2</sup>.

To meet the needs of future experiments, for example in HL-LHC: single point resolution ( $25 \times 50 \mu\text{m}^2$ ), time resolution (50 ps) and radiation tolerance ( $5 \times 10^{15}$  neq/cm<sup>2</sup>), the HV-CMOS pixel sensor performance needs to be further improved. The Liverpool HV-CMOS group has developed an HV-CMOS prototype chip, named UKRI-MPW0, which aims at addressing some of these challenges. This chip is developed using the 150 nm HV-CMOS process from LFoundry. It implements a novel sensor cross-section with no substrate contacts on its top-side for backside-only biasing. I-V measurements have shown the chip is able to sustain unprecedented high bias voltages ( $> 600$  V), thus promising a large improvement in radiation tolerance. A pixel matrix of 20 rows and 29 columns (pixel size of  $60 \times 60 \mu\text{m}^2$ ) and several test structures are included in the chip.

UKRI-MPW0 chips are fabricated on two high-resistivity ( $1.9 \text{ k}\Omega\cdot\text{cm}$ ) wafers which are thinned to  $280 \mu\text{m}$  and backside processed using different methods: one with Beam-Line Ion Implantation (BLII) and Rapid Thermal Annealing (RTA), and the other one with Plasma-Immersion Ion Implantation (PIII) and UV laser annealing. Samples have been irradiated to different neutron fluences up to  $1 \times 10^{16}$  neq/cm<sup>2</sup>.

This contribution covers the design details and evaluation of UKRI-MPW0 before and after irradiation, including IV, edge-TCT measurements and the characterisation of its pixel matrix. Initial measured results show the chip can be biased to 600 V and 400 V before and after irradiation ( $1 \times 10^{16}$  neq/cm<sup>2</sup>) with leakage currents of  $\sim 1 \mu\text{A}$  and  $\sim 100 \mu\text{A}$ . The chip substrate of samples irradiated to fluences  $< 1 \times 10^{14}$  neq/cm<sup>2</sup> is fully depleted with bias voltages larger than 300 V. A depletion depth of  $> 50 \mu\text{m}$  can be achieved in samples irradiated to the fluence of  $1 \times 10^{16}$  neq/cm<sup>2</sup>. Pixels have Equivalent Noise Charge (ENC)  $< 100 \text{ e}^-$  and gain  $> 100 \text{ mV/ke}^-$  before irradiation. Figures showing the listed performance are included in the attachment. The performance of the active pixel matrix after irradiation will be presented.

A succeeding chip, UKRI-MPW1, has been designed and submitted for fabrication, which includes improvements to reduce the leakage current and eliminate parasitic channels between pixels.

**Thursday posters session / 164****Electronics Upgrade for the HADES MDC Drift Chambers**

**Authors:** Jan Michel<sup>1</sup>; Jan Michel<sup>1</sup>

**Co-authors:** Christian Müntz<sup>2</sup>; Christian Wendisch<sup>3</sup>; Joachim Stroth<sup>4</sup>; Ole Artz<sup>2</sup>; Tomasz Gniazdowski<sup>5</sup>; Volodymyr Svintozelskyi<sup>6</sup>

<sup>1</sup> Goethe University Frankfurt (DE)

<sup>2</sup> Goethe University Frankfurt

<sup>3</sup> GSI Helmholtz Center for Heavy Ion Research Darmstadt

<sup>4</sup> Goethe University Frankfurt, GSI Helmholtz Center for Heavy Ion Research and Helmholtz Forschungssakademie Hessen für FAIR

<sup>5</sup> Warsaw University of Technology

<sup>6</sup> Taras Shevchenko National University of Kyiv (UA)

**Corresponding Authors:** jan.michel@cern.ch, michel@physik.uni-frankfurt.de

The drift chambers of the HADES spectrometer at GSI, Darmstadt/Germany, form its main tracking system. Designed more than twenty years ago, the whole front-end electronics chain is being replaced with state-of-the-art electronics.

The new analog signal processing is based on the PASTTREC ASIC, developed for the PANDA Straw Tube Tracker. The digitization of data happens in FPGA-based TDCs.

The main challenges of the project are the strict spatial constraints given by the experiment setup and the noise sensitivity of the large area gas detectors. In addition, the power consumption needed to be kept low due to thermal constraints.

**Summary (500 words):**

The HADES experiment is a di-electron and hadron spectrometer at GSI / FAIR in Darmstadt, Germany. Currently it is operated at GSI's SIS-18 synchrotron and is foreseen to be moved to the FAIR SIS-100 accelerator once it becomes operational.

The central tracking part of the spectrometer is formed by the MDC (Mini Drift Chamber) detector. The original read-out electronics were built 20 years ago and start suffering from increased failure rates and missing replacement parts.

A fully new set of read-out electronics has been designed: The analog signals will be shaped, amplified and discriminated by PASTTREC, an ASIC developed at AGH Krakow for the PANDA Straw Tube Tracker. Digitization is accomplished by FPGA-based TDCs that also contain all necessary data handling, filtering and event building features. The design and operation of the existing drift chambers posed a couple of challenges to the design of the electronics that will be explained in detail.

HADES has been designed as a high acceptance spectrometer leaving minimal space for infrastructure in the gaps between sensitive detector areas. Combined with fixed and short signal cables the geometry of the new electronics was restricted to narrow and long boards. Densely packed electronics also limit the allowable power consumption as cooling is only foreseen by air, including some forced flow in the most dense regions.

Another crucial aspect is the design of the powering scheme. Noise sensitivity of the detector does not allow for switching power supplies close to the read-out electronics. On the other hand, the distance to power supplies varies substantially (up to 15 m) and local power dissipation has to be kept low. The solution was a distributed scheme, employing adjustable low-noise DCDC converters just outside the detector and on-board LDO regulators for precise adjustment.

Further design considerations include easing installation and replacement operations. All connections for power, data and flex signal cables are located on Add-On boards that can easily be connected and removed in hardly accessible spaces. These Add-Ons also contain the whole signal filter and protection circuits as these are the components most likely to fail over time when subject to high-voltage discharges inside the detector.

The digital electronics stage is based on Lattice ECP5 FPGA that provide a low-power and low-cost platform to implement digitization and communications. Time measurement is accomplished by a common clocked TDC design running at a average bin size of 400 ps (140 ps RMS). Data is filtered by applying spike rejection and trigger windows before it is forwarded to the data collection servers. All communications are based on the existing HADES DAQ network TrbNet that provides full control and monitoring access, triggering and busy time controls.

We are going to present a comprehensive summary of the read-out electronics and the design considerations leading to the final solution.

**Thursday posters session / 168**

## **Design and measurements of SMAUG1, a prototype ASIC for voltage measurement using noise distribution**



**Authors:** Grzegorz Jan Wegrzyn<sup>1</sup>; Grzegorz Jan Wegrzyn<sup>2</sup>; Robert Szczygiel<sup>3</sup>

<sup>1</sup> CERN

<sup>2</sup> AGH University of Cracow

<sup>3</sup> AGH University of Cracow

**Corresponding Authors:** grzegorz.jan.wegrzyn@cern.ch, wegrzyn@agh.edu.pl

In this work, we present the design, test system, and measurement results of the SMAUG\\_ND\\_1 ASIC. The described circuit implements an indirect energy measurement algorithm based on noise distribution measurement. The algorithm is similar to the threshold scan procedure but is done with a single pulse. The chip implements the matrix of 7x7 pixels each with 8 independent comparators and a size of 75x75um. The work describes the measurement process and the results of the algorithm as well as a brief discussion of what can be improved in the next version of the ASIC.

### Summary (500 words):

SMAUG\\_ND\\_1 is a prototype ASIC, developed in CMOS 28nm technology, which is designed to test the algorithm for voltage measurement using a noise distribution. This algorithm is similar to the threshold scan procedure. The main difference is that it is performed on a single pulse instead of a series of pulses and simultaneously utilizes multiple threshold levels. The idea is to fit the Gaussian curve to get a higher energy resolution than widely used  $CR - RC^2$  filters with amplitude or ToT measurements. The tested algorithm was described in our previous work [1].

The main challenge was related to the accurate distribution of threshold levels which positions should be well known to be useful in the mentioned algorithm. Therefore we had to implement fine-tuning DAC within each comparator. The next possible source of errors is the difference between the speed of comparators, which also can be trimmed using dedicated DACs, separated for each comparator (fig 1.).

Another requirement was related to the charge-sensitive amplifier (CSA) which is used as the very first stage of the processing chain. CSA should work in charge integrating mode to provide a possible flat response, which will be easy to measure using the mentioned algorithm. Therefore as a CSA feedback, we used the simple transistor whose gate potential can be controlled by an external voltage source. At the time of measurement, the transistor is in the off state, and just after measurement, it can be easily turned into an active state to discharge the preamplifier. To minimize gate leakage currents that can discharge feedback capacitance we decided to use thick oxide transistors as an input transistor and in the feedback.

The chip provides 8 comparators in each channel to increase the accuracy of further Gaussian curve fitting. Comparators are divided into two banks with separated DACs for coarse tuning of the threshold. This allows the tested algorithm to be combined with correlated double sampling [2]. To increase the maximum counting rate, we have not implemented hysteresis in the comparators. Each discriminator is connected to a 16-bits ripple counter.

The initial measurements show a problem with the analog buffer, which has a very limited dynamic range compared to the simulation. Nevertheless, the available range is still sufficient to check the linearity of the internal DACs for fine-tuning the threshold (see fig. 2). The comparator's count rate measurement shows a relatively large mismatch (compare the height of the bars in fig. 3.), so if the comparator count rate trimming is not sufficient, normalization will be necessary.

The goal of the first prototype is to confirm if we can achieve the required parameters and check if the algorithm will work. At the time of writing this abstract, ASIC is under testing and final data is not yet available. Detailed results will be reported at the time of the conference.

[1] - G. Wegrzyn, R. Szczygiel, "Voltage Measurement Using Noise Distribution", 2021

[2] - W. Buttler et al. "Noise Filtering for Readout Electronics", 1990

## Time and Clock Distribution Over a Hierarchy of Deterministic Optical Links

**Authors:** Vladimir Sidorenko<sup>None</sup>; Walter Mueller<sup>1</sup>; Wojciech Zabolotny<sup>2</sup>; Ingo Froehlich<sup>3</sup>; David Emschermann<sup>4</sup>; Jürgen Becker<sup>5</sup>

<sup>1</sup> *Unknown*

<sup>2</sup> *Warsaw University of Technology (PL)*

<sup>3</sup> *Goethe-University*

<sup>4</sup> *GSI - Helmholtzzentrum für Schwerionenforschung GmbH (DE)*

<sup>5</sup> *KIT*

**Corresponding Author:** vladimir.sidorenko@kit.edu

Accurate clock and time distribution is a key requirement for self-triggered streaming data acquisition in the CBM experiment. This distribution is handled by the Timing and Fast Control (TFC) system by clock forwarding and broadcasting the common time over latency-deterministic optical links in a hierarchical FPGA network. The point-to-point optical connections are served by the latency-optimized GBT-FPGA core, which has been developed at CERN. In the presented work, the performance of GBT-FPGA links for time and clock distribution in a scaled TFC system with multiple hops and endpoints has been investigated.

### Summary (500 words):

The future Compressed Baryonic Matter (CBM) experiment aims to study strongly interacting matter at high baryonic densities by measuring rare diagnostic probes at interaction rates of up to  $10^7$  events per second. Due to the complexity of the potential trigger signatures, this approach requires at least partial event reconstruction to select events of interest. To facilitate this, the CBM experiment will be equipped with a streaming data acquisition (DAQ) system with self-triggered front-end electronics (FEE). Event reconstruction and selection is time-based and will be completely performed online by software running in a computing farm.

Up to 1 TB/s of timestamped experimental data is produced by the FEE and concentrated into optical links using the readout boards (ROB) based on the GBTx chipset. The 4.8 Gb/s optical links transfer the data to a layer of about 200 PCIe-based Common Readout Interface (CRI) boards. The CRI boards are equipped with an FPGA that reformats the data before passing it on to the First-level Event Selector (FLES) cluster for event reconstruction. This readout scheme requires that a common clock signal, together with the time information for accurate and coordinated timestamping, are provided by the CRIs to the FEE via the ROBs. This is achieved by leveraging deterministic downstream clock and data transport capability of GBTx ASICs. The time and clock in the CRI boards, however, must be synchronized independently, which is handled by the Timing and Fast Control (TFC) system. Here, the clock phase stability requirements of the FEE define the requirements for the distribution of common clock and time. To accomplish this task, the TFC system takes the approach of forwarding the clock and time messages from a central master node over an optical network of FPGA boards to the individual CRIs. The challenge of this approach is to ensure sufficient determinism of both phase of the forwarded clock and the time message latency in a tree network, without interfering with the latency-critical Fast Control messages. The relative clock and time offset in all endpoints must be stable to a maximum of 200 ps at all times, including full system restarts.

Implementation of the proposed approach requires the optical point-to-point connections in the hierarchical network to be deterministic in the downstream direction (TFC master to CRIs). Here, the GBT-FPGA core has been selected, as it features latency-deterministic datapaths by design. Whereas latency determinism of a direct GBT-FPGA connection between two FPGA devices has been verified, it requires further study to characterize the downstream link latency determinism of the entire TFC network. With the goal of generating sufficient insight to estimate the quality of clock and time distribution in the final experimental setup, the current work focuses on characterizing latency variance over multiple hops, as well as relative time error between multiple endpoints.

## High-speed front-end electronics and digitisation system for the Crilin calorimeter with enhanced timing performance

**Author:** Daniele Paesani<sup>1</sup>

<sup>1</sup> LNF-INFN

**Corresponding Author:** daniele.paesani@lnf.infn.it

Crilin –a semi-homogeneous, longitudinally segmented highly granular electromagnetic calorimeter with Cherenkov PbF<sub>2</sub> crystals has excellent timing and improved radiation resistance. A two-channel front-end prototype was tested at CERN-H2 with 120 GeV e- using PbF<sub>2</sub> and PWO-UF crystals, yielding a single-cel timing resolution <30 ps for energy deposits <3 GeV. Crilin prototype consists of two sub-modules, housing a 3-by-3 crystal matrices and layers surface-mount 10 um pixel-size UV-extended SiPMs, handled via a fully custom microprocessor-controlled front-end, providing signal amplification/shaping and all slow control functions. The relative CAEN-V1742 based 5Gsp/s digitisation system employs a custom ultra-low-jitter trigger distribution electronics.

### Summary (500 words):

Crilin - a semi-homogeneous, longitudinally segmented electromagnetic calorimeter concept based on Cherenkov PbF<sub>2</sub> crystals, features fine granularity, excellent timing, good pileup capability and energy resolution, along with improved radiation resistance. Its modular architecture, featuring stackable and interchangeable sub-modules, allows crystals granularity, transversal and longitudinal dimensions scaling to maximize performance. Crilin was optimised in the ambit of the Muon Collider experiment as a candidate for an electromagnetic barrel calorimeter. Its architecture was also adopted as a candidate for the Small-Angle-Calorimeter for the HIKE experiment. A two channel Crilin front-end prototype was tested at CERN H2 using 120 GeV e- beams, to study light collection dynamics, and validate the readout chain using PbF<sub>2</sub> and novel PWO-UF crystals. A timing resolution < 30 ps for energy deposits > 3 GeV can be expected from a single calorimeter cell.

In its current design, Crilin prototype (Proto-1) consists of two sub-modules, each composed of a 3-by-3 crystals matrix and a photosensor board housing a layer of 36 surface-mount 10 um pixel-size UV-extended SiPMs –thermalized using an additively manufactured micro-channel heat exchangers – so that each crystal has two independently processed and digitized readout channels, composed by the series connection of two photosensors. SiPMs are handled via micro-coaxial transmission lines by a remote fully custom microprocessor-controlled front-end system. Each front-end houses a two-stage high-speed current-feedback amplifier and a pole-zero shaper for a total of 18 readout channels, while providing individual bias regulation, temperature, and current monitoring –for all photosensors. A high-speed switched-capacitor array digitization system based on CAEN V1742 DRS4 modules, employing a custom ultra-low-jitter trigger distribution and synchronization electronics, is being developed to allow Crilin Proto-1 digitisation at 5 Gsp/s and handle its improved timing performances.

A full description of the system and the qualification of custom high-voltage linear regulators, amplification, and digitisation stages will be shown. The custom trigger distribution allows a DRS4 synchronisation with a 5 ps channel-to-channel (within the same chip) and 30 ps board-to-board jitter capabilities, still under improvement.

Pictures of Crilin's front-end and SiPM boards are shown in attachment along with a photo of the assembled Crilin Proto-1.

**Programmable Logic, Design and Verification Tools and Methods / 171**

## Towards Single-Event Upset detection in Hardware Secure RISC-V processors

**Authors:** Boris Engelen<sup>1</sup>; Jeffrey Prinzie<sup>1</sup>; Karel Appels<sup>1</sup>; Levi Marien<sup>1</sup>; Nain Jonckers<sup>None</sup>

<sup>1</sup> KU Leuven

**Corresponding Author:** jeffrey.prinzie@kuleuven.be

An increasing interest is growing towards reconfigurable processing systems embedded on the detector ASICs. Explorative work has been carried out to investigate Single-Event Upset (SEU) rates in open source RISC-V processors. The Ibex RISC-V core includes hardware security features that could detect SEUs in the core and alert the System-on-Chip (SoC) for possible malfunctions. This research addresses the possibility to rely on such hardware secure extensions for radiation hardness assurance.

**Summary (500 words):**

Single-Event Effects and hardware security show close similarities in terms of vulnerabilities and mitigation techniques. Secure processors address external physical attacks such as external laser stimulation to compromise the program and extract sensitive information from the systems. To overcome this vulnerability, hardware secure architecture extensions are often included in modern processor cores. These include dual program counters, EDAC on the register files and memories and even lock stepping in the CPU pipeline. Such features are highly similar to SEU protection done in spacecraft processing systems such as the LEON-FT and NOEL-V processors, commonly used in satellites. Provided by the limited design resources often found in space or high-energy physics experiment design teams, this paper addresses to which extend hardware secure architectures can be a reliable source to detect SEUs in the processor.

The Ibex open source RISC-V processor has been evaluated in simulation with extensive fault injection. The Ibex core has a hardware security option which can be enabled. This extensions enables a dual CPU pipeline, HSIAO code in the register file and the main instruction and data memories. Although the core does not intend to perform error correction, it provides 3 alert signals that flag possible security issues due to external attacks, henceforth compromising the program flow.

A simulation environment was developed using CoCoTB that includes the Ibex RISC-V instance along with several python models to model the SoC, such as memories, monitors, IO, etc. Fault injection was performed using an initial synthesis pass with Cadence Genus to list all flip-flops in the design. Random bit flips are stimulated from a CoCoTB coroutine. A monitor coroutine monitors critical CPU signals such as memory ports, register file, program counter, status registers, etc. Each cycle, a CRC is calculated on all these ports, providing a signature. Before SEU injection, a golden reference simulation is performed to calculate the correct CRCs on a cycle basis. Afterwards, during SEU injection, the CRCs are continuously compared.

The testbench checks if the Ibex alert signals are asserted if an error is encountered in the CRC check. If the core can successfully detect malfunction, it can be mitigated at system level later on. However, undetected errors can lead to problematic operation. During the tests, the Dhrystone benchmark was ran on the core.

Fault injection results showed that 10 % of all injected SEUs led to an error on the CPU (note that the memories were not stimulated). For SEUs that didn't lead to an error only 4% showed a false positive alert signal. For SEUs that did lead to an error, 88 % was detected by the CPU alert signals. The register file as well as the lockstep core are all detectable. Only the instruction fetch and load store unit can only detect 54% and 36% of all errors respectively.

Based on these results, we can conclude that relying on existing hardware security architectures could be a viable alternative to developing a custom SEU tolerant architectures.

**Module, PCB and Component Design / 172**

## **The development of a laser system for use in the timing performance measurements of CMS HGICAL silicon modules**

**Author:** Fakhri Alam Khan<sup>1</sup>

**Co-author:** Matt Noy<sup>2</sup>

<sup>1</sup> *Universite Libre de Bruxelles (BE)*

<sup>2</sup> *CERN*

**Corresponding Author:** fakhri.alam@cern.ch

For optimal operations in the high radiation and pileup environment of the HL-LHC, the CMS-HGICAL requires precise timing information at the level of 30ps (RMS) for a particle shower. The

time measurement in Silicon detector modules is performed using a per-channel time-of-arrival discriminator coupled with charge measurement to correct for the time-walk. The module design includes access holes in the PCB and in the sensor passivation to enable infrared laser light to be injected directly into the sensor cells. We present the calibration and timing-in of the system used to perform measurements as well as the module time performance results.

#### Summary (500 words):

The Large Hadron collider will enter the High Luminosity phase of operations in the last quarter of this decade. High radiation levels and large pile-up (on average of 200 collisions simultaneously) will be major challenges for the HL-LHC operations. Studies show that there will be a spread of interaction vertices in position of approximately  $\pm 50$  mm along the beam axis, and in time of approximately  $\pm 150$  ps. Detector simulation studies indicate that the physics potential can be improved by mitigating events pileup through time-tagging events with a precision of  $\sim 30$  ps (RMS). To cope with all these challenges, the present CMS endcap calorimeters ECAL and HCAL will be replaced by the new High Granularity Calorimeter (HGCal). The HGCal is a 47-layer sampling calorimeter based on lead and stainless-steel absorbers, with 620 m<sup>2</sup> of silicon active layers in the high occupancy regions and  $\sim 370$  m<sup>2</sup> of scintillating plastic tiles read-out by SiPM in the low occupancy regions. Both endcaps of the HGCal will be instrumented with  $\sim 28$ K silicon detector modules (usually known as Hex-module) which is the glued assembly of Hexaboard PCB with silicon-sensor, Kapton foil and base plate, where the bonding pads from Hexaboard are bonded to silicon sensor via stepped hole structures. The Hexaboard is the front-end read-out board for the silicon Hex-module incorporating radiation hard ASIC HGCROC. The HGCal front-end electronics have very stringent specifications of low noise ( $< 2500$  e<sup>-</sup> for 65 pF silicon sensor), large dynamics range (0.2fC to 10pC) and the capability to measure time of arrival (TOA) for hits having charge  $> 12$  fC with precision better than 100 ps. To validate the Hex-module timing performance, the Hexaboard design includes 1 mm diameter holes in the center of silicon cell, which are coincident with openings in the sensor passivation to allow the injection of short (100ps FWHM), infrared (1060 nm) high time resolution laser pulses directly into the silicon sensor sensitive layers. The synchronization of the laser subsystem with the Hex-module clock distribution and DAQ system is of critical importance and great care has been taken to attain this to better than 20 ps (RMS), whilst still allowing the timing of the light injection to be stepped relative to the Hex-module clock and trigger signal in steps of less than 10 ps. The laser light is delivered through a micro-focal lens, giving a FWHM spot size of less than 10  $\mu$ m. The laser system equipped with X, Y, Z stages permitting the automated movement of the Hex-module relative to the micro-focal lens, allows automated channel selection, and optimizing spot size. The light intensity, translating to the charge injected into the sensor, can be selectively attenuated from 2.58 dB to 50 dB using an attenuator inserted into the fibre network. This combination permits a detailed investigation of the Hex-module performance of over these parameters. A detailed description of the laser system and the timing-in procedure, as well as the performances of both the laser system and the Hex-module will be presented.

#### Thursday posters session / 173

### Proof of principle for a novel PET detector

**Authors:** Alberto Gola<sup>1</sup>; Andrej Seljak<sup>2</sup>; Andrej Studen<sup>2</sup>; Antonio Mariscal Castilla<sup>3</sup>; Constantino Morera<sup>4</sup>; Daniel Guberman<sup>5</sup>; David Gascon<sup>3</sup>; Elena Moretti<sup>6</sup>; Gabriel Pavon<sup>7</sup>; Gašper Razveršek<sup>8</sup>; Georges El Fakhri<sup>9</sup>; Joan Mauricio<sup>3</sup>; Jorge Alamo<sup>10</sup>; Jose Benloch Baviera<sup>11</sup>; Jose Maria Benloch Rodriguez<sup>None</sup>; Jose Maria Fernandez-Tenllado Arribas<sup>12</sup>; Julio Barbera<sup>None</sup>; Kira Suzanne Grogg<sup>9</sup>; M. Penna<sup>13</sup>; Matic Orehar<sup>None</sup>; Peter Krizan<sup>None</sup>; Rafel Manera Escalero<sup>3</sup>; Rok Dolenc<sup>2</sup>; Rok Pestotnik<sup>2</sup>; Samo Korpar<sup>None</sup>; Sergio Gomez Fernandez<sup>3</sup>; Stan Majewski<sup>14</sup>; Stefano Merzi<sup>None</sup>; Thibault Marin<sup>9</sup>

<sup>1</sup> *Fondazione Bruno Kessler*

<sup>2</sup> *Jozef Stefan Institute (SI)*

<sup>3</sup> *University of Barcelona (ES)*

<sup>4</sup> *Oncovision*

<sup>5</sup> *Institut de Ciències del Cosmos (ICCUB)*

<sup>6</sup> *Fondazione Bruno Kessler (FBK), Trento, Italy*

<sup>7</sup> *Oncovision, Valencia, Spain*

<sup>8</sup> *Jožef Stefan Institute, Ljubljana, Slovenia*

<sup>9</sup> *Gordon Center for Medical Imaging and Harvard Medical School, Boston, MA 02114, United States*

<sup>10</sup> *ONCOVISION*

<sup>11</sup> *IBM Molecular Imaging Research Institute, Valencia, Spain*

<sup>12</sup> *CERN*

<sup>13</sup> *Fondazione Bruno Kessler, 38123 Povo TN, Italy,*

<sup>14</sup> *University of California, Davis*

**Corresponding Authors:** andrej.seljak@cern.ch, andrej.seljak@ijs.si

The interplay between High Energy Physics and Positron Emission Tomography detector development keeps providing encouraging outcomes of mutual interest, most notably observed in the development of scintillators, photon detectors, as well as the physics simulation tools. Our group develops PET detectors with the time of flight ability. In this work we present the 16-channel prototype which uses FBK SiPMs and the FastIC ASIC. The prototype has a 3mm pixel pitch and uses LYSO crystals for gamma detection. We present the construction, calibration, measured results and discuss future development directions.

#### **Summary (500 words):**

In time of Flight PET it is crucial to register gamma photons with very high precision. Following the latest developments, we integrate the novel low power FastIC ASICs with HV-NUV-MT SiPM array from FBK into a sensor module, and couple it to a LYSO crystal. The 8 channel FastIC is a front-end ASIC which employs a low power circuitry to discriminate down to single photon signals from various photon detectors. With its power consumption of 12 mW/ch for the default settings, and an input range between the 5  $\mu$ A–25 mA peak current it can cover both positive and negative signals. Its basic output provides the time of arrival signal via the SLVS differential standard, and can be read by an external device like an oscilloscope or external TDC. In addition, it outputs a second signal where the width is proportional to the peak height information. Its functionality was already evaluated in coincidence single channel setup [1] In this work we evaluate a system with multiple channels. We developed a small prototype using 2 ASICs which combined provide a total of 16 readout channels. This 6-layer board is also equipped with local LDO power supplies, biasing circuits and temperature sensors, and can be seen on Figure 1. Half of the SiPMs are read in common cathode mode, while the other is in common anode featuring separate overvoltage bias supply filter for each SiPM. The other electrode of the photodetector is connected directly in into the ASIC's input channel. The selection of scintillating crystals remains flexible, as an external 3D printable holder housing the crystals can be attached on top of the fixed SiPM array. Multiple boards were produced to increase the statistical information outcome, and a separate custom FPGA unit is used for loading of slow control parameters. Finally, data from the 16-channel module are wired straight into a Caen HPTDC with 25ps resolution, and to a more precise system using the PicoTDC [2]. Our final goal is to develop a photodetector that will be used in the next generation imaging device, e.g., for medical [3] and HEP applications (RICH particle identification). In this work we explore the performance and provide a substantial amount of data for image reconstruction studies. In the contribution we will present the module construction, calibration, and obtained results.

**Module, PCB and Component Design / 174**

## **Constant Fraction Discriminator for NA62 experiment at CERN**

**Authors:** Michal Zamkovsky<sup>1</sup>; Peter Lichard<sup>1</sup>

<sup>1</sup> *CERN*

**Corresponding Author:** michal.zamkovsky@cern.ch

The newly build Constant Fraction Discriminator (CFD) with an additional Time over Threshold (ToT) measurement capabilities designed by Peter Lichard, CERN, will be presented. It operates in a wide dynamic range 1:150, with an excellent time resolution better than 70 ps over one order of magnitude. It is highly customizable for a different signal shapes and thresholds, thanks to a remotely programmable parameters through the DCS commands. Two outputs, each in NIM and LVDS standard, provide ToT information with programmable thresholds. The technical specification and performance measured with cosmic rays and in the high-intensity experiment will be shown.

**Summary (500 words):**

A demand from new VetoCounter detector at NA62 experiment, CERN, for a processing of an analog signals from the fast photomultiplier (rise times around 1 ns) in a wide dynamic range of 1:30 with a time resolution better than 200 ps led to the development of the new performant Constant Fraction Discriminator (CFD).

The leading edge discriminator timing performance suffers from time walk caused by varying signal amplitude while threshold is fixed.

The original CFD was proposed to eliminate this time walk by introducing variable threshold following the signal amplitude. The constant fraction of input signal is subtracted from full amplitude delayed input signal.

The final signal has a zero crossing point (walk) which is fixed for signals with different amplitudes.

The schematic sketch of the CFD functionality is shown in Figure 1.

The two important parameters are signal delay 'Td' and signal fraction 'k'.

They depend on the rise time of the signal and the its shape, respectively.

To preserve the signal amplitude and signal to noise ratio, in active CFD, the input signal is not attenuated but delayed signal is amplified by inverse attenuation ratio.

The presented active CFD allows to vary 'Td' by choosing internal PCB traces of different lengths on the prepared pads on the board.

Also, the signal fraction can be changed, either remotely through the DCS commands, or by a potentiometer mounted directly on the board.

In the same way one can vary other parameters, such as walk level, window, low and high thresholds.

The window threshold triggers the CFD, which output enters two SFDR shapers followed by comparators representing low and high thresholds.

They preserve the leading edge triggered from CFD, ensuring the precise timing, and set the trailing edge depending on the time over threshold measurement.

If the signal from CFD does not pass some of these thresholds, it outputs a fixed length signal.

The presented CFD provides a double output of LVDS and NIM signals for each, low and high thresholds.

The CFD was tested and its functionality verified with the cosmic rays, using Hamamatsu R9880U photomultiplier with the BC408 scintillator tile.

The tests were performed also with the pulse generator, varying the input signals in the range from 30 mV up to 4.5 V.

The measured performance with signal amplitudes in the range of 100 mV to 1 V shows an excellent time resolution of 70 ps.

It was successfully installed and commissioned in the NA62 experiment, to process signals from the VetoCounter scintillator detector, which has a large dynamic range of pulses.

The presented CFD demonstrated its functionality and performance in the NA62 experiment and can be used in other installations, where the precise timing over a wide range of the input amplitudes is required.

**Thursday posters session / 175**

## **A prototype readout system for the beam monitor at the CSR external-target experiment**

**Authors:** Bihui You<sup>None</sup>; Chaosong Gao<sup>None</sup>; Hulin Wang<sup>None</sup>; Jun Liu<sup>1</sup>; Xiangming Sun<sup>None</sup>; Zhen Wang<sup>None</sup>

<sup>1</sup> *Central China Normal University CCNU (CN)*

**Corresponding Author:** junliu@mail.ccnu.edu.cn

Beam monitor is a sub detector for the CSR external-target experiment (CEE) at HIRFL, which is designed to monitor the beam status. A custom-designed pixel chip Topmetal-CEEv1 acts as the sensor for locating the position of each particle. In this paper, we present a prototype readout system for beam monitor. Injected pulse test and 241Am alpha test in the laboratory as well as beam test at HIRFL has been done to validate the functionality of the system. The results show that the system could control and configure the pixel chips and read out data from the front end electronics.

**Summary (500 words):**

The Cool Storage Ring (CSR) of the Heavy Ion Research Facility in Lanzhou (HIRFL) is a powerful machine to probe the uncharted nuclear physics field, delivering a variety of heavy ions of element from carbon to uranium and with energies up to 1 GeV/u. The External-target experiment (CEE) at HIRFL-CSR, which is designed to study the nuclear matter phase structure at low temperature and low baryon density, is currently under development. Beam monitor is a sub detector of CEE, which is designed to monitor the beam status. Topmetal-CEEv1, a custom designed pixel chip, acts as direct charge sensor for locating the position of each particle. In order to configure the pixel chips and read data from the front end electronics, a prototype readout system is designed for beam monitor.

The system consists of a bonding board, a front end board and a readout unit. There are four TopmetalCEEv1 chips on top side of the bonding board and they are placed in three rows. With this layout scheme, no dead detection area is left and the effective detection area can reach more than 50 mm to meet the requirements. The front end board is designed to provide the required power, configure TopmetalCEEv1 chip, convert the analog signals, package data and transfer it to back end. As the distance between these two boards and the readout unit (back end) is about 10 meters, a SAMTEC cable is used to transmit power supply and high speed serial signals. Moreover, these two boards are placed inside a magnetic shield in the dipole magnet, the structure and size of the boards, radiation hardening of the devices and cooling are all need to carefully consider. The readout unit is a board based on Xilinx Kintex-7 FPGA. It could receive clock and trigger signals from clock and trigger system. And it could transmit data using transceivers in FPGA with front end board. The interface between the readout unit and the DAQ/PC is the optical fiber/Gigabit Ethernet.

The firmware architecture is divided into physical layer, data link layer, transport layer and application layer. The first three layers are mainly for data stream transmission, while the application layer is mainly for data stream processing. Data stream transmission part is implemented based on Xilinx FPGA transceiver and the widely used high-speed serial communication protocol Aurora 8b/10b. And the transmission protocol between modules is AXI-Stream. For data stream processing part, data stream merging, preprocessing and command distribution are implemented. The standard protocol and interface can effectively increase the independence between layers, reduce the coupling between modules, and make the firmware easy to modify, migrate, and maintain.

The prototype readout system has been designed and the corresponding boards have been produced. Injected pulse test and 241Am alpha test in the laboratory as well as beam test at HIRFL has been done to validate the functionality of the system. The results show that the system could control and configure the pixel chips and read out data from the front end electronics.

**Thursday posters session / 176**

## **Design of the ASIC readout scheme for the JUNO-TAO experiment**

**Author:** Manhao Qu<sup>1</sup>

<sup>1</sup> *IHEP*

**Corresponding Authors:** jie.z@cern.ch, qumh@ihep.ac.cn



One of the main objectives of the Taishan Antineutrino Observatory (TAO) is to accurately measure the reactor neutrino energy spectrum to provide precise input to the Jiangmen Underground Neutrino Observatory (JUNO). In this study, we designed a full potential readout system for TAO based on the Klaus6 chip. We also developed a mockup prototype based on the design, which includes 4 chips (up to 128 channels). The performance of the prototype has been carefully evaluated both at room temperature and at  $-50\text{ }^{\circ}\text{C}$ . Good performance is obtained on gain uniformity, charge linearity, equivalent charge noise, dynamic range, and recovery time.

**Summary (500 words):**

The TAO detector requires 4024 SiPMs to be installed, so a large number of readout channels are needed in the electronics section. Compared with usual discrete readout systems, using ASICs as SiPM readout systems has the advantages of high integration and good performance, which can simplify the design of the whole electronics readout system.

In order to meet the requirements of the TAO experiments on electronic charge noise, time resolution, dynamic range, power consumption. We investigated many current ASIC chips that might be used as SiPM readout. In this paper, we show the comparison of these chips in terms of these parameters and introduce the performance of the Klaus6 chip finally selected in detail.

This paper designs a complete ASIC readout system for the TAO detector, mainly divided into two parts: Front-End Board (FEB) and Front-End Controller (FEC). FEB is used as front-end interface board for SiPM, which has a Klaus6 chip and a high voltage connector to provide bias voltage to the SiPM. Every four FEBs are cascaded together (up to 128 channels). On the last FEB, the HDMI connector, power distribution network, configuration bus and readout driver are designed. FEC is used for control and readout, which consists of the Front-End Electronic (FEE) board and the Rear Transfer Module (RTM) board, which are connected through the backplane connector and placed in the Micro-TCA (Telecom Computing Architecture) chassis.

In addition, this paper designs an ASIC readout prototype system and introduces it from both the hardware and software aspects. The performance of the prototype has been carefully tested both at room temperature and at  $-50\text{ }^{\circ}\text{C}$ . The results show that Klaus6 has good performance at the tested temperatures with no significant degradation of the charge noise, charge linearity, gain uniformity and recovery time, all of which meet the requirements of TAO.

Therefore, this ASIC readout system has very good application prospects and can serve as an important reference for many similar experiments.

**Tuesday posters session / 177**

## **Development of a multi-purpose DAQ system for Timepix4-based detectors.**

**Authors:** Angelo Cotta Ramusino<sup>1</sup>; Massimiliano Fiorini<sup>1</sup>; Michael Campbell<sup>2</sup>; Nicolo Vladi Biesuz<sup>1</sup>; Riccardo Bolzonella<sup>3</sup>; Viola Cavallini<sup>1</sup>; Xavi Llopart Cudie<sup>2</sup>

<sup>1</sup> *Universita e INFN, Ferrara (IT)*

<sup>2</sup> *CERN*

<sup>3</sup> *University of Ferrara and INFN*

**Corresponding Author:** nicolo.vladi.biesuz@cern.ch

We present the development of a data acquisition system dedicated to detectors using the Timepix4 ASIC, developed in 65nm CMOS technology by the Medipix4 Collaboration, as integrated front-end.

A control board is needed for system configuration and data acquisition, up to the maximum bandwidth of 160 Gbps. To avoid the need for multiple custom boards, we designed a system based on commercial hardware and a user-configurable open-source firmware and software allowing for reusability and scalability of the system.

**Summary (500 words):**

We present the development of a configurable data acquisition system for detectors using the Timepix4 ASIC as an integrated front-end.

We will describe the methodologies that used to allow for full firmware flexibility.

The Timepix4, developed by the CERN Medipix4 Collaboration, is a  $65\text{-nm}$  CMOS ASIC. The ASIC implements a matrix of  $512 \times 448$  bump-pads pixels representing the analog input. Data coming from the pixel matrix are processed and the Time-over-Threshold and Time-of-Arrival in

We propose a fully customizable system based on commercial hardware and standard communication protocols. Customization of the system is provided by an open-source fully configurable firmware, described here.

The system is based on a Xilinx KCU105 development kit and uses a standard VITA 57.1 connector as interface. A combination of the IPbus protocol and firmware and of the use of Hog features allows for an easy configuration. As shown in Figure, the firmware top level module is divided in three main blocks.

A  $1\text{-GbE}$  connection provides communication with a remote server for configuration. This module is connected to a set of slaves used to configure the detector and ancillary electronics. Finally a fully configurable high speed data-path allows for read back of output data through two  $10\text{-GbE}$

The slaves needed to configure a specific system are selected at project creation, thus avoiding the need for a custom board. The customization is based on a bash that allows to interactively select the slaves to be instantiated. At the end of the customization process, a project is automatically generated and compiled, users can

Data coming from the Timepix4 output links are sent to an optional data-reduction logic, provided by a router followed by a merger logic provides a data path to the output  $10\text{-GbE}$  links. As shown only 8 out of the 16 Timepix4 links are routed to the FPGA, furthermore the presence of 2  $10\text{-GbE}$  systems needing the full Timepix4 output bandwidth can avoid this bottleneck by disabling this logic.

We presented the approach used to develop a firmware for a fully configurable data acquisition system. This system is composed by a commercial hardware and open-source firmware and software.

Both the firmware and software can be configured to tailor the requirements of different detectors. The system is currently under development and a prototype system has shown good results.

**Tuesday posters session / 178**

## **AstroPix: A novel HV-CMOS pixel sensor for space-based experiments**

**Author:** Nicolas Striebig<sup>1</sup>

**Co-authors:** Ivan Peric<sup>1</sup>; Richard Leys<sup>1</sup>

<sup>1</sup> *KIT - Karlsruhe Institute of Technology (DE)*

**Corresponding Author:** nicolas.striebig@cern.ch

A new application for monolithic pixel detectors is NASA's AMEGO-X project [1], which is a low-orbit gamma ray observatory for multimessenger astrophysics, proposed as a 3 to 5 year mission. For the 40-layer gamma-ray telescope, which will consist of over 64000 sensors with a total area of more than  $25\text{ m}^2$ , a new low power  $< 2\text{ mW/cm}^2$  and high dynamic range 20 –600 keV monolithic active pixel sensor with 500  $\mu\text{m}$  depletion thickness, named AstroPix, is currently being developed.

**Summary (500 words):**

The first two versions, AstroPix1 a  $5 \times 5\text{ mm}^2$  test chip with  $18 \times 18\ 200 \times 200\ \mu\text{m}^2$  pixels and AstroPix2 a  $1 \times 1\text{ cm}^2$  test chip with  $35 \times 35\ 250 \times 250\ \mu\text{m}^2$  pixels have already been designed and fabricated in TSI's 180nm process. The energy resolution and the SEU and latchup performance required for the usage in space are currently studied in test beams [2]. The newest version AstroPix3, has been submitted for fabrication in July 2022 and received back in January 2023.

This prototype is the first full reticle chip with  $300 \times 300 \mu\text{m}^2$  large pixels and a  $500 \mu\text{m}$  pitch. It features a new guard ring design expected to withstand a reverse bias of over 300 V, which is needed to reach the required  $500 \mu\text{m}$  depletion thickness on a  $> 10\text{k}\Omega\text{-cm}$  resistivity substrate.

The AMEGO-X tracker will consist of 4 towers with 40 layers, each embedding  $20 \times 20$  pixels. To simplify the module construction, AstroPix features a daisy-chain QSPI interface, which allows chip-to-chip readout and configuration, occupying only 5 data lines per SPI-bus on the DAQ for multiple chips. All bias currents and voltages need are internally generated by 6-bit current and 10-bit voltage DACs. The analog in-pixel front-end consists of a charge-sensitive amplifier implemented as n-type cascode amplifier with an additional feedback capacitance to increase the dynamic range, a band-pass filter, and a CMOS comparator converting the analog pulse to a digital signal. Pixels are or'd in row and column, to reduce the number of readout channels to the sum of rows and columns. To reduce crosstalk between the long metal traces connecting the pixel and the synthesized digital logic in the bottom periphery of the chip, the or'd signal is level shifted to a reduced amplitude.

In the periphery, a global timestamp generated by an 8-bit counter driven by an external 2.5 MHz timestamp clock is assigned at the leading edge of the hit. At the same time the ToT is measured by a 12-bit counter driven by an external 200 MHz clock. The readout via SPI is only triggered, if there is data to be read out i.e. an open-drain signal connected to all the chips on one bus is pulled low, to keep the active duty-cycle of the SPI interface low.

A new version AstroPix4 is currently in submission, which removes the or'd readout and implements a per-pixel readout, while at the same time reducing the power consumption by replacing the fast counter-based ToT measurement by a Flash TDC based method, resulting in a very low power consumption given the low duty cycle of 10-5 and an improved time resolution of 3.125 ns for timing and ToT. The integration of a PLL reduces the number of connections to the DAQ to one 2.5 MHz reference clock and the SPI lines.

The design and first measurements of AstroPix3 as well as the development of AstroPix4 will be presented.

## Tuesday posters session / 179

# Development and performance of a pixel chip for the readout of GEM detectors for high-rate particle tracking

**Author:** Hulin Wang<sup>None</sup>

**Co-authors:** Jun Liu<sup>1</sup>; Zhen Wang; chaosong gao

<sup>1</sup> *Central China Normal University CCNU (CN)*

**Corresponding Author:** hulin.wang@ccnu.edu.cn

In this talk we report the R&D program underway at CCNU to develop a pixel chip for the readout of GEM detectors appropriate for use in the CSR external-target experiment (CEE) at HIRFL for beam monitoring. The chip offers simultaneous Time over Threshold (ToT) and Time of Arrival (ToA) measurements, with an event-driven readout mode. The chips were tested with injected pulses and a Fe-ion beam of 350 MeV/u, coupled with single GEM. The position resolution, rate capability and reconstruction efficiency for the beam particles were characterized.

### Summary (500 words):

Topmetal-CEEv1 is a front-end chip fabricated in GSMC 130 nm CMOS process for the readout of GEM detectors. This prototype features a column of 180 pixels and the peripheral circuitry in a  $19 \text{ mm} \times 4.2 \text{ mm}$  die. Each pixel occupies an area of  $100 \mu\text{m} \times 1.013 \text{ mm}$ , consisting of purely the top metal layer as the charge collecting anode. The charge-sensitive preamplifier (CSA), discriminator, Time over Threshold (ToT) and Time of Arrival (ToA) functionalities of each pixel, as well as the digital readout circuits are all implemented on the periphery.

Injected pulses were used to evaluate the key characteristics of the chip, including the noise, threshold and gain of the CSA and the ToT output. For medium gain setting and a charge threshold of  $10\text{k } e^-$ , the temporal noise and the fixed-pattern noise are around  $350 e^-$  and  $3000 e^-$ , respectively. The threshold

equalization via the in-pixel DAC could reduce the fixed-pattern noise by more than 80%. The measured gains of the CSA are consistent with the simulation values for medium and low gain settings, which have the feedback capacitance of 20 and 100 fF, respectively.

The Fe-ion beam of 350 MeV/u at HIRFL-CSR was used to characterize the response of the Topmetal-CEEv1 chips. Four chips were arranged in three columns in the bonding board, placed under single GEM and acting as the anode of a 6 cm × 5 cm × 5 cm field cage. The beam density varied between about 10<sup>4</sup> pps and 10<sup>6</sup> pps. Scans of the GEM voltages and pixel thresholds were performed. At the time of the beam test, the readout system was not fully developed. As a result, only binary readout and coarse ToA measurement with the accuracy of 25 ns were used. With binary readout, the position resolution of the beam particle for one column of pixels varied between about 70 to 150 μm, depending on the GEM voltage and pixel threshold. The cluster reconstruction efficiency as a function of the requirement on the number of pixels were evaluated. The rate capability up to 10<sup>6</sup> pps was demonstrated.

More results are foreseen by the time of the conference, including the position resolution with ToT measurements, and the test results using minimum ionization particles with triple GEM.

#### Thursday posters session / 180

## A common readout unit for multichannel array detectors at HIRFL-CSR

**Authors:** Xianqin Li<sup>1</sup>; haibo yang<sup>None</sup>; Chengxin Zhao<sup>2</sup>

<sup>1</sup> *Institute of modern physics, Chinese Academy of Sciences*

<sup>2</sup> *Institute of Modern Physics, CAS*

**Corresponding Author:** [lixianqin@impcas.ac.cn](mailto:lixianqin@impcas.ac.cn)

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science, and relative applications. A Common Readout Unit (CRU) has been designed for HIRFL-CSR to reduce the development time, production cost, and maintenance difficulties of the data transmission at HIRFL. With the Xilinx the Virtex 7 as its main FPGA, the CRU has 32 high-speed fiber optic interfaces to receive the data and two 10 Gigabit Ethernet links to transmit the data out. This paper will discuss the design and performance of the CRU.

#### Summary (500 words):

##### 1.Introduction

The Cooling Storage Ring of the Heavy Ion Research Facility in Lanzhou (HIRFL-CSR) is constructed to study nuclear physics, atomic physics, interdisciplinary science, and related applications. The major experiments on the HIRFL-CSR are the Internal Target Facility (ITF), the External Target Facility (ETF) and the External-target Experiment (CEE). With the rapid development of experiments in recent years, high-performance detector readout electronics is essential for the upgrade of the detectors. Hence, the CRU has 32 high-speed fiber optic interfaces to receive the data from the front-end electronics and two 10 Gigabit Ethernet links to transmit the data to the Data Acquisition System. In addition, the CRU also has a 1 Gigabit Ethernet interface, DDR3, and peripheral circuit design to complete the data transmission system. This paper will discuss the design and performance of the CRU.

##### 2.The desgin of CRU

The CRU is composed of several functional modules: system clock and trigger interface, optical fiber array interface, gigabit Ethernet interface, 10 gigabit Ethernet interface, DDR3 interface, field programmable gate array (FPGA) (Xilinx virtex-7-485T) and its peripheral circuits. Through the system clock and trigger interface, the FPGA of CRU and detector system work at the same frequency and phase, and the CRU can receive the trigger signal from the detector trigger system. It can receive data collected from up to 32 FECs and transmit it to the CRU through a high-speed fiber array interface. The high-performance Xilinx virtex-7-485T (FFG1158) FPGA and DDR3 cache module with 75K Configurable Logic Blocks (CLBs) can complete the implementation of data processing algorithms and the reorganization of all channel data packets for the entire event. The 10 Gigabit Ethernet interface based on TCP/IP can transmit data

to the data computer at high speed and stability. At the same time, control instructions and status feedback can be carried out on RCUs through Gigabit Ethernet.

### 3. Performance

To evaluate the functionality and performance of the CRU, we conducted a series of laboratory tests, including long-term stability hardware testing, communication link transmission performance testing, and joint testing with the Gamma detector system. Firstly, for electronic systems using fiber optic interfaces, long-term testing of eye charts and bit error rates can indicate hardware stability. The electric eye diagram has a large opening and clear outline, with an error rate of less than  $2E-15$ . In order to verify the integrity of the communication link and the correctness of data communication within the FPGA, a FEC that can collect periodic sine signals has been added to the input. The collected data is transmitted to the data computer through fiber optic communication, DDR3, and 10 Gigabit Ethernet, and the collected data matches the input signal data. Finally, a CSI detector array unit was added and the detector system was tested using a  $^{60}\text{Co}$  radiation source. The test results clearly separated the full energy peaks of 1.17 and 1.33 MeV.

## Optoelectronics and Electrical Data Links / 181

# Compact Silicon Photonic Mach-Zehnder Modulators for High-Energy Physics

**Author:** Simone Cammarata<sup>1</sup>

**Co-authors:** Fabrizio Di Pasquale<sup>2</sup>; Fabrizio Palla<sup>1</sup>; Philippe Velha<sup>3</sup>; Sergio Saponara<sup>4</sup>; Stefano Faralli<sup>2</sup>

<sup>1</sup> *Universita & INFN Pisa (IT)*

<sup>2</sup> *Istituto di Intelligenza Meccanica - Scuola Superiore Sant'Anna*

<sup>3</sup> *Dipartimento di Ingegneria e Scienza dell'Informazione - Università di Trento*

<sup>4</sup> *Università di Pisa*

**Corresponding Author:** simone.cammarata@cern.ch

The characterization of compact non-traveling-wave Mach-Zehnder modulators (NTW-MZMs) for optical readout in high-energy physics experiments will be presented to provide power-efficient alternatives to conventional traveling-wave devices and a more resilient operation compared to ring modulators. Electro-optical small-signal and large-signal measurements will be reported to show the performances of a custom NTW-MZM designed and fabricated in iSiPP50G IMEC's technology in the framework of INFN's FALAPHEL project. Bit-error-rate results will demonstrate its potential suitability for data links up to 25 Gb/s when being driven by voltage levels compatible with integrated CMOS drivers.

### Summary (500 words):

Novel radiation-tolerant optical links are required to handle the foreseen growth of data volumes and radiation intensities in the innermost regions of future detectors (e.g., HL-LHC, FCC, etc.). Limitations in the radiation hardness of current readout optoelectronic modules (e.g., lpGBT) have led to research activities regarding the suitability for using silicon photonics (SiPh) in high energy physics (HEP) experiments. Recent works have already reported SiPh active devices (e.g., high-speed depletion-driven PN-junction phase shifters, photodetectors, etc.) with reasonable radiation-tolerant behavior with the application of proper design hardening techniques or annealing procedures [1,2]. Although being still under deeper evaluation, this promising radiation resistance is now driving the development of fully-integrated SiPh-based transceivers (TRXs) to provide next-generation HEP readout systems [3].

In this context, the selection of electro-optical modulating devices becomes critical in addressing system-level requirements. Standard foundry-process SiPh technologies typically allow to implement free-carrier-based Mach-Zehnder (MZMs) or ring modulators (RMs). While RMs offer compact sizes, low-power high-speed operation and straightforward wavelength division multiplexing (WDM), their resonance is highly sensitive to temperature and process fluctuations, and they often need power-intensive

wavelength-locking mechanisms. On the other hand, MZMs are optically broadband and do not typically require strict stabilization against environmental changes. Nonetheless, they are often characterized by large footprints which impose careful radio-frequency (RF) traveling-wave (TW) design to efficiently apply modulation to optical waves. This translates in the need for on-chip RF termination resistors where both static and dynamic power dissipation take place and make TW-MZMs less power-efficient than RMs.

To provide a more compact and low-power interferometric modulator version to be used in HEP TRXs, we will report in this work the experimental characterization of a non-TW-MZM fabricated in iSiPP50G IMEC's technology within INFN's project FALAPHEL. Millimeter-scale phase shifters which usually compose TW-MZMs have been laid out in a meandered pattern to decrease the footprint but still retain a reasonable modulation depth. A 1.5 mm-long active phase shifting length has indeed been folded in a  $\sim 500\mu\text{m} \times 500\mu\text{m}$  area considering all required bond-pads. To give a fair comparison, RM designs typically end up with  $\sim 400\mu\text{m} \times 150\mu\text{m}$  footprint (including thermal heater contacts), while TW modulators more than  $\sim 500\mu\text{m} \times 2\text{mm}$ .

The active optical length in a non-TW-MZM design is thus decoupled from the effective RF length, allowing to shift the onset of TW effects to higher RF frequencies. Probing the proposed MZM in a 50  $\Omega$  testing environment results in  $\sim 6.5$  to  $\sim 8.5$  GHz -3dB electro-optical bandwidth depending on bias voltage.

Non-return-to-zero (NRZ) transmission experiments have been conducted recording eye diagrams and bit-error-rate (BER) versus optical power at the photo-receiver. The latter measurements have been taken with a (quasi-)CMOS compatible voltage swing of 1.4 V showing that BER levels below the soft-decision forward error correction (FEC) threshold are still achievable till 25 Gb/s. Instead, almost error-free transmissions have been captured till 35 Gb/s with 4.5 V peak-to-peak driving.

#### References

- [1] M. Lalović et al., doi: 10.1109/TNS.2022.3148579
- [2] M. Lalović et al., doi: 10.1088/1748-0221/18/03/C03028
- [3] T. Prousalidi et al., doi: 10.1088/1748-0221/17/05/C05004

#### Thursday posters session / 182

## Radiation Tolerance of the MUX64 for the High Granularity Timing Detector of ATLAS

**Authors:** Chuanye Wang<sup>1</sup>; Jie Zhang<sup>2</sup>; Jingbo Ye<sup>3</sup>; Lei Zhang<sup>4</sup>; Li Zhang<sup>5</sup>; Qiyu Sha<sup>6</sup>; Tiankuan Liu<sup>7</sup>; Xing Huang<sup>5</sup>; Yimin Che<sup>1</sup>; Zhenwu Ge<sup>1</sup>; Zhijun Liang<sup>6</sup>; Zifeng Xu<sup>1</sup>; Ming Qi<sup>4</sup>; Suen Hou<sup>8</sup>

<sup>1</sup> Nanjing University (CN)

<sup>2</sup> Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)

<sup>3</sup> Southern Methodist University, Department of Physics

<sup>4</sup> Nanjing University

<sup>5</sup> Southern Methodist University

<sup>6</sup> Chinese Academy of Sciences (CN)

<sup>7</sup> Brookhaven National Laboratory (US)

<sup>8</sup> Academia Sinica (TW)

**Corresponding Author:** chuanye.wang@cern.ch

The MUX64 ASIC is a 64-to-1 analog multiplexer developed to expand the ADC input channels in the peripheral electronics of HGTD for the ATLAS Phase-II upgrade. The MUX64 chips will be used in the radiation field of high-luminosity pp collisions at LHC to an integrated luminosity of 4000 fb<sup>-1</sup>. The radiation hardness of MUX64 have been tested with 80 MeV protons and X-ray exposures for damages caused by NIEL and TID, respectively. The irradiated samples have shown tolerance to withstand the NIEL to a fluence of  $3.21 \times 10^{15}$  (Si 1 MeV neq/cm<sup>2</sup>), and the TID of 0.746 MGy (Si).

**Summary (500 words):**

The High Granularity Timing Detector (HGTD) is developed for the ATLAS Phase-II upgrade to resolve high-luminosity event pileups. The detector modules are made with Low Gain Avalanche Detectors (LGAD) sensors which will be operated at  $-20\text{ }^{\circ}\text{C}$ . The detector operation requires monitoring on temperatures of the sensors and voltage drops of biases connected by flexible cables. The monitoring signals in analog format are read by the ADC channels of the lpGBT on the Peripheral Electronics Board (PEB). To accommodate the large number of monitoring channels, a 64-to-1 multiplexer (MUX64) is design to reduce input channels to the lpGBT ADC. The MUX64 accommodates 64 analog inputs to one analog output. One of the inputs is selected by a 6-bit decoder for connection to an lpGBT ADC channel. The dynamic range of the input signal to MUX64 ranges from 0 to 1.0V, and the on-resistance (RON) between the selected input channel and the output must be less than  $900\ \Omega$  to achieve the required resolution. The HGTD detector vessels are located in the endcap regions of the ATLAS at a distance of 3.5 m from the interaction point. The MUX64's on the PEB's are distributed around 0.8 m from the beam pipe center. The radiation tolerance is required for operation in the high-luminosity operation of LHC with the integrated luminosity of up to  $4000\ \text{fb}^{-1}$ . The PEB's will be exposed to Non-Ionizing Energy Loss of  $2.50 \times 10^{15}$  (1 MeV  $n_{\text{eq}}/\text{cm}^2$ , and the Total Ionizing Dose of 0.497 MGy. The radiation hardness of MUX64 were tested with the on-resistance of all 64 inputs examined in the nominal operation condition. The NIEL test has been conducted with 80 MeV protons at the Associated Proton Experiment Platform (APEP) of the China Spallation Neutron Source (CSNS). Two open-cavity chips were irradiated to a fluence of  $3.21 \times 10^{15}$  (Si 1 MeV  $n_{\text{eq}}/\text{cm}^2$ . The on-resistances responded to input signals ranging from 0.05-1.2 V were examined for deviation. On-resistance of one of the MUX64 chip had increased up to  $14\ \Omega$ , and the other up to  $25\ \Omega$ . The NIEL test shows MUX64 chips satisfy the requirement of HGTD. The TID tests were conducted in an X-ray facility equipped with a MultiRad160 X-ray machine. The test samples included an open-cavity chip and a QFN88 packaged chip, which were irradiated to 0.746 MGy (Si) at a dose rate of 5.98 Gy/s (Si). After the irradiation these chips were kept for annealing, in room-temperature for 24-hour, and were later heated at  $100\text{ }^{\circ}\text{C}$  for 168 hours. The on-resistance of the 64 input channels of each MUX64 were also measured with input voltages range from 0.05 to 1.2 V. Both MUX64s have shown negligible deviation in response to TID. The radiation hardness of MUX64 can fulfill the requirement for HGTD.

**Thursday posters session / 184****Beam test of a baseline vertex detector for the CEPC**

**Authors:** Shuqi Li<sup>1</sup>; Tianya Wu<sup>2</sup>; Xinhui Huang<sup>1</sup>

**Co-authors:** Hao Zeng<sup>1</sup>; Hongyu Zhang; JIA WANG; Jia Zhou<sup>1</sup>; Jianing Dong; Jinyu Fu<sup>1</sup>; Joao Barreiro Guimaraes Da Costa<sup>2</sup>; Jun Hu<sup>1</sup>; Ming Qi<sup>3</sup>; Mingyi Dong; Raimon Casanova Mohr<sup>4</sup>; Sebastian Grinstein<sup>4</sup>; Wei Wang<sup>1</sup>; Wei Wei; Weiguo Lu<sup>2</sup>; Xiaomin WEI; Xiaoting Li; Xiaoxu Zhang<sup>3</sup>; ZHANG Ying zhangying83; Zhijun Liang<sup>1</sup>; Ziyue Yan<sup>1</sup>

<sup>1</sup> IHEP

<sup>2</sup> Chinese Academy of Sciences (CN)

<sup>3</sup> Nanjing University

<sup>4</sup> IFAE - Barcelona (ES)

**Corresponding Author:** wuty@ihep.ac.cn

The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of pixel size and material budget. A Monolithic Active Pixel Sensor (MAPS) prototype, TaichuPix, based on a column drain readout architecture, has been implemented to achieve high spatial resolution and fast readout. A 6-layer telescope made by TaichuPix-3 chips and baseline vertex detector were tested at the DESY II TB21 beamline. This presentation proposes to show the architecture and beam test results of the baseline vertex detector prototype.

**Summary (500 words):**

The baseline vertex detector is proposed with a three-ladder architecture which will be double-sided with TaichuPix sensors. Thus, it can provide 6 precise reconstruction points. The key elements of the

baseline vertex detector are the pixel sensors, a test system made by TaichuPix-3 sensors was set up in DESY II TB21 in December 2022. Two detectors under test (DUT) were characterized, the analysis results indicate the spatial resolution is better than  $5\ \mu\text{m}$  and the detection efficiency is better than 98% under the set threshold. The experimental setup included 6 planes with the same test modules and one test module was configured as a DUT and the rest of the 5 test modules were set as a reference telescope. The distance between neighboring planes is 4 cm. The main beam energy used is 4 GeV, which is running at a data rate of 67.4 KB/s per plane to the system.

For the verification of the baseline vertex detector prototype, the double-sided structure is adopted to reduce the multiple scattering of particles and improve the impact parameter. That means the silicon pixel sensors and cables are installed on both sides of the support structure. Therefore, a ladder was made by common support together with two layers of silicon detectors. For this prototype, one side of a ladder is proposed to assemble 10 TaichuPix sensors on a flexible printed circuit board (PCB). Two flexible boards will be installed on the front and back sides of the lightweight carbon fiber support structure.

A preliminary baseline vertex detector was made by 2 TaichuPix-3 chips on each flexible PCB, and it was tested in DESY beamline in April 2023, which kept the main structure of the proposed design but fewer chips. The offline results of this prototype are under analysis and will be shown in the presentation.

**Thursday posters session / 185**

## **Implementation and performance comparison of MMC firmware on RISC-V and ARM-based MCUs**

**Author:** Aoqi Su<sup>None</sup>

**Corresponding Authors:** jie.z@cern.ch, suaq@ihep.ac.cn

The MicroTCA standard is widely used in the field of particle physics, and Advanced Mezzanine Card is the basic component of the MicroTCA system that requires module management control (MMC) for management. RISC-V is an open source ISA (Instruction Set Architecture) with extensive use. In this paper, we implement the MMC firmware on the MCU with RISC-V architecture. We build a universal standard library that is compatible with both the STM32F1XX and GD32VF1XX series MCU based on ARM and RISC-V architecture respectively. Interrupt response time is tested to compare real-time transaction processing performance of two popular processor architectures.

### **Summary (500 words):**

To manage and control the advanced mezzanine card (AMC) which is the basic component of the MicroTCA system, various MMC solutions have been developed. However, most of these solutions operate in polled mode and use MCUs (Micro Controller Units) based on x86 and ARM processor architectures. In our work, we have implemented an MMC solution based on the RISC-V architecture MCU. We used GigaDevice's GD32VF103 MCU chip and implemented all the necessary functions of MMC based on FreeRTOS. Our implementation shows that the real-time performance is better than the polling method. We build an universal standard library by referring to STM32 standard peripheral libraries. To verify its compatibility, we used the development platform VScode and PlatformIO to compile and download. The result show that the library is compatible with both the STM32F1XX series MCU and GD32VF1XX series MCU chips based on ARM and RISC-V architecture respectively.

To evaluate the real-time performance of the two chips, we downloaded the FreeRTOS-MMC firmware to both MCUs through the JLink tool and inserted the AMC based on these two chips into the MicroTCA chassis. We performed interrupt response time tests by inserting and unplugging the hot-swappable handle. They have different interrupt response performance.

We analyzed the reasons for this difference by comparing the processor of the ARM architecture (taking Cortex-M3 as an example) and the processor of the RISC-V architecture (taking Bumblebee as an example). The interrupt response mechanism of the two processors is very different. In the ARM Cortex-M processor, the work related to the interrupt response is all done by the hardware. In contrast, in the RISC-V Bumblebee processor, before the processor enters the interrupt service program, the context needs to be saved by the software first, and the complete interrupt response is done by the hardware and software. Additionally, after compiling the source program into assembly instructions, the number of instructions between them is also different, with RISC-V having more instructions than ARM, about 6%



## Module, PCB and Component Design / 186

## Real-time Signal Processing and Data Acquisition for the Electric Field Detector (EFD-02) on the CSES-02 satellite

**Authors:** Alexandra Parmentier<sup>1</sup>; Andrea Russi<sup>2</sup>; Cristian De Santis<sup>3</sup>; Davide Badoni<sup>4</sup>; Elio Alunno Camelia<sup>5</sup>; Emiliano Fiorenza<sup>2</sup>; Fabrizio De Angelis<sup>2</sup>; Fabrizio Nuccilli<sup>2</sup>; Glammaria Rebustini<sup>6</sup>; Giuseppe Masciantonio<sup>6</sup>; Igor Bertelli<sup>2</sup>; Nello Vertolli<sup>2</sup>; Piergiorgio Picozza<sup>7</sup>; Piero Cipollone<sup>6</sup>; Piero Diego<sup>2</sup>; Pietro Ubertini<sup>None</sup>; Roberta Sparvoli<sup>None</sup>; Roberto Ammendola<sup>8</sup>

<sup>1</sup> *Tor Vergata University of Rome*

<sup>2</sup> *INAF-IAPS*

<sup>3</sup> *Universita degli Studi di Roma Tor Vergata (IT)*

<sup>4</sup> *INFN Sezione di Roma Tor Vergata*

<sup>5</sup> *NEAT SRL*

<sup>6</sup> *INFN Roma Tor Vergata*

<sup>7</sup> *INFN and University of Rome Tor Vergata*

<sup>8</sup> *INFN e Universita Roma Tor Vergata (IT)*

**Corresponding Authors:** gianmariarebustini@gmail.com, rebustini@roma2.infn.it, roberto.ammendola@roma2.infn.it

The Electric Field Detector (EFD-02) on board of the second China Seismo-Electromagnetic Satellite (CSES-02) will measure the ionospheric electric field components at a Low Earth Orbit (LEO) over a wide frequency band (DC - 3.75 MHz) and with less than  $1 \mu\text{V}/\text{m}/\sqrt{\text{Hz}}$  sensitivity. EFD-02 will measure the voltage differences between pairs of probes installed at the tips of four booms deployed from the satellite. In this work we describe the digital hardware section based on a Zynq SoC device in charge of signal processing and data acquisition and we show the instrument overall performances.

### Summary (500 words):

The China Seismo-Electromagnetic Satellite (CSES) program is meant to monitor dynamic perturbations of top-side electromagnetic field, plasma and particles of the Earth's ionosphere to study their possible correlations with the occurrence of seismic events. Another major goal of the mission is the investigation of the interaction between the solar wind and magnetosphere-ionosphere system. The CSES-02 mission foresees the launch of a second satellite, scheduled by the end of 2023, with an expected lifetime of 6 years.

Aboard of CSES-02 there will be the Electric Field Detector (EFD), that measures the differences in electric potential (with respect to the spacecraft potential) between different pairs of probes mounted at the tips of 4 booms deployed at 4.5 m from the satellite. Electric field components are obtained as the difference between two probes voltages divided by their relative distance (8.3 m on average).

Regarding the instrument specifications, EFD-02 band range will cover from DC to 3.5 MHz, with a typical resolution  $\leq 1 \mu\text{V}/\text{m}$  (DC-16 Hz). Signal acquisition is realized in five bands defined as follows: ULF band in the range from 0 to 100 Hz, with dynamic range of 144 dB; ELF band up to 2 kHz with a dynamic range of 120 dB; VLF band up to 30 kHz with a dynamic range of 96 dB; VLFe up to 100 kHz with a dynamic range of 96 dB; HF in the range of 21 kHz to 3.75 MHz with a dynamic range of 72 dB. There are 4 different ULF channels, each one deriving from the 4 probes, while there are 3 channels for ELF, VLF, VLFe and HF bands, deriving from 3 analog signal differences between programmable pairs of the 4 probes. The measured sensitivity of the instrument is less than  $0.1 \mu\text{V}/\text{m}/\sqrt{\text{Hz}}$ .

The instrument is composed of several parts, such as the Electric Field Probes, that are 4 identical sensors housing a spherical shell placed at the end of the satellite boom; the Low Voltage Power Supply and Control, that manages power supply, housekeeping and TM/TC interface towards the satellite; the Splitter, that controls the switching of signals and power supply lines of the probes between the hot and cold electronics; the Analog Processing Unit, that makes the analog-to-digital conversion and pre-filtering of the signals; the Digital Processing Unit (DPU) that performs digital processing and data handling. The architecture of the DPU will be described, in particular the Programmable Logic part implemented in a Zynq SoC device, that is in charge of signal filtering, frequency band division, Fourier transform, statistical functions calculation and, finally, data scheduling and formatting according to the 82 Gbit/day

payload requirement.

Regarding the statistical functions, we perform real-time calculation of average, standard deviation and kurtosis of spectral data on VLF, VLFe and HF bands with a streaming pipelined architecture, implemented both in fixed point and in floating point arithmetics. The results and comparison of these two implementations will be shown.

**Thursday posters session / 187**

## Commissioning of the Upstream Tracker for the LHCb upgrade

**Author:** Carlos Abellan Beteta<sup>1</sup>

<sup>1</sup> *University of Zurich (CH)*

**Corresponding Author:** carlos.abellan.beteta@cern.ch

This contribution presents the latest advancements in integrating the Upstream Tracker in LHCb, including deploying control software, data acquisition firmware, decoding algorithm, and data analysis software. Additionally, the progress of different tasks is detailed, along with plans for the immediate future. The main focus of this talk is on the assessment of detector performance, including environmental conditions, electronics performance at the nominal operating temperature, and efficiency and noise hits at the nominal detector operation conditions. Various quality-control tests and component performance verification is described, as data captured with the dedicated firmware, showing the steps of the detector integration in LHCb.

### Summary (500 words):

The LHCb experiment, a forward spectrometer located at the Large Hadron Collider, is focused on the study of decays involving beauty and charm hadrons.

During the second run of data taking, the experiment generated extensive data in flavour physics as well as other physics areas that make use of the LHCb experiment's forward acceptance.

A significant upgrade of the LHCb detector has been recently installed and is being commissioned. The upgraded detector can handle higher luminosity and has a flexible software trigger requiring all detector components to release their information at 40 MHz.

The upgrade included the Upstream Tracker: a detector comprising four planes of silicon microstrip detectors mounted on staves, located upstream of LHCb's bending magnet.

This critical component of the LHCb detector, essential for the software trigger, has recently been installed and is currently undergoing the commissioning phase with the goal of a careful but swift integration in the global data taking framework.

The installation process involved several quality control tests to ensure proper functionality, but the operation underground pose new challenges and each aspect of the detector performance need to be properly validated. For example, some aspects of the grounding are naturally different, and this is the first time that the two detector halves are brought together, with a new beam pipe seal. The commissioning process verifies performance and tunes all possible parameters to improve the situation if it is not the case.

Another important current goal is integrating the Upstream Tracker with the rest of LHCb; this includes a myriad of tasks like: deploying a control software, a data acquisition firmware, a decoding algorithm to be run in GPUs, data analysis software and many others.

This contribution presents the progress achieved in these tasks. It begins by summarizing the various components of the detector and explaining the steps to be undertaken to ensure its integration in the experiment. The contribution concludes by presenting the first available data that captured with the Upstream Tracker, with a preliminary assessment of its performance.

**Thursday posters session / 190**

## Evaluating the RFSoc as a Software-Defined Radio Readout System for Magnetic Microcalorimeters

**Authors:** Luis Ardila<sup>1</sup>; Timo Muscheid<sup>None</sup>

<sup>1</sup> *KIT-IPE*

**Corresponding Authors:** robert.gartmann@kit.edu, luis.ardila@kit.edu

Arrays of superconducting sensors enable particle spectrum analysis with superior energy resolution. To efficiently acquire data from these sensors, the readout electronics operating at room temperature must perform multiple tasks, such as real-time frequency demodulation. We designed a Software-Defined Radio (SDR) system composed of an MPSoC board, an analog-to-digital conversion stage, and a radio frequency front-end mixing stage to meet the system requirements. Nevertheless, utilizing an Radio Frequency System-on-Chip (RFSoc) could simplify the overall system by integrating the conversion stage and potentially eliminating the mixing stage. This work investigates the applicability of RFSocs for the aforementioned use case.

### Summary (500 words):

The development of high-precision superconducting particle detectors, such as Magnetic Microcalorimeters (MMC) operating at temperatures of a few millikelvins, enables the investigation of fine details in particle interactions. With their inherent high energy resolution, broad energy range, and excellent quantum efficiency, these detectors are ideally suited for precise measurements. To increase the spatial detection area or the number of measurements per time unit, arrays of tens of thousands of these detectors can be operated in parallel. Using a Microwave SQUID Multiplexer (uMUX), multiple sensors can be read out via frequency multiplexing utilizing a single common transmission line. This reduces the number of thermal bridges in the cryogenic environment but increases the complexity of the readout electronics at room temperature, as both the generation and acquisition of a frequency comb at several GHz are required.

A Software-Defined Radio (SDR) has been developed to perform signal generation, demodulation of the frequency comb, and recovery of the raw sensor signals. This SDR comprises a heterogeneous MPSoC platform connected to a conversion stage equipped with several high-speed DACs and ADCs. The converters are in turn connected to another board, designed for mixing the analog signal from baseband to microwave frequencies and vice versa, to meet the requirements of the uMUX. The first application for our SDR system will be at the ECHO-100k experiment, which investigates the electron neutrino mass by detecting the decay spectrum of Ho-163 with more than 10,000 MMCs over a three-year period. Currently, the room-temperature SDR readout electronics system is based on custom hardware. However, Radio Frequency System-on-Chips (RFSocs) from AMD Xilinx offer a new possibility for accelerating and simplifying SDR systems for future experiments. In addition to the processing system and the programmable logic, these devices also contain tightly coupled high-speed DACs and ADCs for the transmission and acquisition of analog signals, respectively. The third generation of these RFSocs provides sufficient converters to be comparable to the system we have developed for the ECHO experiment. In this work, we evaluate the feasibility of using such an RFSoc device in an SDR system for the readout of superconducting particle detectors. We ported our firmware from a conventional MPSoC to the RFSoc and operated the system on a ZCU216 evaluation board. For the RFSoc to operate comparably to our system, several modifications in the FPGA modules and drivers were necessary due to the differing clock tree structure and converter interfaces on the two platforms.

Through the characterization of both our custom hardware and the ZCU216 under the same conditions, a comparison of the signal quality and measurement accuracy was carried out. The tests were performed within the context of the ECHO experiment, considering the specific requirements of the experiment for the preparation of the measurement setup. The results of our analysis are presented here, as is an assessment of whether the RFSoc can be used for potential extensions of the ECHO experiment or for the readout of frequency-multiplexed superconducting particle detectors in general.

Thursday posters session / 191

## A novel Front-End for Monolithic Active Pixel Detectors ASICs

**Author:** Ana Dorda<sup>1</sup>

**Co-authors:** Michael Campbell<sup>2</sup>; Rafael Ballabriga Sune<sup>2</sup>

<sup>1</sup> *KIT - Karlsruhe Institute of Technology (DE)*

<sup>2</sup> *CERN*

**Corresponding Author:** ana.dorda.martin@cern.ch

In this work, a low-power low-noise readout circuit for monolithic pixel detectors is presented. The design focuses on robustness and scalability for both reticle sized chips and stitched designs. The front-end includes a differential charge sensitive amplifier, a reset network and a two-stage discriminator. Threshold trimming is performed with a 3-bit DAC. The feedback capacitance is kept at 0.3 fF to boost the gain for low input charges. The gain is 0.4 mV/e<sup>-</sup>, the noise is 19 e<sup>-</sup> r.m.s. and the threshold dispersion after equalization is 68 e<sup>-</sup> r.m.s. Simulations at schematic level and post-layout extraction are presented.

**Summary (500 words):**

The EP R&D Work Package 1.2 aims to develop monolithic CMOS pixel sensors using the TPSCo 65 nm Image Sensor Process, with a small collection electrode. This process permits increased component density while reducing power consumption with respect to the previous node used by the High Energy Physics community (the 180nm node). Several possible applications of this process (e.g., ALICE inner tracker) impose strict constraints regarding power consumption to ensure the scalability to wafer level dimensions in stitched CMOS sensors. This requires the design to be robust for voltage drop and power supply variations. The low noise for the front end is another constraint in order to amplify the signal deposited in the small depletion region of the sensor.

This front-end includes a Charge Sensitive Amplifier (CSA). The CSA is based on a differential folded cascode amplifier (nominal gain of 50 dB), which allows for external baseline adjustment (nominal baseline at 300 mV). An nMOS transistor in weak inversion provides the feedback to discharge the feedback capacitance. This transistor is biased via a replica circuit, which keeps the baseline stable in case of temperature variations. The discriminator comprises a two-stage CMOS OTA that ensures speed and a high gain (nominal 55 dB). A 3-bit DAC is included to compensate for the pixel-to-pixel threshold variation.

These types of front-ends have two-time constants. The rise time constant depends on the transconductance of the input transistor, the feedback capacitance and the sum of the input, output, and feedback capacitance. The feedback capacitance, when the pulse is above ~25mV, is discharged with a constant current, which leads to a linear time over threshold measurement. One of the particularities of this process is the small input capacitance of the sensor (~ 1 fF). The strict requirement for lower consumption (10 nA CSA biasing current) reduces the transconductance of the input transistor, affecting the rise time. To keep the low power consumption and the benefits of the small input capacitance, the feedback capacitance has a nominal value of 0.36 fF. This allows for amplification of small input charges, working on a range from 100 e<sup>-</sup> to 2000 e<sup>-</sup> with a gain of 0.4 mV/e<sup>-</sup>, fast rise time (~ 1 us) and low noise (19 e<sup>-</sup> r.m.s). Schematic simulations prove a linear ToT up to 1750 e<sup>-</sup> and a systematic ToA dispersion of 800 ns. The 3-bit DAC for threshold equalization reduces the minimum detectable charge from ~165 e<sup>-</sup> to ~68 e<sup>-</sup>. Corner simulations confirm the robustness of this amplifier against bias and temperature variations.

Simulations of this design demonstrate how this type of front-end, based on a transconductance amplifier, can be used in applications that require a low power consumption and where the focus is on detecting and amplifying Minimum Ionizing Particle (MIP) signals.

ASIC / 192

## First test results for ECON-T and ECON-D ASICs for CMS HG-CAL

**Author:** Jim Hirschauer<sup>1</sup>

**Co-authors:** Alpana Shenai<sup>1</sup>; Chinar Syal<sup>1</sup>; Cristina Ana Mantilla Suarez<sup>1</sup>; Cristinel Veniamin Gingu<sup>2</sup>; Danny Noonan<sup>1</sup>; Datao Gong<sup>1</sup>; Davide Braga<sup>3</sup>; Di Guo<sup>4</sup>; Duje Coko<sup>5</sup>; Feas Bram<sup>6</sup>; Iraklis Kremastiotis<sup>7</sup>; James Hoff<sup>1</sup>; Jeffrey Prinzie<sup>8</sup>; Jingbo Ye<sup>9</sup>; Jon Wilson<sup>10</sup>; Matteo Lupi<sup>7</sup>; Mike Hammer<sup>11</sup>; Paul Leroux<sup>6</sup>; Paul Michael Rubinov<sup>1</sup>; Paulo Rodrigues Simoes Moreira<sup>7</sup>; Pedro Vicente Leitao<sup>7</sup>; Quan Sun<sup>12</sup>; Ralph Owen Wickwire<sup>13</sup>; Rui De Oliveira<sup>7</sup>; Szymon Kulis<sup>7</sup>; Xiaoran Wang<sup>1</sup>; Yang Dongxu<sup>14</sup>

<sup>1</sup> *Fermi National Accelerator Lab. (US)*

<sup>2</sup> *Fermi National Accelerator laboratory*

<sup>3</sup> *FERMILAB*

<sup>4</sup> *Southern Methodist University (US)*

<sup>5</sup> *University of Split. Fac.of Elect. Eng., Mech. Eng. and Nav.Architect. (HR)*

<sup>6</sup> *Katholieke Universiteit Leuven*

<sup>7</sup> *CERN*

<sup>8</sup> *KU Leuven (BE)*

<sup>9</sup> *Southern Methodist University, Department of Physics*

<sup>10</sup> *Baylor University (US)*

<sup>11</sup> *Argonne National Laboratory*

<sup>12</sup> *Fermi National Accelerator Lab.*

<sup>13</sup> *Fermilab*

<sup>14</sup> *Southern Methodist University*

**Corresponding Author:** cristina.ana.mantilla.suarez@cern.ch

With over 6 million channels, the High Granularity Calorimeter for the CMS HL-LHC upgrade presents a unique data challenge. The ECON ASICs provide a critical stage of on-detector data compression and selection for the trigger path (ECON-T) and data acquisition path (ECON-D) of the HGCal. The ASICs, fabricated in 65nm CMOS, are radiation tolerant (200 Mrad) with low power consumption (<2.5 mW/channel). We report the first functionality and radiation tests for the ECON-D-P1 full-functionality prototype including a comparison of single event effect (SEE) cross sections measured for different methods of triple modular redundancy.

#### **Summary (500 words):**

The High Granularity Calorimeter (HGCal) for the CMS HL-LHC upgrade is a sampling calorimeter that will feature fine readout segmentation. Amplitude and arrival time of analog sensor signals are digitized by the HGCROC ASIC, which also provides 12.5 us of trigger buffering of the digitized data. The transmission of digital data to the back-end electronics is handled by the ECON ASICs for data selection, compression, and concentration, and the lpGBT ASIC for data serialization to 10.24 Gbps.

The ECON-D ASIC manages data flow for events passing the 750 kHz L1 trigger. ECON-D specifically performs (a) zero suppression of raw HGCROC data with user-configurable corrections for common-mode front-end noise and contamination from out-of-time pileup and (b) autonomous generation of a front-end “reset request” based on highly configurable algorithms for time analysis of front-end error conditions. The ECON-T ASIC manages data flow on the HGCal trigger path, which provides data to the L1 trigger at the full LHC 40 MHz bunch crossing frequency. ECON-T includes several user-selectable data compression algorithms, allowing the user to operate in modes with either fixed or variable latency and data format. In addition to traditional selection/compression algorithms, ECON-T features the first implementation of a radiation tolerant, low-power neural network (NN) for machine learning-based, on-detector data compression. Full reconfigurability of NN weights and biases allows reoptimization of the NN for changing detector and beam conditions.

Full functionality prototypes of both chips have been or are being produced: ECON-T-P1 was received in December 2021, and ECON-D-P1 will be received in June 2023. Both ASICs are produced in a 65nm CMOS process and designed to meet radiation tolerance requirements for SEE and TID (200 Mrad), low power consumption (less than 5 mW/channel for both ECON-D and ECON-T combined), and a programmable number of 1.28 Gbps inputs and outputs. The radiation hard IP blocks for the PLL, receivers, transmitters, and input phase alignment are taken from the lpGBT IP. SEE protection is achieved through

triple modular redundancy: ECON-T-P1 includes triplication sequential logic with a single-voter strategy. ECON-D-P1 implements triplication of sequential and combinatorial logic, resets, and clocks in most of the design.

In this report, we summarize full test results for the ECON-T-P1 including functionality and radiation (SEE and TID) performance. We present first results from ECON-D-P1 functionality and radiation testing, and we show a unique comparison of the level of SEE protection provided by the different methods of triple modular redundancy used in the two ASICs.

**Thursday posters session / 193**

## **Development of quad-channel high resolution digital picoammeter for beam diagnostics**

**Author:** Mauricio Donatti<sup>1</sup>

**Co-authors:** Fernando Henrique Cardoso ; Lucas Yugo Tanio <sup>1</sup>

<sup>1</sup> LNLS

**Corresponding Author:** mauricio.donatti@lnls.br

In particle physics applications the photon beam interaction with various materials can produce electric charge which can be measured as current and be used to diagnose particle trajectories, beam intensity, beam profile, position, and stability. SIRIUS, the new 3 GeV fourth-generation Brazilian light source, will make use of hundreds of low-intensity measurement instruments. This work aims at showing up and discussing the design details, challenges and test results of a four-channel high-performance digital ammeter, applied for general-purpose beam diagnostics.

### **Summary (500 words):**

High accuracy and high resolution low current measurements are a common demand for many beam-lines attached to SIRIUS, the new 3GeV fourth-generation Brazilian light source. Due to femtoampere resolution measurements technical requirements and the need for a large number of diagnostic elements such as photodiodes, ionization chambers, and photon beam position monitors, we have developed a four-channel digital general-purpose current meter. The device is based on low-noise and extremely low input bias bipolar transimpedance amplifiers with eight selectable ranges (full scales from pA to mA).

This wide dynamic range is implemented by using the classical multirange transimpedance amplifier circuit, which makes use of high insulation reed relays to select different high-precision gain resistors on the amplifier stage. The circuit is followed by floating 2ksps, 24-bit Delta-Sigma analog-to-digital converters. The range selection, ADCs configuration, and digital data acquisition are managed by an ARM microcontroller. The data stream is sent through a 100 Mbps Ethernet link and can be synchronized by means of external triggering input and outputs. The electronics is prepared to bias the connected device up to 400 V using an external HV power supply.

This work aims at discussing the theory of very low current measurements focusing on explaining the several sources of errors that can impact the electronics performance. The component selection process and the adopted strategies to make a proper guarding, shielding, and PCB layout in such a way to effectively reduce static and dynamic errors are also presented.

The PCB was designed to guarantee extremely low leakage on the current path from the input connector to the transimpedance amplifier input pin employing guard ring tracks, planes, and metallic shielding driven by a guard buffer circuit, combined with PCB cut-outs and solder mask removal from sensitive region. Even using several low-current leakage techniques, a careful cleaning process was developed to improve the circuit's accuracy.

The characterization results show that the achieved gain, temperature stability, accuracy, and noise performance are on the same order of magnitude as those of expensive commercial benchtop equipment.

In low bandwidth applications the device was able to measure hundreds of picoampere with intrinsic noise of units of femtoampere (RMS). For many particle physics applications, the designed device could be an excellent low-cost multichannel choice.

Trigger and Timing Distribution / 194

## Testing a Neural Network for Anomaly Detection in the CMS Global Trigger test crate during Run 3

**Authors:** Jennifer Ngadiuba<sup>1</sup>; Sioni Paris Summers<sup>2</sup>; Thea Aarrestad<sup>3</sup>

<sup>1</sup> *FNAL*

<sup>2</sup> *CERN*

<sup>3</sup> *ETH Zurich (CH)*

**Corresponding Author:** noah.zipper@colorado.edu

We present the deployment and testing of an autoencoder trained for unbiased detection of new physics signatures in the CMS Global Trigger test crate during LHC Run 3. The GT test crate is a copy of the main GT system, receiving the same input data, but whose output is not used to trigger the readout of CMS, providing a platform for thorough testing of new trigger algorithms on live data, but without interrupting data taking. We describe the integration of the DNN into the GT test crate, and the monitoring, testing, and validation of the algorithm during proton collisions.

### Summary (500 words):

In the CMS Level-1 hardware trigger, the Global Trigger ( $\mu$ GT) component is responsible for selecting which collisions are recorded and which are discarded, based on the signals from the different sub-detectors.

The  $\mu$ GT comprises several custom MP7 processing boards equipped with Xilinx Virtex-7 FPGAs with high-speed 10 Gb/s optical connections. For Run 3, a test crate comprising the same hardware as the  $\mu$ GT has been added. Consisting of 7 MP7 boards with the same Virtex-7 FPGAs and high-speed optical fibers, the GT test crate is a copy of the main  $\mu$ GT system, receiving the same input data, but whose output is not used to trigger the readout of CMS. This provides a platform for thorough testing and validation of new trigger selection on live data, without interrupting data taking.

ML-based anomaly detection methods have been gaining popularity in particle physics as a way of extracting potential new physics signals in a model-agnostic way, by rephrasing the problem as an out-of-distribution detection task. One promising technique is self-supervised variational autoencoders, which have the added benefit of enabling algorithms to be trained on unlabeled data rather than simulations.

In this project, we present the deployment and testing of a variational autoencoder trained for unbiased detection of new physics signatures in the test crate of the CMS Global Trigger during LHC Run 3. The DNN is integrated into the  $\mu$ GT test crate using hls4ml, a software package that allows the conversion of machine learning models into hardware descriptions that can be implemented on FPGAs. This allows the DNN to be run in real-time, with low latency and high throughput, making it suitable for deployment in the  $\mu$ GT system.

We describe the monitoring, testing, and validation of the algorithm during proton collisions in 2023. From the  $\mu$ GT test crate trigger bit counters are read out and logged, enabling validation of the rate of the algorithm in data against the emulation of the algorithm on Zero Bias data. Through the central Prometheus monitoring database, the performance of the algorithm can be evaluated in real time.

Since the test crate is not able to trigger the readout of the CMS experiment, it is also possible to deploy trigger menus not intended for data taking but enabling full characterisation and probing of the behavior of an algorithm during LHC collisions. This includes, for example, applying different thresholds than the eventual online target, or using different NN trainings simultaneously.

The deployment and testing of this DNN in the GT test crate is a crucial step towards the development of new trigger algorithms for the CMS detector. By providing an unbiased platform for testing and validation, we can ensure that new algorithms are effective, while maintaining the efficiency and reliability of the overall  $\mu$ GT system.

**Module, PCB and Component Design / 195**

## Front End Board for Large Area SiPM Detector

**Authors:** Andrea Fabbri<sup>None</sup>; Carlo Venettacci<sup>None</sup>; Fabrizio Petrucci<sup>1</sup>; Salvatore Loffredo<sup>None</sup>; Stefano Maria Mari<sup>None</sup>

<sup>1</sup> INFN - Sezione Roma III

**Corresponding Authors:** carlo.venettacci@roma3.infn.it, andrea.fabbri@roma3.infn.it

Silicon photomultipliers (SiPMs) are widely used for several applications, such as High Energy Physics experiments, as well as other research and industrial fields. SiPMs working at low temperature, in particular, are the most interesting application for the newly large particle detectors for neutrinos and dark matter experiments. In this work we present a low-noise, high-speed front-end electronics (Front-End Boards, FEBs) for large area SiPMs to be used in the JUNO-TAO experiment. The FEBs are able to manage the signals coming from a 25 cm<sup>2</sup> tile, showing single photoelectron resolution better than 13% and dynamic range up to 250 p.e.

### Summary (500 words):

In the proposed work, a careful approach to the front-end electronics design has shown to be critical in order to fully keep the exceptional performances of the SiPMs in terms of single photon detection, dynamic range and fast timing properties. At the moment 100 preproduction batch is ready and tested with an ultra-low background construction material in order to be used in rare event searches. A complete test report about

the performance of the preproduction batch at room temperature and at -50° will be presented, showing the solution taken to ensure an high stability and reproducibility of the results.

The board dimensions is 5cm x 3cm, so it can be perfectly arranged behind a 5cm x 5cm SiPM tile. Different shapes were already tested showing the same performances.

The proposed Front End Board has two separate channels and it has been tested with many SiPM-based photodetector multi-pixel photon counter (MPPC) available on the market from different vendors, from temperatures down to -70° and up to +80°, showing excellent performances and a mean time between failure of  $9 \cdot 10^6$  hours, due to reduced component numbers and the accurate selection of the passive part number.

The nanosecond timing properties make them suitable to work with the typical mixtures of liquid scintillators currently used in particle and astroparticle physics experiments. FEB can read from few squared millimeter SiPM, ensuring a very high timing resolution, up to several squared centimeter by the use of passive gangling.

Moreover, by changing the shaping time and the gain factor by changing two resistor, the board can be coupled even with plastic scintillators where more photons are expected.

The JUNO-TAO experiment will need more than 8000 channels (by the use of 4000 FEB) to ensure the proposed energy resolution (<1.5% @ 1 MeV), spatial resolution (around 1 cm) and timing performances (around 1 ns).

**Tuesday posters session / 197**

## RD50-MPW: A monolithic High Voltage CMOS pixel chip with high granularity and high radiation tolerance



**Author:** Eva Vilella Figueras<sup>1</sup>

<sup>1</sup> *University of Liverpool (GB)*

**Corresponding Authors:** chenfan.zhang@cern.ch, vilella@hep.ph.liv.ac.uk, chenfan@hep.ph.liv.ac.uk

This contribution presents results from the RD50-MPW family of monolithic High Voltage CMOS (HV-CMOS) pixel chips, which are developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems. Parameters especially considered in this programme are radiation tolerance, time resolution and granularity. This contribution reviews the design of RD50-MPW3, and presents its laboratory and test beam results. It also presents the design details of the latest prototype, RD50-MPW4. The prototypes developed so far are in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry S.r.l.

#### **Summary (500 words):**

RD50-MPW3 has a 64 rows x 64 columns matrix of 62  $\mu\text{m}$  x 62  $\mu\text{m}$  pixels with both analogue and column drain digital readout electronics embedded inside the large collection electrode. The pixel electronics also include logic to mask noisy pixels and an 8-bit SRAM shift register for serial configuration. RD50-MPW3 implements a double column scheme, which together with the 8-bit SRAM shift register, alleviates the routing congestion and facilitates means to minimise the crosstalk. This prototype has an advanced digital periphery for effective pixel configuration and fast data transmission, which consists of one EOC circuit per double column and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. The event data generated by the pixels is packed into frames, zero suppressed and encoded following the 8b/10b Aurora protocol. It is serialised over a single 640 Mb/s LVDS line.

We have evaluated RD50-MPW3 in the laboratory and also with particle beams at CERN SPS and MedAustron in Vienna, Austria (see figure 1). Electrical tests in the laboratory confirmed the functionality of the pixels and digital periphery, however the noise level was found to be too high especially for those pixels that are near the digital periphery. This forced us to increase the threshold voltage to 300 mV above the baseline voltage, which limits the efficiency of the sensor. The main goals of the test beams were to integrate RD50-MPW3 and its DAQ (i.e. chip carrier board, CaR board and Xilinx ZC706 evaluation board) into a reference system while enabling synchronisation between the chip and the reference with an AIDA2020 Trigger Logic Unit (TLU), and evaluate the chip with a particle beam. The average efficiency of the sensor, measured to be 60%, is low due to the high threshold voltage (see figure 2). We will evaluate RD50-MPW3 with a particle beam at DESY in July 2023, before and after irradiation to high fluence. Masking noisy pixels is a potential solution being currently explored to reduce the threshold voltage, and therefore improve the average efficiency at the price of reducing the sensitive area.

RD50-MPW4 essentially implements solutions to achieve a much higher breakdown voltage ( $> 400$  V) and reduce the noise across the pixels of the matrix ( $< 50$  mV), while maintaining the high granularity of 62  $\mu\text{m}$  x 62  $\mu\text{m}$  pixels. Unlike its predecessors, RD50-MPW4 uses floating p-stop style pixel-to-pixel isolation and has an optimised multi-guard ring chip frame. RD50-MPW4 implements topside edge biasing, and we will add backside biasing as a post-processing step on a subset of the fabricated samples. Unlike RD50-MPW3, the pixel matrix and peripheral readout use separate power and ground domains in RD50-MPW4. We expect this will allow us to reduce the threshold voltage and therefore increase the average efficiency across the whole chip, as post-layout simulations have shown the noise is low and there are no fake events (see figure 3). Table 1 summarises the main design details and performance parameters of the RD50-MPW pixel chips.

**System Design, Description and Operation / 198**

## **From 3D to 5D tracking: SMX ASIC-based Double-Sided Micro-Strip detectors for comprehensive space, time, and energy measurements**

**Author:** Maksym Teklishyn<sup>None</sup>

**Co-authors:** Adrian Rodriguez ; Alberica Toia<sup>1</sup>; Christian Joachim Schmidt<sup>2</sup>; Dairon Rodriguez Garces ; Dario Alberto Ramirez Zaldivar ; Hans Rudolf Schmidt<sup>3</sup>; Joerg Lehnert<sup>4</sup>; Johann Heuser<sup>5</sup>; Kshitij Agarwal<sup>6</sup>; Lady Maryann Collazo Sánchez ; Marcel Bajdel ; Shaifali Mehta<sup>7</sup>; Uli Frankenfeld<sup>2</sup>

<sup>1</sup> *Goethe University Frankfurt (DE)*

<sup>2</sup> *GSI - Helmholtzzentrum für Schwerionenforschung GmbH (DE)*

<sup>3</sup> *Eberhard-Karls-Universität Tübingen (DE)*

<sup>4</sup> *GSI Darmstadt, Germany*

<sup>5</sup> *GSI*

<sup>6</sup> *Eberhard Karls Universität Tübingen (DE)*

<sup>7</sup> *University of Tübingen*

**Corresponding Author:** m.teklishyn@cern.ch

We present the recent development of a lightweight detector capable of accurate spatial, timing, and amplitude resolution of charged particles. The technology is based on double-sided double-metal p+n-n+ micro-strip silicon sensors, ultra-light long aluminum-polyimide micro-cables for the analogue signal transfer, and a custom-developed SMX read-out ASIC capable of measurement of the time ( $\Delta t \simeq 5$  ns) and amplitude. Dense detector integration enables material budget  $> 0.3\%$ ,  $X_0$ . The sophisticated powering and grounding keeps the noise under control.

In addition to its primary application in Silicon Tracking System of the future CBM experiment in Darmstadt, our detector will be utilized in other research applications.

**Summary (500 words):**

We present the recent development of a lightweight silicon micro-strip detector (DSSD) with the capability for accurate spatial, timing, and amplitude resolution of charged particle interactions. The technology is based on a  $300 \mu\text{m}$  double-sided double-metal  $p^+ - n - n^+$  micro-strip silicon sensor of various form-factors, ultra-light long aluminum polyimide micro-cables for the analogue signal transfer, and a custom-developed STS-MUCH XYTER (SMX) read-out ASIC capable of simultaneous measurement of the time ( $\Delta t \simeq 5$  ns) and amplitude (0.1 – 100.0 fC) of the interaction with the incident particle.

The detector assembly features dense integration, enabling a reduction in material down to 0.3%,  $X_0$  in the sensitive area. The read-out electronics, along with their associated support and cooling interfaces, can be located up to 500 mm away. The sophisticated powering and grounding concept of the detector reflects the necessity of synchronous reading of the both sides of DSSD sensor while also keeping the electronics noise under control.

In addition to its primary application in the Silicon Tracking System (STS) of the future heavy-ion fixed target Compressed Baryonic Matter experiment in Darmstadt, Germany, our detector is also being utilized in various research applications, such as the Tracker of the E16 hadron experiment at J-PARC and the \textsc{Strasse} tracker at the Radioactive Isotope Beam Facility at Riken in Japan. We also are exploring opportunities to expand its use to medical imaging, where the unique features of our detector could prove to be essential.

**Tuesday posters session / 199**

## **Characterization of the BigRock 28 nm Fast Timing Analog Front End**

**Authors:** Amanda Simone Krieger<sup>1</sup>; Amanda Simone Krieger<sup>1</sup>

**Co-authors:** Carl Grace ; Kennedy Caisley<sup>2</sup>; Maurice Garcia-Sciveres<sup>1</sup>; Timon Heim<sup>1</sup>; Zhicai Zhang<sup>1</sup>

<sup>1</sup> *Lawrence Berkeley National Lab. (US)*

<sup>2</sup> University of Bonn

**Corresponding Authors:** amanda.simone.krieger@cern.ch, akrieger@lbl.gov

A full characterization of the BigRock high-speed, low-power analog front end (AFE) will be presented. The BigRock AFE previously described in [1] has been refined in a second generation testbed ASIC, Pebbles. The AFE utilizes a current-mode signal path that has been designed for 4D tracking applications with precision time resolution of order 50 ps. The preamplifier concept is based on a prior art current-feedback CMOS topology in [2]. An on-chip test bench comprised of a variable injection circuit and high-resolution TDC measures the AFE timing resolution. An array of integrated load capacitors and IO IPs enhance the characterization capability.

#### Summary (500 words):

##### Summary

A succession of design refinements have been implemented in a common 2x2 mm testbed ASIC series. The family of 28 nm CMOS prototype ASICs, from initial to final are: BigRock, Pebbles, and MetaRock. The 1st chip in the series, BigRock, contains an IO design flaw that renders it untestable, as well as a bug in the digital TDC. Pebbles, the device now being characterized in the lab, ameliorates these flaws, and implements an array of on-chip input capacitor loads for characterizing the BigRock AFE noise from 0 to 100 fF. In this presentation, the critical metrics of noise-vs-power, timing dispersion, threshold tuning, ToT-vs-Qin, and timewalk will be covered.

The final prototype in the series, MetaRock, will be taped-out in June of 2023. MetaRock will have a full timing and charge readout AFE based on BigRock, including a new low power analog TDC suitable for implementation in a next-generation pixel readout ASIC for HL-LHC upgrades or other 4D tracking applications.

##### Background

The intent of the BigRock project is to develop a next-generation AFE capable of approximately the same performance requirements as the recently designed ItkPix/CROC readout for the HL-LHC upgrade, but adding a timing requirement, and at the new CERN/HEP target node of 28 nm for increased digital capability. The BigRock module of the Pebbles ASIC is comprised of 17 channels with two main modules:

- An AFE consisting of a preamplifier, comparator, and digital buffer
- An injection circuit and dual TDC with ~ 5 ps resolution, recording the ToT leading and trailing edge time referenced to a 1 GHz synchronous system clock

A low-power TDC will be a follow-on development included in the MetaRock tapeout, to complete the 4D front end. In the Pebbles iteration reported here, the channel TDC is intended only as an on-chip testbench for the AFE, avoiding timing uncertainties in the interface and test PCB. Therefore, the TDC in this prototype is essentially unconstrained in design parameters, excepting resolution. The digital TDC is described in [3].

A preamplifier based on the prior art in [2] is the central element of the BigRock prototype project. The analog requirements are namely:

- analog current consumption of ~4 uA
- noise < 100 e<sup>-</sup> RMS @ 50 fF detector capacitance
- ToA requirement of ~50 ps RMS resolution for 4D tracking
- ToT precision commensurate with timewalk correction
- performance met at a 0.15 fC threshold with 0.5 fC central charge injection

[1] Amanda Krieger, Kennedy Caisley, Maurice Garcia-Sciveres, Carl Grace, Timon Heim, "BigRock, a Fast Timing Front End for Future Pixels in a 28 nm CMOS Process, Conference poster," TWEPP 2022.

[2] Pierre Jarron, Francis Anghinolfi, Eric Delagne, Wlodek Dabrowski, Luitwin Scharfettera, "A transimpedance amplifier using a novel current mode feedback loop", NIM-A, 377 (1996), pp. 435-439.

[2] Kennedy Caisley, "A Monolithic Radiation-Hard Testbed for Timing Characterization of Charge-Sensitive Particle Detector Front-Ends in 28 nm CMOS", Master of Science Thesis, Graduate Program in Electrical and Computer Engineering, The Ohio State University, 2021.

Tuesday posters session / 200

## Design Updates for HPSoC: A very high Channel Density Waveform Digitizer with sub-10ps resolution

**Author:** Luca Macchiarulo<sup>None</sup>

**Co-authors:** Chris Chock <sup>1</sup>; Greg Uehara ; Isar Mostafanezhad <sup>1</sup>

<sup>1</sup> *Nalu Scientific, LLC*

**Corresponding Author:** isar@naluscientific.com

We present the architectural design, prototype fabrication and first results for the High Pitch digitizer System-on-Chip (HPSoC). The HPSoC is a high channel density and scalable waveform digitization ASIC with an embedded interface to advanced high-speed sensor arrays such as e.g. AC-LGADs. The chip is being fabricated in 65nm technology and targets the following features: picosecond-level timing resolution; 10 Gs/s waveform digitization rate to allow pulse shape discrimination; moderate data buffering (256 samples/chnl); autonomous chip triggering, readout control, calibration and storage virtualization; on-chip feature extraction and multi-channel data fusion.

**Summary (500 words):**

In recent years, the introduction of very fast optical sensors with extremely low pitches (e.g. Low Gain Avalanche detectors -LGADs) has enabled high-density designs for high energy and nuclear physics detectors offering excellent spatial and timing precision; the performance of detector systems composed of large arrays of such components is currently limited mostly by the readout capabilities of the existing readout electronics. To address these issues, we studied and designed the architecture of the HPSoC, a customized multi-channel waveform digitizing readout that is capable of directly interfacing with state-of-the-art sensor arrays, can extract relevant information from each pixel's interaction and internally combine such information in a compact digital format, with timing precision at the picoseconds level and capable of sub-pixel spatial precisions at a few tens of micrometers or less. The design has targeted the following specifications and features:

An input preamplification handling fast current-based sensors (~100 ps rise times);

A timing resolution of at least 5ps with a target of 1ps;

Very large integration (100+ channels) with modular tileable, scalable structure;

Waveform digitization of at least 10Gs/s, allowing for pulse shape discrimination;

Moderate data buffering (256 samples/channel);

Autonomous chip triggering and storage virtualization;

On-chip feature extraction and multi-channel data fusion;

In this presentation we concentrate on the features related to the digitization and data processing as the preamplification has been described elsewhere.

The architectural design of the HPSoC was performed based on the following ideas:

A dense sensor array has all its outputs connected directly to the input of the HPSoC. The connection is performed through bump bonding to area IOs on the ASIC:

The HPSoC is modularly built as an equivalent array of "tiles", each fully capable of independently gathering data from the corresponding pixel.

The signal is initially going through an analog conditioning stage composed of a transimpedance amplifier to convert the current input into the proper input voltage range for the subsequent processing

A mixed signal section performs then a continuous waveform sampling while a trigger (external or generated by a local discriminator) selects a subset of samples for digitization.

The digitized data is then transferred to a digital component that performs on the fly amplitude and timing calibration, and extracts timing and amplitude (charge) information.

The time and charge information is finally transferred to a data concentrator that can optionally perform data fusion to provide an accurate estimation of the arrival position with a sub-pixel accuracy, and a sub-sampling time estimate of the event arrival.

In order to demonstrate the feasibility of the design and test some of its critical components, a prototype chip containing most of the parts and with 4 fully functional channels was fabricated. The digital front end and back ends have also been designed for future integration. The chip is currently under evaluation and we will report the results of the first measurements. Upon satisfactory test completion, we will proceed designing, fabricating and testing a fully functional revision incorporating front end and back end digital partitions.

## Design updates for AARDVARCv4: Waveform Sampling System On Chip with Picosecond Timing Resolution

**Author:** Isar Mostafanezhad<sup>1</sup>

**Co-authors:** Chris Chock<sup>1</sup>; Dean Uehara<sup>1</sup>; Gary Varner<sup>2</sup>; Greg Uehara; Luca Macchiarulo; Ruth Perron<sup>1</sup>

<sup>1</sup> *Nalu Scientific, LLC*

<sup>2</sup> *University of Hawaii*

**Corresponding Author:** isar@naluscientific.com

In this article we describe the measurement results on an “AARDVARC” prototype in 130 nm. AARDVARC is a multi-channel waveform digitizing and processing Application Specific Integrated Circuit (ASIC) front-end. We report on various performance metrics: fast sampling (10-14 Gsa/s), deep storage (32K samples), timing resolution (better than 5ps), low power consumption (<100mW/channel).

### Summary (500 words):

State of the art large collider experiments pose conflicting requirements to the data acquisition electronics: extreme integration and density, extremely good timing accuracy, low power, high data transfer rates, large radiation awareness. The sheer number of channels also calls for reduced per-channel cost. In order to achieve accuracy goals, fast waveform sampling and digitization are often preferred to allow for tracking of radiation degradation of the light detectors, pile up events and ultra precision timing resolution.

Through higher integration with analog signal conditioning, waveform sampling, digital readout and signal processing with extended digital functions on chip, the AARDVARC allows for flexible digital signal processing within the front-end which reduces the amount of data needed to be transferred to the backend. The device performs continuous sampling and deep analog storage and on-demand or self-triggered digitization of analog storage, packetization and digital transmission (with parallel or serial interfaces). The AARDVARC v4 ASIC has been fabricated in 130nm process (in Dec 2022). In this paper we cover various measurement results from the testing campaign.

**Voltage Noise/RMS:** due to the distributed nature of the ADC conversion, the individual samples are subject to large recording offsets (“pedestals”), that need to be measured, recorded and corrected. The remaining errors in voltage conversion after this correction are due to noise during conversions, and have been measured for each storage sample position. The typical errors are normally distributed with a standard deviation of approximately 0.7 mV.

**Sampling Speed:** AARDVARC uses an internal Delay Locked Loop (DLL) to adjust and control a variable delay line - by controlling the frequency of an input clock it is therefore possible to automatically adjust the sampling frequency. The sampling speed of the AARDVARC was measured by feeding a fast periodic input (approximately 1GHz). The results for a sampling frequency of 13 GSa/s will be presented.. Effect of sampling rate on various ASIC parameters has been studied.

**Accuracy/Sample jitter:** To better study the achievable accuracy, the individual sample stability was investigated by feeding a signal whose phase relationship with the sampling clock was known and with jitter better than 100 fs. By varying the phase and repeating the measurement, jitter as a function of sampling array position was investigated, as it was expected that it would increase with integrated delay across the delay chain. The delay distribution for an individual sample position will be presented. Both measurements are performed at a sampling rate of 13 GSa/s. At this sampling rate, the figure shows that individual samples have a stable timing with a standard deviation of less than 2.5ps across the entire sampling space. Other experiments show that the accuracy is higher for higher sampling frequency - this is understood, and due to the specifics of the delay line. Methods to better control jitter at lower sampling rates are now being studied and will be implemented in the next revision of the AARDVARC.

System Design, Description and Operation / 204

## Outer Barrel services chain characterization for the ATLAS ITk Pixel Detector

**Author:** Leyre Flores Sanz De Acedo<sup>1</sup>

**Co-authors:** Aaron Paul O'Neill<sup>2</sup>; Daniele Dal Santo<sup>3</sup>; Michele Weber<sup>2</sup>; Silke Mobius<sup>2</sup>; Susanne Kuehn<sup>1</sup>

<sup>1</sup> CERN

<sup>2</sup> Universitaet Bern (CH)

<sup>3</sup> Universität Bern

**Corresponding Author:** leyre.flores.sanz.de.acedo@cern.ch

For the high-luminosity upgrade of the ATLAS Inner Tracking detector, a new pixel detector will be installed to allow for a bigger bandwidth and cope with the increased radiation among other challenges. This contribution will present the evaluation of the Outer Barrel Pixel layer services chains. A full data transmission study covering data merging will be presented from the pixel module all the way to the FELIX data acquisition system, using most of the components foreseen for the detector. Challenges and results of the services chain of the Outer Barrel will be highlighted.

**Summary (500 words):**

In the high-luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of ITk will consist of a pixel detector, with an active area of about 14 m<sup>2</sup>.

The layout of the pixel detector is foreseen to have five layers of pixel silicon sensor modules in the central region and several ring-shaped layers in the forward regions. Beside the challenge of radiation hardness and high-rate capable silicon sensors and readout electronics many system aspects have to be considered for a fully functional detector. The modules will be powered serially in chains up to 14 modules to reduce the power consumption. Both stable and low mass mechanical structures and high-rate capable services are important.

This contribution focuses on the results of the services realization for the outer central layers of the detector, the Outer Barrel (OB). The OB will have 4472 pixel quad modules, arranged on 158 light-weight carbon fibre local support structures (longerons and inclined-half rings). The services chain extends from the FELIX data acquisition system all the way to the module flex PCBs inside the detector. It is composed of custom flex-rigid circuits (type-0 and type-1 OB services) which vary for longerons and inclined half-rings. These so-called PP0s and pigtailed are then connected with adapter PCBs to custom twinax cables, and terminated to PCBs with the ASICs that recover data, GBCR, serialize and deserialize data, lpGBT (low power Gigabit Transceiver), and that transform light into electrical signals, VTRx. Optical fibres connect then to the readout hardware hosted in racks.

In the presentation, the latest results and full evaluation of the services chain tests between pixel modules with the most recent front-end chip and the readout system are presented. Important qualification steps of the system design and its operation are discussed. The lack of physical space in the detector means that in the OB either one or two front-end chips receive the data from the others and it comes all out in one or two links at 1.28 Gbps. The functionality of this so-called data merging is crucial for the verification of the data transmission chain. Moreover, the operation of several quad modules at full speed and including the opto-components is important. These key aspects for future operation of the detector are measured and analysed in detail. The outcome of these tests is relevant to fully qualify the services chain, aiming to continue with the pre-production and production phases for several flavours of these detector components.

**Thursday posters session / 205**

## **MightyPix at the LHCb Mighty Tracker –Verification of an HV-CMOS pixel chip's digital readout**

**Author:** Sigrid Scherl<sup>1</sup>

**Co-author:** Nicolas Striebig <sup>2</sup>

<sup>1</sup> *University of Liverpool (GB)*

<sup>2</sup> *KIT - Karlsruhe Institute of Technology (DE)*

**Corresponding Author:** sscherl@hep.ph.liv.ac.uk

A new HV-CMOS pixel chip, called MightyPix, is being developed for the Mighty Tracker, an upgrade planned for LHCb in anticipation of the HL-LHC. Extensive research is ongoing to study the tracks and occupancy at the Mighty Tracker. This data is now used to simulate MightyPix's performance in the LHCb environment, with focus on the digital readout. First results show an efficiency of 99.7% for MightyPix for the highest hit rates expected at the Mighty Tracker, which reach 17 MHz/cm<sup>2</sup>. The bottleneck was found to be the readout speed, which yielded new design ideas to further improve the digital readout.

#### **Summary (500 words):**

Part of the upgrade towards the High Luminosity LHC, is the development of a new tracker for the LHCb experiment. This tracker, called Mighty Tracker, will be hybrid, combining scintillating fibres in the outer regions and silicon sensors in the inner regions, where the hit density and radiation damage are highest. For the silicon region, a new HV-CMOS pixel chip, called MightyPix, is currently being developed. The first prototype, MightyPix1, is the first monolithic silicon sensor that has a digital periphery compatible with the LHCb online system. Various studies are ongoing to ensure that the Mighty Tracker will prove successful.

On the one side, the particle tracks and occupancy at the tracker are studied in simulations, while on the other side the general MightyPix functionality is verified by the chip designers. The studies presented here provide an interface between the two. Using the Mighty Tracker simulation data and a behavioural model of MightyPix1, representing the analogue pixel matrix, together with the synthesised digital logic, the chip's performance within the LHCb environment is characterised. The focus lies on the digital readout of MightyPix1, to validate that the chip can handle the highest particle hit rates at the Mighty Tracker, which are expected to reach 17 MHz/cm<sup>2</sup>. Studying the efficiency (which decreases with increasing occupancy) over the whole silicon region of the tracker can inform decisions on the number of readout links in different tracker areas. Looking at the behaviour of the digital readout can additionally reveal bottle necks in the design. The idea behind this verification process is to provide a simple framework on top of the Cadence tool chain, written in python, to make use of the complex work done in different areas, namely the extensive simulations of particle tracks and the design of the HV-CMOS pixel chip. The framework is constructed for an easy exchange of simulation data as well as chip model, making it possible to use it for different chips and environments.

First simulation results yield an efficiency of 99.7% for hit rates of 17 MHz/cm<sup>2</sup> (Fig. 1), showing that MightyPix1 can handle the maximum rates expected at the Mighty Tracker. Further investigations show the limiting factor being the readout time of the hits. For 17 MHz/cm<sup>2</sup> the maximum readout times lie around 7 us, while for 50 MHz/cm<sup>2</sup> they reach 190 us (Fig. 2). This is due to the much higher number of hit buffers (one for each of the 9280 pixels) compared to the column buffers (one for each of the 29 columns). Increasing the number of column buffers by a factor two means the hits can be read from the hit buffers twice as fast. For a hit rate of 50 MHz/cm<sup>2</sup> this reduces the peak readout times to 100 us (Fig. 3) and increases the efficiency of MightyPix1 from around 84% to over 96%. Although such high rates are not expected for the current Mighty Tracker design, the new readout scheme would permit installing MightyPix chips even closer to the beam pipe.

**Module, PCB and Component Design / 206**

## **The OBDT-theta board: time digitization for the theta view of Drift Tubes chambers.**

**Author:** Javier Sastre Alvaro<sup>1</sup>

**Co-authors:** Alvaro Navarro Tobar<sup>1</sup>; Clara De Lara<sup>1</sup>; Cristina Fernandez Bedoya<sup>1</sup>; David Daniel Redondo Ferrero<sup>1</sup>; David Francia Ferrero<sup>2</sup>; Ignacio Redondo Fernandez<sup>1</sup>; Jaime Leon Holgado<sup>1</sup>; Sergio Cuadrado Calzada<sup>1</sup>

<sup>1</sup> *CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)*

<sup>2</sup> *Cent.de Investigac.Energeticas Medioambientales y Tecnol. (CIEMAT)*

**Corresponding Author:** javier.sastre@ciemat.es

We present the design and performance of the new On-Board electronic for the Drift Tubes (OBDT) for the superlayer theta along the direction parallel to the beam-line, built to substitute part of CMS DT Muon on-detector electronics. The OBDT-theta is responsible of the time digitization of DT chamber signals for the theta view, allowing further barrel muons tracking and triggering. It's also in charge of part of the slow-control of the DT chamber systems. A prototype is being tested in the laboratory and in a demonstrator inside CMS, as well as the full functionality in real conditions, showing satisfactorily results.

**Summary (500 words):**

The on-detector electronics of the CMS Muon DT chambers will need to be replaced for the HL-LHC operation due to the increase of occupancy and trigger rates in the detector, which cannot be sustained by present system. The OBDT-theta boards, together with OBDT-phi boards, will be located inside mini-crate mechanics attached to the DT chamber, inside the CMS volume. It will be in charge of performing the 1 ns time digitization of the DT chamber signals of the theta view and the multiplexing for further transmission to the readout and trigger backend electronics. This board is also in charge of some of the slow-control tasks needed by part of the DT chamber system. There will be 180 boards representing roughly 1/5 of all the OBDT boards in the system. The OBDT-theta board has been built around a Microsemi Polarfire FPGA, responsible of the time digitization of up to 228 input signals. It implements a deserialization method which runs at 600 MHz and allows obtaining a time bin of 0.833 ns. The input data is forwarded to the output optical link for data transmission to the readout and trigger chains. Communication for this prototype is based on two VTRx+ transceivers that provide two bi-directional links for slow-control and six transmitter links, capable to output data up to 10.24 Gbps to the backend system. One of the bi-directional links goes to the lpGBT chip in the OBDT board, that provides the main slow-control functions and reception of LHC clock and some TTC signals. The other one is directly connected to the FPGA serving as a secondary slow-control to recover OBDT in case of loss of main slow-control. The protocol implemented so far follows lpGBT protocol for all links. The lpGBT chip plus a SCA chip in the board allow clock and synchronization reception as well as e-link implementation for configuration and monitoring of the Microsemi FPGA. Through this link it is also possible to implement the different slow-control functionality of the barrel system, such as setting the front-end discriminators thresholds and bias values, implementation of the I2C links for temperature monitoring and channel masking, communication to the PADC, RPC and Alignment slow-control chains and finally, control of the test pulse generation mechanisms that allows to perform the DT chamber time measurements calibration for the theta view superlayers. A prototype of this board has been produced and is being tested both in the laboratory and also in different test stands with DT chambers and other phase-2 electronics prototypes. The different functionality of the OBDT-theta board has been verified and the overall architecture has been validated both through specific tests and through cosmic ray and LHC collisions data taking integrated with the rest of the DT system. The OBDT-theta architecture together with its performance results will be presented in this contribution, showing the goodness of the design for the expected functionality during HL-LHC.

**System Design, Description and Operation / 209**

## **Design and implementation of the Hybrid Detector for Microdosimetry (HDM): Challenges in readout architecture and experimental results**

**Authors:** Chiara La Tessa<sup>None</sup>; Christoph Schuy<sup>None</sup>; Enrico Pierobon<sup>None</sup>; Marta Missiaggia<sup>1</sup>; Vincenzo Monaco<sup>2</sup>

<sup>1</sup> *INFN - National Institute for Nuclear Physics*

<sup>2</sup> *Universita e INFN Torino (IT)*

**Corresponding Author:** enrico.pierobon@unitn.it



This talk presents the Hybrid Detector for Microdosimetry (HDM), capable of providing a superior characterization of the radiation field. This is of critical importance in radiation therapy, where a better description of the radiation field can lead to a better treatment plan and, therefore, a better treatment outcome.

HDM is composed of a commercial gas microdosimeter, TEPC, and a tracker made of 4 silicon LGADs layers. This presentation will cover the challenges in implementing the HDM readout architecture, including synchronization and triggering, and will show first measurements obtained with clinical protons.

#### Summary (500 words):

Over the past 30 years, clinical results have shown that ion therapy may be a superior treatment option for several types of cancer, including recurrent cancers, compared to conventional radiation. Despite these promising results, there are still several treatment uncertainties related to biological and physical processes that prevent the full exploitation of particle therapy.

Among the physical characterizations, it is paramount to measure the quality of the irradiating field in order to link the biological effect to its physical description. In this way, uncertainties in treatment can be reduced and outcomes optimized. One tool for studying the radiation field that has become increasingly important in the last decade is microdosimetry. The latter provides a description of radiation at the micrometer level typical of cell dimensions, where energy deposition exhibits stochastic behavior. In microdosimetry, the fundamental quantity is the lineal energy  $y$ , defined as the energy deposition in the detector divided by the Mean Chord Length (MCL): an approximation used to estimate the track length traveled by radiation in the detector, valid in an isotropic, uniform radiation field. A more accurate description of the radiation field can be obtained by replacing the mean chord with the actual track traveled by radiation in the detector.

Following this rationale, we designed the Hybrid Detector for Microdosimetry (HDM), composed of a commercial gas microdosimeter Tissue Equivalent Proportional Counter (TEPC) followed by 4 silicon detector layers of Low Gain Avalanche Detectors (LGADs) strips, capable of measuring the actual track length.

Although HDM has been validated and optimized with Monte Carlo simulations, the readout implementation of this detector is still a technological challenge.

As a two-stage detector, the information obtained is interdependent. The energy deposited in the TEPC is correlated with the corresponding particle track observed by LGADs.

Specifically, the signal generated by the TEPC, after being amplified by three different amplification lines, is digitized by three FPGA-controlled ADCs. Since the FPGAs are based on the Zynq architecture, the approximately 100 Mbps data stream is sent to the processor via Direct Memory Access (DMA) and then to a PC via TCP-IP protocol, where it is stored. The signal from the LGADs is managed by dedicated ASICs capable of setting the thresholds and producing a digital signal when the strips are activated. Four layers are required to spatially identify two points along the particle track, for a total of 284 channels. Again, FPGAs are used to manage the readout, one for each layer.

In this talk, I will give a detailed description of the HDM readout architecture and discuss the main challenges, namely synchronization and triggering, and how we are addressing them. In addition, I will show the first experimental data obtained with clinical protons at the Trento Proton Therapy Facility, where layers of HDM were characterized over different experimental conditions.

#### Thursday posters session / 212

## Time-Delay-Based Analog Front-End for Monitored Drift Tubes in 65 nm CMOS with < 200 ns Baseline Recovery Time and Coherent Time-over-Threshold

**Author:** Syed Adeel Ali Shah<sup>None</sup>

**Co-authors:** Andrea Baschiroto<sup>1</sup>; Hubert Kroha<sup>2</sup>; Marcello De Matteis<sup>1</sup>; Robert Richter<sup>2</sup>; Usman Amin<sup>1</sup>

<sup>1</sup> UNIMIB

<sup>2</sup> Max-Planck-Institute for Physics

**Corresponding Author:** s.shah4@campus.unimib.it

Monitored Drift Tube (MDT) chambers for muons detection at ATLAS Experiment adopt analog front-end read-out electronics for precise-tracking/momentum measurements of detected particles [1]. State-of-the-art has historically used bipolar shaping electronics (at approximately 800 ns baseline recovery time [2]) that scarcely fits with High-Luminosity (HL) requirements where small-MDT (sMDT [3]) are used at 180 ns input signal time-width. This brief presents 4-channels Application Specified Integrated Circuit in 65 nm CMOS for sMDT signal amplification and shaping that performs < 200 ns baseline recovery time and avoids distortion of Time-over-Threshold (ToT) characteristic due to multiple close input charge pulses composing sMDT signal.

#### Summary (500 words):

**Introduction.** ATLAS (s)MDT charge-to-voltage conversion is performed by Charge-Sensitive-Preamplifier (CSP) feeding analog signal processing stages differentiated by Unipolar or Bipolar shaping circuits. Due to complex requirements of unipolar shaping circuits bipolar shaping schemes are preferred.

However, in classical readout electronics [2], Bipolar shaping circuits suffer from long Baseline Recovery Time (BLR), higher than 800 ns, unfit for >1 MHit/sec required by HL-sMDT experiments [3]. Another drawback with current readout electronics is that the secondary pulses due to main track superimpose the main pulse, hence the ToT is not correlated to the main pulse. These problems are even more critical in sMDT chamber which has a drift-time of 180 ns. To profit from high data rate sMDT performance, BLR time must be less than the drift-time and ideally with no pile-up effects.

**Method.** The proposed ASIC is based on an innovative time-delay-based technique that significantly accelerates the BLR time performance. The qualitative block-scheme and time-domain evolution of the proposed approach are shown in Fig. 2. The incoming sMDT multiple charge signal is processed by <10 ns rising time CSP for charge-to-voltage conversion. Key performance parameters of CSP are fast peaking-time and noise performance which are optimized by using high input device transconductance (i.e. = 25 mA/V). CSP output feeds a Low-Pass-Filter (LPF) whose differential input signal is composed by voltage difference between the CSP output and a delayed replica. In this way, along the rising time of the CSP output voltage, the LPF output signal maintains the fast shaping while along the decay phase accelerates the BLR time, removing some electrical power from CSP main pulse output signal.

Delay Stage is composed by simple phase-shift R-C network feeding a voltage buffer for driving LFP input impedance. This way, the LPF performs both single-to-differential and unipolar-to-bipolar conversion of the CSP output voltage signal. Accuracy of the phase shift is essential and for this reason the capacitor of the Delay Stage is designed by binary weighted 5-bit programmable capacitor array to achieve a programmable time delay. Finally, the resulting < 180 ns BLR time bipolar signal is fed into comparator which compares it with a programmable threshold value to generate ToT signal. The complete electrical scheme of the integrated analog front-end is shown in Fig. 3,

**Results.** Single channel design is validated by both ideal  $\delta$ -Dirac input pulse (Fig. 4) and sMDT Garfield signal (Fig. 5-6) (swept in 5-100 fC range) by Post-Layout Extracted View (PEX) simulations.

Fig. 4 displays a peaking time of 13 ns with sensitivity (Output voltage/Input charge) of 8 mv/fC. BLR time is reduced, by 78% as compared to classical models, to 165 ns that is even less than drift time of sMDT chamber.

Fig. 4-7 shows time domain evolution of the output signals of CSP, Delay Stage, LFP and discriminator vs input signal. Fig 8 shows ToT range as input charge pulse varies from 5-100 fC. Secondary pulses crossing threshold value are suppressed by asynchronous finite state machine logic triggered by falling edge of ToT.

Invited / 213

## FPGA Firmware design with High Level Synthesis: Methodology, gains, and pitfalls

Author: Michalis Bachtis<sup>1</sup>

<sup>1</sup> UCLA

Corresponding Author: michail.bachtis@cern.ch

High Level Synthesis (HLS) of FPGA firmware using C/C++ has been popular in the design of upgrade trigger systems in High Energy Physics, allowing physicists with no previous firmware expertise to efficiently design digital systems. This presentation will describe the methodology of HLS

designs, including comparison of basic building block design of HLS and Hardware Description language (HDL).

Design examples from the CMS L1 trigger system will be presented along with pitfalls to provide a proposed efficient approach to system design with these methods

**Summary (500 words):**

Firmware development using High Level Synthesis (HLS) of C/C++ code is a novel methodology that enables fast development of FPGA firmware by directly converting C++ code to Hardware Description language (HDL) using a set of conversion rules. The method has been successful in high energy

physics experiments, allowing graduate students to contribute to firmware development, increasing the effective personpower on the relevant projects.

This presentation will cover the basic methodology, the lessons learned from its application in Run-3 and HL-LHC trigger upgrade of CMS, and pitfalls to avoid when using HLS.

Initially, the methodology of writing C code while thinking in parallel will be explained, along with the code optimizations (pragmas) used to map the C code to HDL logic. Details will be provided on how to

control the pipeline and map logic to specific hardware. Examples

of simple modules will be provided comparing a direct HDL implementation with an HLS one comparing

utilization, clock speed, and latency. The HLS gains in DSP related developments and in synchronization of different pieces of logic will be demonstrated. Examples where the method does not succeed in creating good logic will be shown, along with strategies on how to avoid these problems. The talk will be tailored to the level of young engineers and graduate students starting with HLS development for their projects.

**System Design, Description and Operation / 216**

## **Design and performance of the front-end electronics of the charged particle detectors of PADME experiment**

**Authors:** Paola Gianotti<sup>1</sup>; Simeon Ivanov<sup>2</sup>

<sup>1</sup> INFN Laboratori Nazionali di Frascati (IT)

<sup>2</sup> Sofia University, Bulgaria

**Corresponding Authors:** simo@phys.uni-sofia.bg, paola.gianotti@cern.ch

The PADME experiment at LNF-INFN employs positron-on-target-annihilation technique to search for new light particles. Crucial part of the experiment are the charged particle detectors, composed of plastic scintillator bars with light transmitted by wavelength shifting fibers to silicon photomultipliers (SiPM). The location of the detector –close to a turbomolecular pump, inside a vacuum tank, and exposed to 0.5 T magnetic field –has driven the design of custom modular SiPM front-end and power supply electronics. The design of the system and its performance, confirming the desired sub-ns resolution on the reconstructed particle times, will be shown and discussed.

**Summary (500 words):**

The PADME experiment aims to search for new light particles by performing a precise measurement of the final state products of the interaction of accelerated positrons in a thin diamond target. The charged particle detector system of the experiment has to detect deflected by 0.5 T magnetic field electrons and positrons with higher than 99% efficiency and less than 1 ns time resolution, to provide the required vetoing capabilities of the Standard Model background channels. In addition, by design, the PADME experiment uses a vacuum tank with pressure less than 10<sup>-6</sup> mbar to decrease beam-gas interaction probability. The adopted solution was a plastic scintillator detector composed of polystyrene bars with a WLS fiber, placed inside a groove along the bar, with light detected by 3 x 3 mm<sup>2</sup> Hamamatsu S13360 silicon photomultipliers (SiPM).

Custom front end electronics modules were designed, composed by a controller, located outside close to the major data acquisition components of PADME experiment, and front-end cards with SiPMs, placed

inside the vacuum tank and the 0.5 T magnetic field. The controller delivered low voltage, a fixed 100 V high voltage, and communicated through I2C with the front-end cards to allow bias voltage configuration and SiPM voltage, current, and temperature monitoring. In addition, the controller also provided ethernet connectivity with web-interface to facilitate the user configuration and monitoring.

The front end card hosted a configurable high voltage generator to provide bias to each of the SiPMs. To ensure stability, the initial stage of the bias voltage generator was realized as a current generator followed by a DAC regulated comparator. The signal from the SiPM was preamplified with a fixed gain (4 in PADME case) and then the output signal was formed by a differential line driver, which showed very high immunity against externally induced electromagnetic noise. The differential signals were taken via a feed-through flange and about 10 m long line back to the controller, where they were converted to single ended, to match the chosen digitization electronics. A single front-end card served four independently configurable SiPMs.

The described SiPM front end electronics served more than 200 readout channels for extended periods inside the magnet in vacuum with temperature ranging from 15°C to 46 °C, without degradation of its nominal performance.

Thursday posters session / 217

## The Optosystem: validation and testing of the high-speed optical-to-electrical conversion system for the readout of the ATLAS ITk Pixel upgrade

**Author:** Silke Mobius<sup>1</sup>

**Co-authors:** Aaron Paul O'Neill<sup>1</sup>; Daniele Dal Santo<sup>2</sup>; Michele Weber<sup>1</sup>; Roman Mueller<sup>1</sup>; Susanne Kuehn<sup>3</sup>; Vakhtang Tsiskaridze<sup>4</sup>

<sup>1</sup> *Universitaet Bern (CH)*

<sup>2</sup> *Universität Bern*

<sup>3</sup> *CERN*

<sup>4</sup> *University of Toronto (CA)*

**Corresponding Author:** silke.mobius@cern.ch

After Run III the ATLAS detector will undergo a series of upgrades to cope with the harsher radiation environment and increased number of proton interactions in the High Luminosity-LHC. One of the key projects in this suite of upgrades is the ATLAS Inner Tracker (ITk). The pixel detector of the ITk must be read out accurately and with extremely high rate. The Optosystem performs optical-to-electrical conversion of signals from the pixel modules. We present recent results related to the performance of the data transmission chain pivoted on the Optoboards and to the design, testing and production of the Optopanel.

### Summary (500 words):

In the High Luminosity-LHC (HL-LHC) the number of proton interactions per bunch crossing is set to increase drastically and so the amount of radiation components are exposed to will also increase. The ATLAS detector will perform a suite of upgrades to cope with these challenges. The ATLAS Inner Tracker (ITk) will provide high precision tracking while being resistant to the high levels of radiation it will receive over its lifetime. The ITk Pixel is at the very heart of the experiment and, critically, the data from the modules must be read out and sent to the ATLAS counting rooms with high precision. The quality of the electrical signals produced by the detector would be compromised by the differential loss along the cables connecting the detector to the counting room. So, an optical-electrical conversion system known as the Optosystem was proposed as a solution.

The Optosystem takes electrical signals from the front-end sensor modules (uplink) via twinax cable to the Optopanel. These are four mechanical structures, located at each end of the ATLAS detector. Each Optopanel houses 28 Optoboxes and these house the Optoboards. The Optoboard can be considered the heart of the Optosystem. These devices host four signal recovery ASICs (Gigabit Channel Receivers,

GBCRs), four ASICs for signal aggregation (low power Gigabit Transceivers, lpGBTs) which pass the uplinks to a final ASIC for optical conversion (VTRx). The command-and-control lines coming towards the front-end modules (downlinks) undergo the reverse process.

In this talk we present an introduction to the ATLAS ITk Optosystem and to its performances. The validation and signal quality checks of the Optosystem are gauged using many robust techniques, including monitoring of PRBS7 pattern and idle signal produced by the front-end electronics of the ITk Pixel. An estimate of the 95% Confidence Level Bit Error Ratio (BER) is used to quantify the goodness of the data transmission. Strict requirements on data quality impose that the BER must be less than  $10^{-12}$  at 95% CL.

Results related to the powering of the Optoboards will also be reported: two separate DC-DC step down converters, used to provide the Optoboards with the correct tensions, have been designed and tested.

The progress on the construction and testing of the Optoboxes will be outlined.

Finally, a Graphical User Interface (GUI) has been developed to allow easy control over the complex Optoboards and the overall Optosystem. Information about the integration of this GUI with the software under development for the ITk Pixel System Test will be provided.

## Module, PCB and Component Design / 218

### Lessons from integrating CMS Phase-2 back-end electronics and first results from Serenity-S1, a production optimised ATCA blade.

**Authors:** Gregory Michiel Iles<sup>1</sup>; Torben Mehner<sup>2</sup>

**Co-authors:** Alexander Howard<sup>1</sup>; Andrew William Rose<sup>1</sup>; Charles Ralph Strohman<sup>3</sup>; Denis Tcherniakhovski<sup>2</sup>; Duncan Parker<sup>1</sup>; Fabrizio Palla<sup>4</sup>; Giacomo Fedi<sup>1</sup>; Luis Ardila<sup>5</sup>; Magnus Loutit<sup>6</sup>; Mark Pesaresi<sup>1</sup>; Marvin Fuchs<sup>2</sup>; Matthias Norbert Balzer<sup>2</sup>; Michael Schleicher<sup>7</sup>; Oliver Sander<sup>2</sup>; Sam Mansbridge<sup>8</sup>; Tom Williams<sup>9</sup>

<sup>1</sup> Imperial College (GB)

<sup>2</sup> KIT - Karlsruhe Institute of Technology (DE)

<sup>3</sup> Cornell University (US)

<sup>4</sup> Universita & INFN Pisa (IT)

<sup>5</sup> KIT-IPE

<sup>6</sup> University of Bristol (GB)

<sup>7</sup> KIT

<sup>8</sup> Imperial College London

<sup>9</sup> Rutherford Appleton Laboratory (GB)

**Corresponding Author:** torben.mehner@kit.edu

The Serenity-S1 is a Xilinx VU13P based Advanced Telecommunications Computing Architecture (ATCA) processing blade that has been optimised for production. It incorporates many developments from prototype cards and where possible adopts solutions being used across CERN. It uses many new parts because commonly used parts have disappeared from the market during the semiconductor crisis with only some returning.

We discuss improvements to simplify manufacture, the performance of new components, some of the more difficult aspects of procurement, the performance of production-grade Samtec 25 Gb/s optical firefly parts and issues with the rack cooling infrastructure.

#### Summary (500 words):

At least 500 Serenity-S1 cards will be needed to provide back-end electronics to the CMS Tracker, Level-1 Trigger, and High Granularity Calorimeter. They will be used to interface to the front-end electronics within the detector and also provide a firmware platform for processing data, particularly for running trigger algorithms.

The card uses a modular approach that splits the service area, which provides infrastructure that is needed on all ATCA cards, and the payload area, which contains all application-specific components. The service area is situated towards the backplane and includes the Intelligent Platform Management Controller (IPMC), an Ethernet switch, and a Xilinx KRIA System-on-Module (SoM) that is based on a Zynq Ultrascale+ System-on-Chip (SoC).

The payload is specific to the Serenity-S1 board and includes a Xilinx VU13P FPGA as the main processing unit as well as Samtec FireFly optical transceivers that are used to transmit data to and from the FPGA. There are 10 FireFly 12-channel transmitters and receivers each, as well as one single 4-channel bi-directional FireFly on the board, all of which are capable of running at 25 Gb/s depending on the type of firefly installed.

The card also contains features to protect itself in case of unexpected events. For example, loss of 48 V power will trigger a controlled shutdown of the card within a few ms before locally stored energy is exhausted. This ensures all power supply sequencing requirements are met, not just at power-up, but also at power-down.

Due to component shortages, we were not able to use the already evaluated Skyworks Si5395A jitter cleaners and switched to the recently released Microchip ZL30274 as well as new power supply modules for the FPGA. Because the availability of our core power supply, the LTM4700, is still uncertain, we also implemented a redundant solution using high-current power connectors and an additional power module based on industry-standard multiphase converters.

To accommodate the increased power requirement of ATCA cards new 2U, short depth heat-exchangers have been designed to remove up to 7 kW instead of the 2.3 kW 1U heat exchangers used for Versa Module Eurocard (VME). However, they require increased water flow and water pressure, which has an implications on the rack cooling infrastructure. An investigation into racks used by the Tracker for test and development will be presented, along with how it pertains to the underground system.

Production is expected to span 2024 and 2025 starting with a pre-series of about 50 cards in early 2024. Procurement is complicated by several issues. For example, the cards must be manufactured with a high yield due to high cost of free-issued components, but simply demanding this risks deterring companies from tendering.

The 25 Gb/s FireFly optical links are a new product which has also required extensive performance evaluation (Bit-Error-Rate (BER), pattern integrity and attenuation tolerance) and lifetime testing.

First results from Serenity-S1 will presented along with a discussion of the issues raised above.

ASIC / 225

## **A low crosstalk 768-channel of 14-bit analog to digital converters for high resolution array of detectors.**

**Authors:** Daniel Dzahini<sup>1</sup>; Etienne Leheurteur<sup>2</sup>; Laurent Gallin-Martel<sup>3</sup>; Mohamed Zeloufi<sup>2</sup>

<sup>1</sup> *Tima Laboratory / CNRS*

<sup>2</sup> *Xdigit*

<sup>3</sup> *LPSC/IN2P3 Grenoble*

**Corresponding Author:** dzahini@univ-grenoble-alpes.fr

This paper reports the design and measurement results of a 768-channel of 14-bit analog to digital converters. Each channel's layout pitch is only 8.5 $\mu$ m with a sampling rate from 40KS/s up to 100KS/s. Testing results show a crosstalk about only +/- 1 LSB. The architecture of the circuit and the structure of the layout make it extensible to exceptionally large format of detectors beyond 1000 channels. The circuit is produced to be used as a side element for multi-channel readout systems or alternatively as an IP to be transferred inside very dense integrated circuits.

**Summary (500 words):**

For many physics and photonics applications, silicon detectors are increasingly used, and their density will continue to grow for next generations. This creates the need of very dense readout circuits in which the analog to digital stage will play a crucial role. The reduced pitch makes the layout particularly challenging for high resolution mixed signal circuits as converters. We report here the results of 14-bit array of analog to digital converters compatible with pixels' pitch of  $8.5\mu\text{m}$ . The crosstalk is measured about  $\pm 1$  LSB. This hybrid architecture of converter dissipates in total  $110\mu\text{W}/\text{channel}$  when sampling at 40KHz rate. Each channel includes its own reference voltage buffers. This strategy paves the way for more dense arrays beyond one thousand channels of 14-bit resolution in the future. This prototype was produced in a 130nm process, and the total surface of the die is  $6\text{mm} \times 4\text{mm}$ . The integral non-linearity (INL) is  $\pm 5/-9$  LSB over a single-ended dynamic range from 0.6V to 2.9V with a power supply of 3.3V. The noise is less than 4 LSB rms when all the channels are fully working. We show the die photograph in an additional document.

**Tuesday posters session / 226****The first full size full functionality ETROC2 (16x16) prototype for CMS MTD Endcap Timing Layer (ETL) upgrade**

**Author:** Tiehui Ted Liu<sup>1</sup>

<sup>1</sup> *Fermi National Accelerator Lab. (US)*

**Corresponding Author:** [tiehui.ted.liu@cern.ch](mailto:tiehui.ted.liu@cern.ch)

The Endcap Timing ReadOut Chip (ETROC) is designed to process LGAD signals with time resolution down to about 40-50ps per hit. The ETROC2 is the first full size (16x16) prototype design with the front-end based on and scaled up from the ETROC1 (4x4). The readout designs at pixel and global level and the system interfaces are all new and are compatible with the final chip specifications in terms of functionality. The ETROC2 is intended as a learning chip, as a stepstone to the ETROC3 which is intended as the pre-production design. The ETROC2 design and test results will be presented.

**Summary (500 words):**

The ETROC2 is the first full size (16x16) and full functionality prototype design and its dimension is 21mm x 23mm making it one of the largest chips in HEP. The analog front-end design (preamp, discriminator and TDC) for each pixel is based on the ETROC1 pixel design, while the pixel readout and global readout design is entirely new with a switch-cell based network approach. The bump bonded ETROC1 chips (with LGAD sensors) have encountered a noise originated from its own 40MHz readout clock and coupled via the bump bonded sensor into the preamplifier input. One of the main focuses of the ETROC2 design is to minimize this digital noise in order to reach low enough discriminator threshold to achieve the timing performance when LGAD gain is reduced due to irradiation towards the end of life at HL-LHC. The clock distribution is also based on the ETROC1 4x4 H-tree design, scaled up to 16x16 with a new shielding structure added to alleviate potential interference. The ETROC2 PLL is migrated from the clock generator block from lpGBT with metal stack change and some new blocks for calibration. A few new features have been added to the ETROC2, including a waveform sampler for the preamplifier output for one of the pixels for monitoring purpose, the on-chip and in-pixel auto discriminator threshold calibration, built-in self-testing capability with digital pattern generation within each pixel, as well as the capability to provide a coarse map of delayed hits continuously for every bunch crossing for monitoring or Level 1 triggering purposes. To minimize the risk from ETROC1 to ETROC2, a few dedicated testing chips were designed and carefully tested, including the rad-hard version of the waveform sampler chip, the ETROC-PLL chip which is based on the lpGBT PLL, and special I2C testing chip. In addition, the new pixel and global readout has been emulated in FPGA for design verification and testing purposes. The ETROC2 emulator has been tested with the rest of the system before the ETROC2 submission and has been used extensively for the preparation of the ETROC2 chip level testing as well as system level testing. In this presentation, the main ETROC2 design features along with the testing results will be summarized, followed by lessons learned from ETROC2 design, fabrication and testing experiences to guide the ETROC3 design.

Tuesday posters session / 227

## GaN based DC-DC converters for high energy physics applications

**Authors:** Alvaro Pradas Luengo<sup>1</sup>; Guillermo Plumed Asensio<sup>1</sup>

**Co-authors:** Alberto Arcusa Puente<sup>1</sup>; Claudio Rivetta<sup>2</sup>; Fernando Jose Artech Gonzalez<sup>1</sup>; Ivan Echeverria Ciaurri<sup>1</sup>; Javier Galindo Guarch<sup>1</sup>; Mateo Iglesias Amella<sup>1</sup>

<sup>1</sup> *Aragon Institute of Technology Itainnova (ES)*

<sup>2</sup> *SLAC National Accelerator Laboratory-Unknown-Unknown*

**Corresponding Authors:** alvaro.pradas.luengo@cern.ch, gplumed@itainnova.es

This paper introduces a prototype of a GaN FET based 200 W DC-DC converter. Its design has been carried out to ensure optimal efficiency and minimal electromagnetic interference (EMI) issues that are commonly associated with the high switching frequency converters. To achieve this, hardware-in-the-loop (HIL) techniques have been used to enhance the control at high switching speed, and ANSYS HFSS-SiWave models have been developed to assess noise emissions based on the parasitic elements of PCB layout. Prototypes performance have been evaluated through extensive testing. This work offers insight into the potential of this technology in future physics detectors.

### Summary (500 words):

In recent years, the industry has identified GaN transistors as a pioneering technology to enhance high-density power modules that can augment efficiency, reduce weight, and shrink in size. The ECFA DRD roadmap has also recognized this technology as a promising candidate for overcoming limitations imposed by the higher power densities required for future physics detectors. Specifically, DRD7 of the ECFA roadmap has highlighted the importance of identifying synergies with the industry to assess and tailor this emerging technology to meet the requirements of physics detectors. The Advanced Electrical Technologies division at ITAINNOVA has spent the last years developing power converters based on GaN transistors for both the automobile industry and physics detectors. One such project, GANCaP4CMS, has been dedicated to the design of a DC-DC utilizing GaN transistors for physics detectors.

This paper describes the development and testing of a GaN-based DC-DC power converter prototype intended for high-energy physics detectors. The converter delivers 200W output power and operates within a 12V to 24V input voltage range at a maximum switching frequency of 2MHz. It is a current source capable of providing 10A output for serial power testing applications. The primary objective of this prototype is to validate the technology for high-energy physics environments where high power density and radiation tolerance are critical.

The design of the converter comprises three main stages, which will be presented in this paper. The first stage involves using a simplified simulation model of the power elements and control loop to dimension and choose the main components based on the application requirements. The second stage involves programming and testing the control loop of the system on a Hardware in the Loop (HIL) platform using a microcontroller while running a real-time simulation of the power converter. This approach ensures reliable and stable control while implementing advanced techniques to reduce noise emissions. The third and final stage involves high-frequency simulations using both Spice-based software (Cadence Orcad) and finite element models (ANSYS) to optimize the layout of the gate drivers and power stages, and better understand the effects of parasitic elements of PCB design on robustness and potential EMI issues. This stage also enables fine-tuning of drivers' components, snubber circuits, and input/output filter design.

During prototype testing, the performance of the converter, efficiency, stability, step response, and current ripple, has been measured for all the range of input voltage and loads, and different switching frequencies. The switching behavior of the converter has been also characterized using different dead-times and driving circuitry configuration to validate and improve the high frequency simulation models.

Future work based on this paper includes full design optimization to maximize the converter power density, using integrated power GaN modules (modules that integrate drivers and transistors) and planar inductors. Also, higher voltage and power prototypes will be developed and studied for integration optimization purposes.



**Module, PCB and Component Design / 228****Design, production and irradiation results of the new advanced front end electronics of CMS iRPC****Author:** Maxime Gouzevitch<sup>1</sup><sup>1</sup> *Centre National de la Recherche Scientifique (FR)***Corresponding Author:** maxime.gouzevitch@cern.ch

New advanced front end electronics are designed for the improved RPCs of CMS experiment for data taking during HL-LHC era. This electronics is developed to read out the RPC detectors from both ends of a signal strip, using a new ASIC, iRPCROC, which triggers the Cyclone V FPGA to record the timing information, allowing the correct identification of the position along it. The on-chamber results of the test beams and commissioning at CMS with focus on performance of the electronics will be presented.

**Summary (500 words):**

New advanced front-end electronics are designed for the new improved RPCs of CMS experiments for data taking during the HL-LHC era. During the High Luminosity CERN LHC (HL-LHC) operation phase, the instantaneous luminosity will be increased to  $5 - 7.5 \times 10^{24} / \text{cm}^2 / \text{s}$ , a factor 5–7.5 above the LHC design value.

The front-end electronics (FEBv2) is designed to read out the RPC signals from 2 ends of a strip and determine the hit position along the strip with high precision and the absolute hit timing. The analog RPC signal first enters the iRPCROC, a new ASIC from the PETIROC family. There it is pre-amplified, and the rising edge is discriminated at GHz frequency. This version of the ASIC includes features drastically reducing the cross-talk between channels as well as the retriggering effects. Finally, the resulting digital signal is time-stamped by a delay-line Time-Digital-Converter (TDC) implemented into the Cyclone V INTEL FPGA.

In the first step, we describe the schematic of the FEB. We will discuss the main features of the design, which reduce the noise, cross-talk, retriggering, and grounding scheme.

The second step will present the calibration, synchronization, and measurement of the time resolution. It is as low as 30 ps, well below the time resolution effects from the RPC chamber. We describe how we calibrated and estimated the charge sensitivity of the FEB and how we determined the optimal working point. The FEB can be operated with a threshold of 30 fC, with negligible noise. This threshold can be lowered if needed down to 20 fC.

In the third step, we will describe the peculiarities of the FEB operation in the hard radiation background characteristic of the HL-LHC phase. We developed a radiation-tolerant firmware which we will describe. The FEB underwent multiple certification sessions for the total integration dose and for the Single Event Upsets and Single Event Latch-Up in gamma, neutron, and mixed field (thermal neutrons ThN, high energy neutrons, and hadrons - HEH) facilities in ENEA, Italy, and at CERN.

No cumulative effects in the FEB operation were observed after irradiation with the mixed field in the CHARM facility. The total integrated dose was 60 Gy and fluences  $1.6 \times 10^{11} \text{ HeH/cm}^2$ ,  $3.3 \times 10^{11} \text{ ThN/cm}^2$ . In the neutron irradiation facility FNG in ENEA, Frascati, we pushed the high energy neutron flux up to  $25 \times 10^{11} \text{ neq1MeV/cm}^2$  concentrated on 1 of the Petiroc2B. No degradation was observed either.

In the CHARM facility, it was demonstrated that in the HL-LHC conditions, with an expected flux of  $5000 \text{ HEH/s/cm}^2$ , including safety factor 3, an SEU would occur 1-2 times per day, and an SEL once one year. The SEL protection system was proven to work well. Furthermore, the SEU recovery time does not exceed 20 s.

**Invited / 232****Accelerators overview, outlook, differences, why do we need the**

## **different concepts, FCC/e<sup>+</sup>-/muon..., impact on detector R&D and electronics**

**Corresponding Author:** dave.newbold@cern.ch

**Invited / 233**

## **Advancing fusion energy: Meeting the challenges of diagnostics and electronics for the ITER project**

**Author:** Raphael Tieulent<sup>None</sup>

**Corresponding Author:** raphael.tieulent@iter.org

In the pursuit of clean and sustainable energy, the International Thermonuclear Experimental Reactor (ITER) project has emerged as a beacon of hope. As the world's largest experimental fusion reactor, ITER aims to demonstrate the feasibility of fusion as a viable energy source. However, operating in a challenging nuclear environment presents numerous technical and engineering obstacles that must be overcome to ensure safe and reliable operation.

The diagnostic systems are critical to the successful and safe operation of ITER. They provide the means to observe, monitor and maintain plasma performance over extended periods of time. They provide accurate measurements of plasma behaviour and performance, including those required for protection of the machine and its control, as well as measurements required for physics studies. In total, about 50 diagnostic systems will be installed on ITER.

This presentation focuses on the development of diagnostics systems and the utilization of electronics within the ITER project. The harsh environment, characterized by high temperatures, intense neutron fluxes, and strong magnetic fields, poses significant challenges for electronics and instrumentation.

The first part of the presentation discusses the design and development of diagnostic systems for ITER. These systems encompass a wide range of measurements, including plasma temperature, density, and impurity content.

The second part of the presentation delves into the unique requirements and challenges associated with electronics used in the nuclear environment of ITER. The radiation effects, including total ionizing dose, displacement damage, and single-event effects, pose serious reliability concerns for electronic components. Radiation-hardened designs, materials, and techniques are discussed, along with strategies for mitigating radiation-induced failures and ensuring the longevity of electronic systems. Finally, this presentation provides an overview of the research and development efforts underway in the field of diagnostics and electronics as part of the ITER project. By addressing the technical challenges and presenting the progress made, it aims to encourage the exchange of knowledge, collaboration and innovation in the field of electronics for nuclear fusion. The knowledge gained from this research will not only contribute to the success of ITER, but will also pave the way for future advances in fusion energy technologies.

**Disclaimer:** The views and opinions expressed herein do not necessarily reflect those of the ITER Organization

**Link Users Group / 235**

## **Introduction**

**Corresponding Author:** francois.vasey@cern.ch

Link Users Group / 236

## **lpGBT calibration**

Corresponding Author: stefan.biereigel@cern.ch

Link Users Group / 237

## **VTRx+ production ramp up challenges and status**

Corresponding Author: csaba.soos@cern.ch

Link Users Group / 238

## **VL+ optical fibre plant preproduction status and production plans**

Corresponding Author: stefano.meroli@cern.ch

Link Users Group / 239

## **The Design and Packaging Challenges of a High Density 25G Optical Engine**

Welcome / 240

## **Opening**

Corresponding Author: alexander.kluge@cern.ch

Welcome / 241

## **Introduction**

Corresponding Author: alessandro.cardini@cern.ch

Welcome / 242

## **The search for gravitational waves from LIGO/Virgo/KAGRA detectors to Einstein Telescope: recent results and new frontiers of gravitational wave instruments and astronomy**

**Corresponding Author:** alberto.masoni@ca.infn.it

Einstein Telescope is the future European Laboratory for gravitational waves. The discovery of gravitational waves (GW), in 2015, 100 years after the publication of Einstein's general theory of relativity, was soon followed, in 2017, by the assignment of the Nobel prize for physics to three scientists of the LIGO-VIRGO collaboration. LIGO in the USA and VIRGO in Italy are, at present, the unique detectors worldwide capable to observe the GW signals. In 2017 with a coordinated effort of LIGO-VIRGO and a network of Telescopes on earth and in the space the gravitational waves signal from a neutron star collision was detected and combined with its electromagnetic counterpart, opening the era of multi messenger astronomy.

This provided the substantial momentum which led to the proposal of a third generation GW detector in Europe. In July 2021 Einstein Telescope was officially approved and inserted in the ESFRI program. The detector will substantially improve the current ones in sensitivity and in background suppression. In the present configuration it is designed as a triangle, underground, of 10 km per side, but a twin L shape system, with same concept of the LIGO detector is under consideration, There are presently two site candidates, one in Italy, in Sardinia, and one in the Netherlands, in the Limburg region.

This presentation will cover both the genesis of the project and the principles of GW detection, its technological challenges and an overview of the present status and future schedule.

**Welcome / 243**

## **Sardinia cultural heritage: the nuraghi and nuragic civilization**

Sardinia has an age old history told by a great cultural heritage and the nuraghi are probably the most important archaeological and cultural evidence. These majestic stone towers, built in the second millennium B.C., have represented a long term landscape marker and a symbolic reference point for Sardinian communities. Extraordinary ancient architects designed and built at least 7000 monumental buildings all over the island, big stone towers that were symble and centre of life of a great civilization. Sardinia territory still preserves many other archaeological evidences of this great people life, such as monumental tombs (giant's tombs), temples as sacred wells, sanctuaries, villages and an important bronze artifact production (axes, swords, figurines, ecc.). Nuragic people controlled the whole island from North to South, but were also involved in the main sea routes and traffics of the Mediterranean sea. Nuragic finds in Cyprus, Crete, Sicily, Spain, Northern Africa show us the important role of this civilization in the Mediterranean Bronze and Iron age trades and networks.

**Micro electronics Users Group / 244**

## **Welcome**

**Author:** Kostas Kloukinas<sup>1</sup>

<sup>1</sup> CERN

**Corresponding Author:** kostas.kloukinas@cern.ch

**Micro electronics Users Group / 245**

## **EUROPRACTICE IC services and foundry news**

**Corresponding Author:** paul.malisse@imec.be

**Micro electronics Users Group / 246**

## **EUROPRACTICE EDA tools for the HEP community**

**Corresponding Author:** mark.willoughby@stfc.ac.uk

**Summary (500 words):**

**Micro electronics Users Group / 247**

## **CERN ASIC support and Foundry services news**

**Corresponding Author:** alessandro.caratelli@cern.ch

**Summary (500 words):**

**Micro electronics Users Group / 248**

## **Open discussion**

**Summary (500 words):**

**FPGA Users Group / 249**

## **Experience with RFSoc for Beam Instrumentation applications**

**Corresponding Author:** andrea.boccardi@cern.ch

**FPGA Users Group / 250**

## **RFSoc used as a readout for Magnetic Microcalorimeters**

**Corresponding Authors:** le8a9p@gmail.com, luis.ardila@kit.edu

**FPGA Users Group / 251**

**TBC**

**FPGA Users Group / 252**

**Discussion**

**Welcome / 253**

**Associazione "Sardegna verso l'UNESCO"**