Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

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1 Abstract

During the next Long Shutdown (LS3) of the LHC, the innermost three layers of the ALICE Inner Tracking System will be replaced by a new vertex detector composed of curved ultra-thin monolithic silicon sensors. The R&D initiative on monolithic sensors of the CERN Experimental Physics Department, in synergy with ALICE ITS3 upgrade project, prepared the first submission of chip designs in the TPSCo 65 nm technology, called MLR1 (Multi Layer per Reticle). It contains four different test structures: CE-65, DPTS, APTS-SF and APTS-OPAMP, with different process splits and pixel designs. This work illustrates the validation of the technology in terms of pixel performance and radiation hardness.

2 Summary

Monolithic Active Pixel Sensors (MAPS) embed integrated front-end electronics in the same silicon volume that constitutes the sensing substrate. A new vertex detector composed of curved, ≤ 50 μm thin monolithic silicon sensors will be installed during the LHC LS3 to replace the innermost three layers of the ALICE Inner Tracking System at CERN.

In particular, the MLR1 submission foresees to validate the Tower Partner Semiconductor Co. 65 nm ISC technology, in which the same principles of process optimization as in 180 nm technology have been applied. Three main pixel designs have been implemented: standard, modified (B) and modified with gap (P). In particular, the P-type combines the advantages of a small collection electrode, as a few fF sensor capacitance, with a fully depleted epitaxial layer, thanks to a low dose deep n-type implant, placed below the wells containing the circuitry. Four different pixel test structures, all measuring 1.5 mm by 1.5 mm were designed to validate the sensor technology: Circuit Exploratoire 65 (CE65), consisting of $64\times32/48\times32$ matrices featuring pixel pitches of 15 and 25 μm respectively, Digital Pixel Test Structure (DPTS), a matrix of 32×32 pixels with 15 μm pitch, including a full digital front-end within each pixel, Analogue

Pixel Test Structure - Source Follower (APTS-SF) and Analogue Pixel Test Structure - Operational Amplifier (APTS-OPAMP). The APTS consists of a 6×6 pixel matrix, of which only the central 4×4 pixels are read out. It features two types of output buffers: source follower or a high speed Operational Amplifier (OPAMP), the latter providing a better timing performance. The pixel pitches range from 10 to 25 μm.

In this talk, the main results of the test structures characterisation from the MLR1 submission will be presented. In particular, testbeam results on the CE-65 have shown that, as expected, in the modified process all the charge is mostly collected by a single pixel. Subsequently, the effect of different irradiation levels on the DPTS chip detection efficiency, on the sensor spatial resolution and average cluster size will be illustrated. In-beam measurements have demonstrated the 99% detection efficiency for a chip irradiated up to 10^{15} 1 MeV n_{eq} cm^{-2} and 100 kGy at 20 °C, while preserving a low fake-hit rate of < 10 $pixel^{-1}$ s^{-1}, thus reaching the goals of detection efficiency and non-ionising and ionising radiation hardness up to the expected levels for ALICE ITS3, below 1×10^{13} 1 MeV n_{eq} cm^{-2} (NIEL) and 10 kGy (TID).

Finally, the major results obtained on the OPAMP test structure will be explored: an intensive characterization with a ^{55}Fe source has demonstrated promising performance in terms of charge collection for the optimized sensor, with suppression of slow events with respect to the standard one and from the testbeam, a time resolution of 77 $\pm$ 5 ps has been measured. To conclude, the characterisation of the test structures from the MLR1 submission has been carried out in various laboratories and testbeam facilities and has revealed the excellent performance of the R&D campaign.