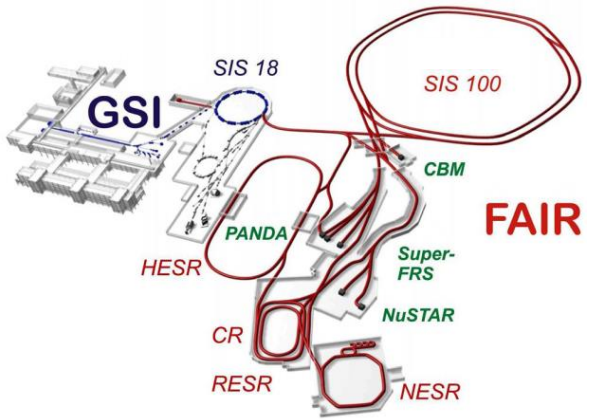
Digital on Top methodology for MAPS

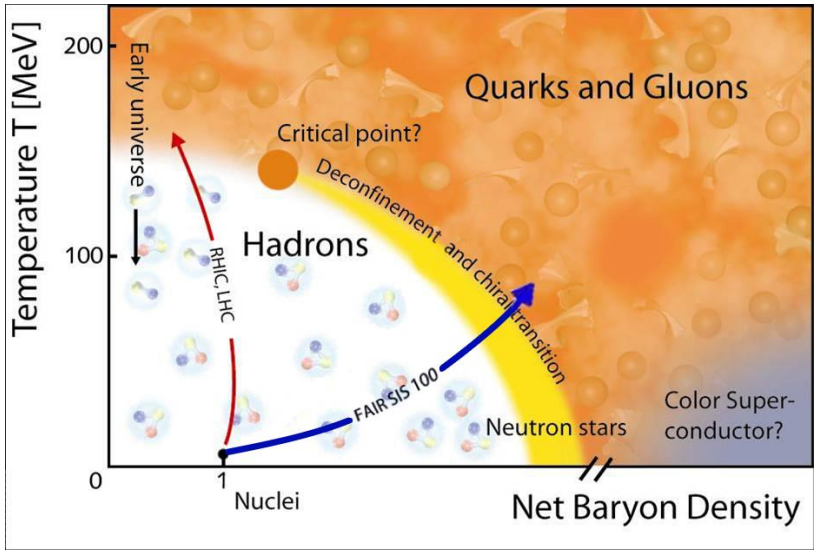
Feedback from MIMOSIS sensors for CBM Micro-Vertex Detector

What about CBM and MIMOSIS?

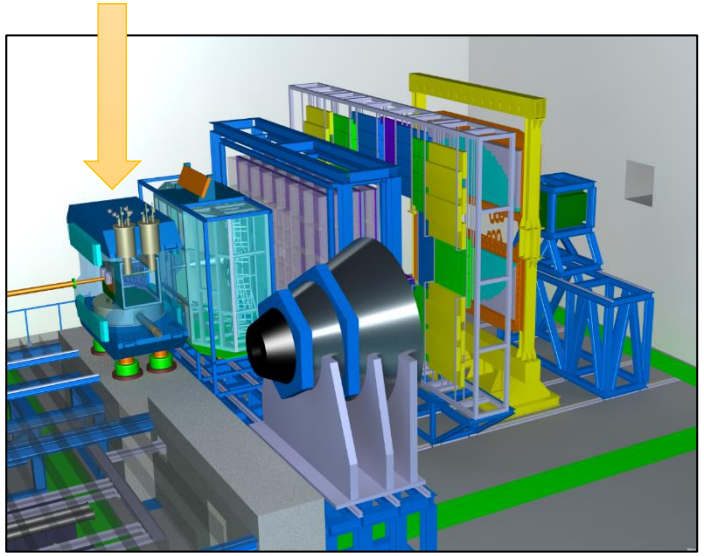
The Compressed Baryonic Matter experiment @ FAIR

- Explore phase diagram at region of highest net-baryon density
- Fix target
- Beam start is schedule for 2028





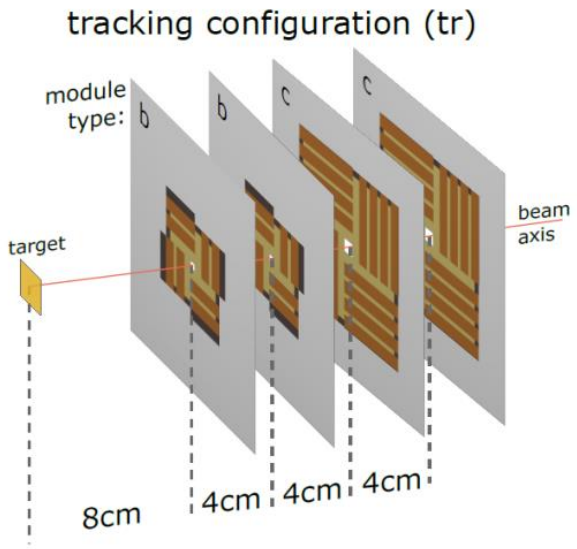
MVD+STS

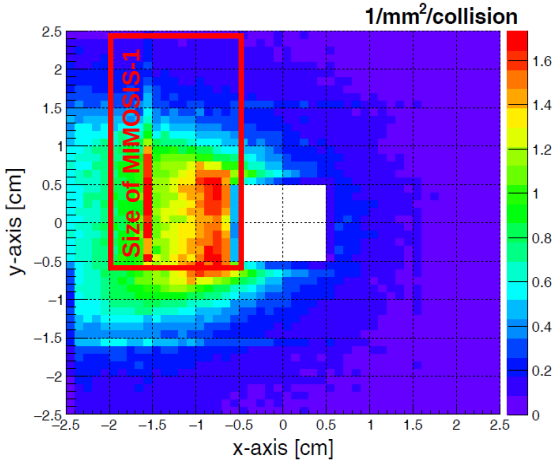


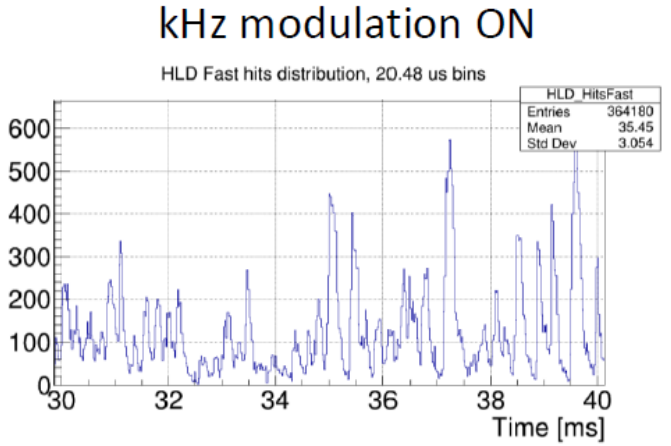
April 2023

Micro Vertex Detector

- Aim for high collision rate capability
  - 100 kHz Au+Au @ 11 AGeV
  - 10 GHz p+Au @ 30 AGeV
- Aim to contribute to tracking
  - 4 planar detector stations
- Aim for good sec. vertex resolution
  - Operate in target vacuum
  - First station 5 cm from target (in vertexing configuration)
  - ~ 5 µm resolution
  - Thin stations
    - ~ 0.3 % X_0 (first station)
    - ~ 0.5 % X_0 (other stations)
- **Sensor must handle occupancy gradients in space**
- **Sensor must handle beam fluctuations in time**

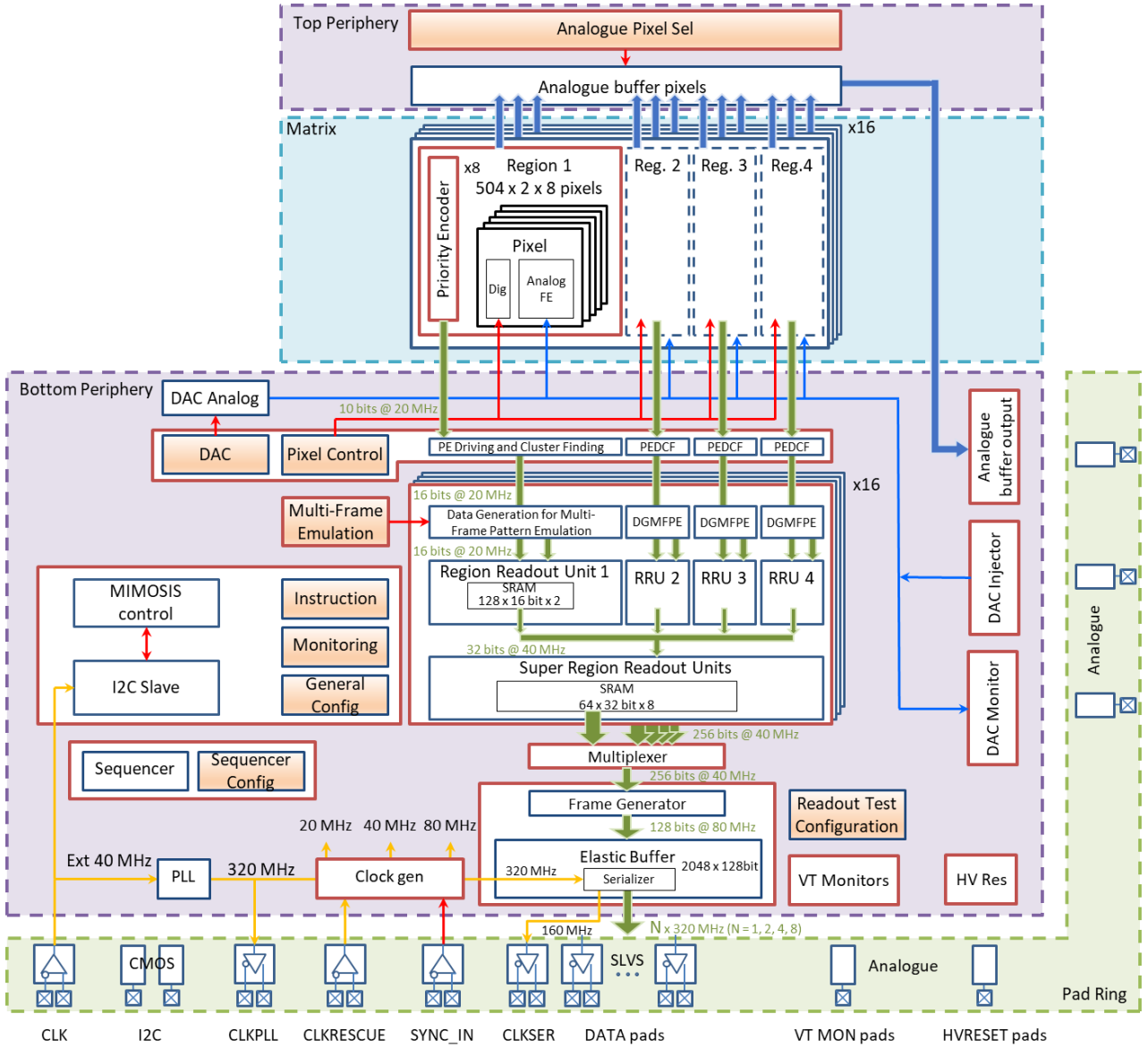






MIMOSIS diagram

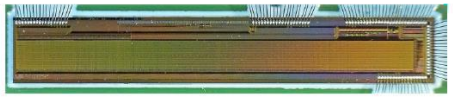
- Based on ALPIDE architecture
  - **New readout** to sustain space and time variations
  - Matrix dimension: 1024 col. X 504 row
  - Pixel dimension: 26.88 µm (height) x 30.24 µm (width)
  - Integration time: 5 µs
  - Tower Semiconductor 180 nm with modified process
- 3 steps prototyping for full scale:
  - MIMOSIS-0 small scale prototype (2017)
  - MIMOSIS-1 first full scale prototype (2020)
  - MIMOSIS-2 final prototype (2022-2023)
  - MIMOSIS-3 pre-production run (end of 2024)
- **MIMOSIS-1 fulfils the requirements of CBM**



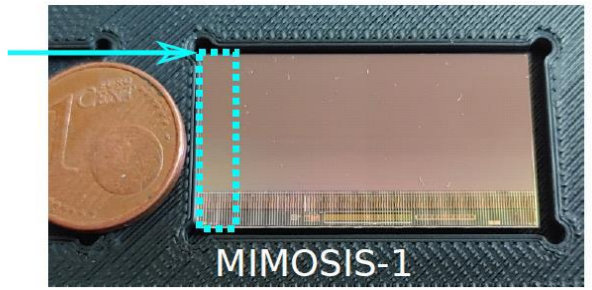
Digital on Top Howto

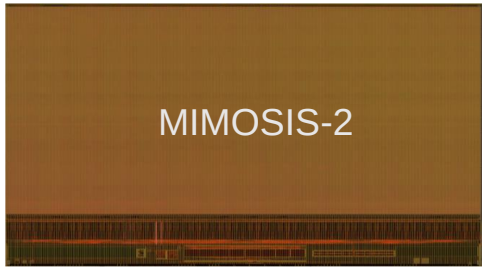
Digital flow evolution with MIMOSIS chips

- My definition of DoT:
  - The use of **digital tools** (Innovus, Tempus, Voltus) to design the top view of the chip
  - The digital tools are **timing driven** ➔ different concepts compare to analogue tools (Virtuoso)
  - The digital tools are made to deals with **large and complex chips**
    - Works on abstraction of cells/blocks ➔ runtime and memory efficient
    - Highly scriptable ➔ easy to modify and respin
- MIMOSIS-0, top in schematic
  - First Digital on Top chip at C4PI ➔ **in prevision of full scale sensors**
  - Mixture between Virtuoso and Innovus ➔ **need to fight with tools**
- MIMOSIS-1, top in verilog
  - Limit Virtuoso on pure analogue cells ➔ **simplify the use of Liberate AMS**
  - No full flat timing verification ➔ **partial verification of the matrix**
- MIMOSIS-2, top in verilog
  - New flow based on Flowkit methodology ➔ **better flow, better reporting, easy to use**
  - Full flat verifications ➔ **timing and power**



MIMOSIS-0



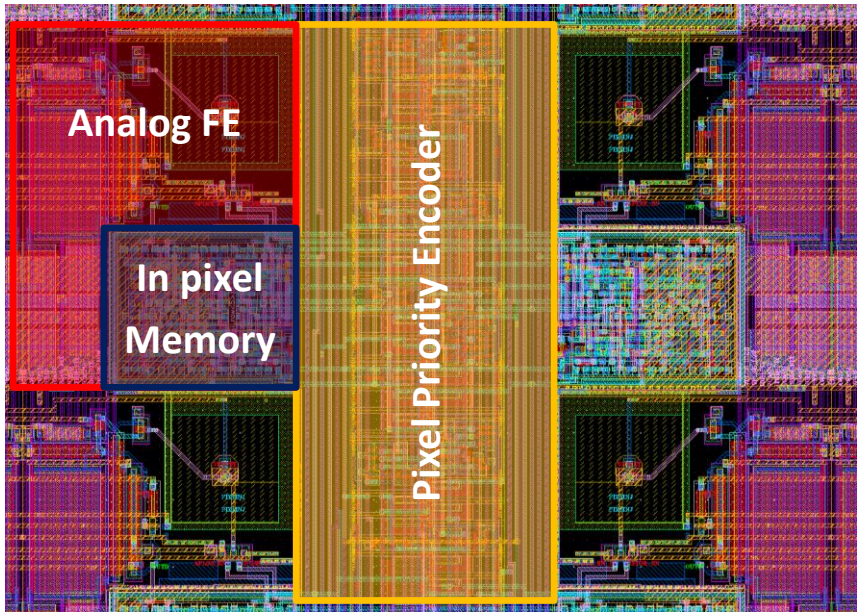


Focus on matrix assembly

- Matrix divided into 64 regions
  - Region is 8 double columns

- Double columns is
  - One priority encoder
  - 1008 Analogue Front-End and In pixel Memory
    - Made with Virtuoso
    - Need an abstract for pin position and antenna ➔ abstract generator
    - Need a liberty file for timing and DRV ➔ **Liberate AMS**

- How it was made in MIMOSIS-1 and MIMOSIS-2
  - Priority encoder made with Innovus
  - Region is assembled with Innovus
    - 8 Priority encoder, 8 x 1008 Analogue FE and In pixel Memory

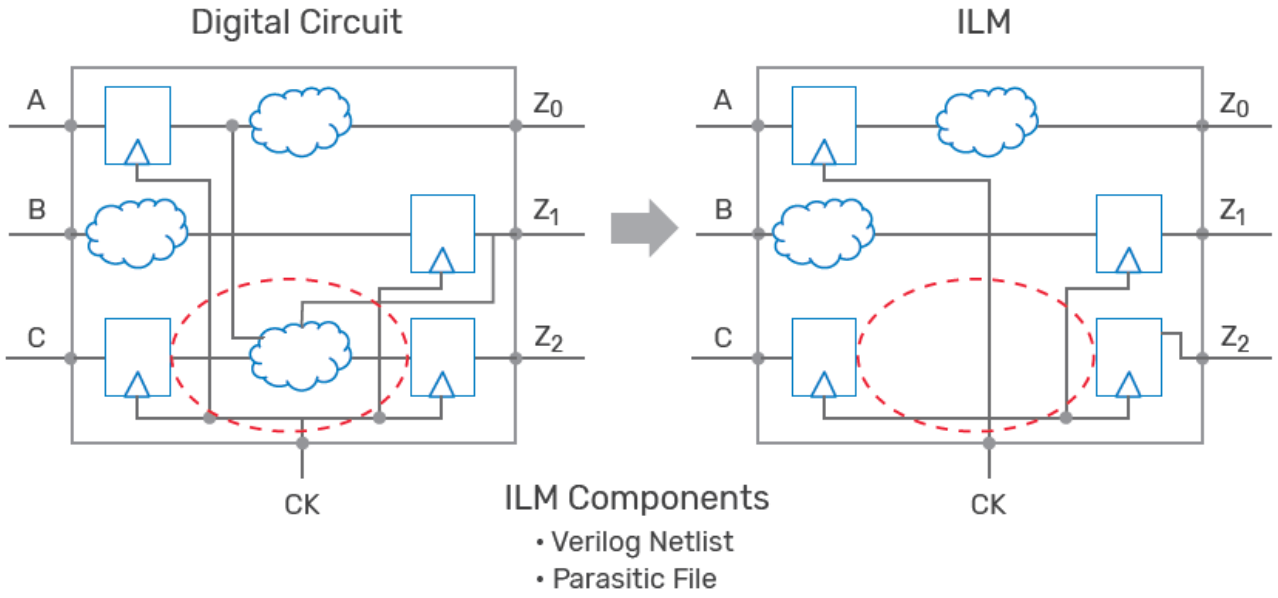


Liberate AMS a needed step

- **Our strategy** with Liberate AMS
  - Lack of experience at the beginning of the project
- Limit Virtuoso on **pure analogue cells**
  - There is no timing constraint on the input of the analogue block
  - There is no digital output
    - At least, limit the number of timing arcs needed from the input to the output
- In that case the Liberate characterization is limited to:
  - **Pins capacitance** on all IO
  - **Drive capabilities** for outputs
    - Slew vs load
    - Fast extraction (only the last buffer is simulated)
- Extract only what you need
  - Need a **close interaction** between digital and analogue **designers**
  - This abstraction keeps **high performances** (few percent, typ. O(ps))

How to handle timing in large chips?

- Need to **model the timing** of digital hierarchical blocks at high level **to reduce the runtime**
  - Needed during optimisation stages
- Interface Logic Model (ILM)
  - Based on **simplification** of the netlist at the interface
  - More accurate timing than ETM (liberty file of blocks)
  - No characterization needed (faster on large blocks)



File Extension	Description
.def	One def file
.v	One netlist file
.place	One Innovus place file
.sdc	One per analysis view
.spef	One per corner
.xtwf	One per analysis view. This file is only available with SI model

Full flat timing verification

- In MIMOSIS-1 the full verification was made after assemble_design
  - All digital blocks and **one pixel region**
  - The command is time consuming and generates large database **(few days)**
- In MIMOSIS-2 use the capability of Tempus and Innovus to load and assemble large design
  - Load for each digital blocks and the top
    - Verilog, spef and optionally def (depending of the analysis)
    - Need **few minutes** on a flat MIMOSIS-2
- Some examples with MIMOSIS-2
  - STA with Tempus DMMMC
    - 4h30 on 4 hosts with 4 cpu each
    - Optimized for memory issue
  - Hierarchical ECO with Tempus without flat pixel array
    - 15 minutes on 8 CPU
  - Rail analysis with Voltus
    - 30 minutes (static)

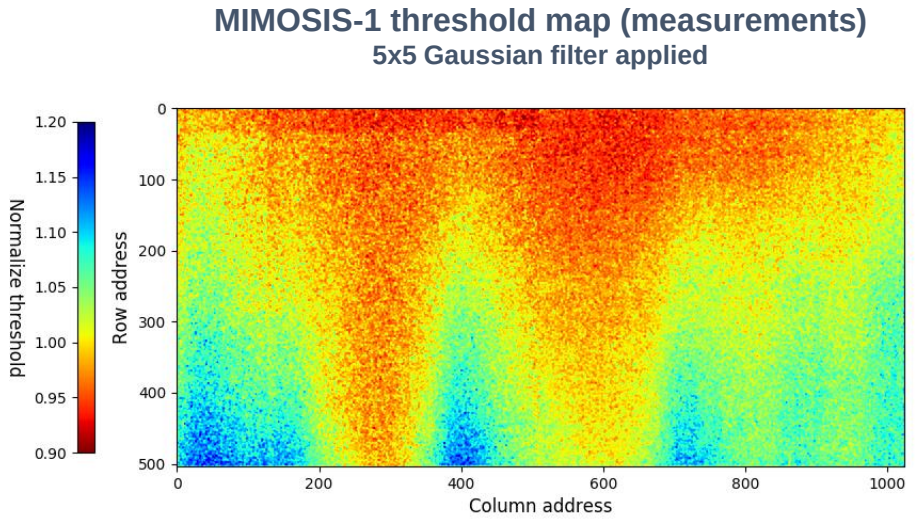
MIMOSIS2 full flat timing analysis

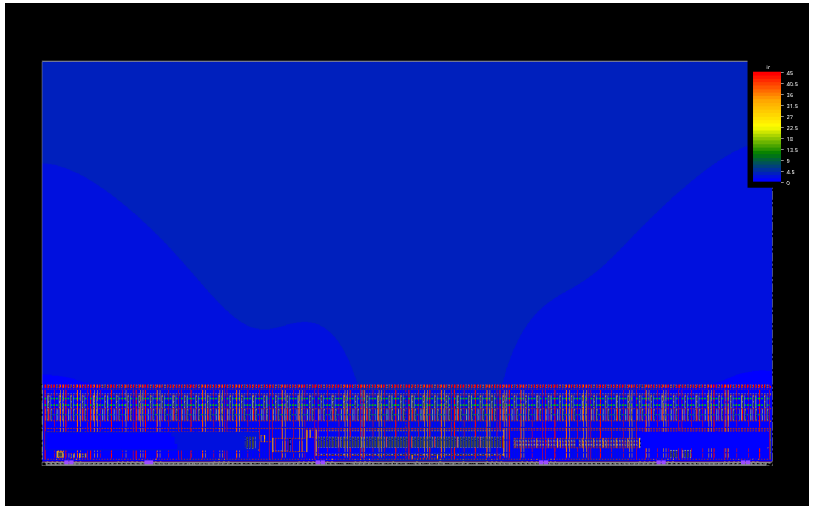
	Local hierarchical (ILM) 1 CPU	Local flat 16 CPU	Distributed flat 4 hosts with 4 CPU
Total Time (h)	0.3	4.2	4.5
CPU Time (h)	0.3	32.75	52
Peak Memory (GB)	20	120	47 for each host

Feedbacks from chips

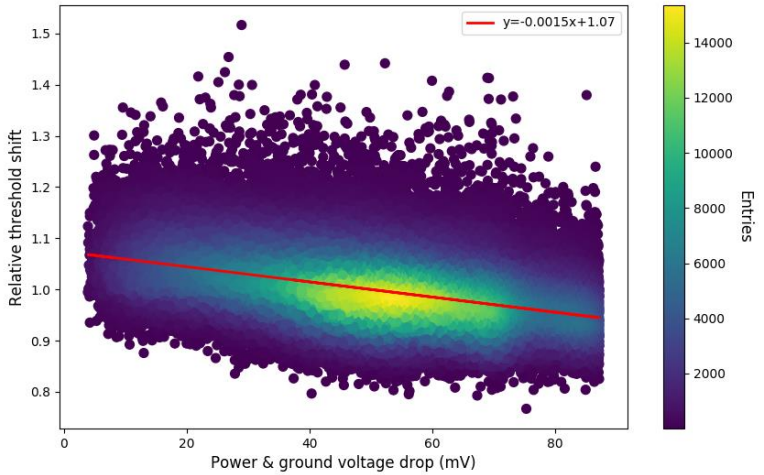
Power grid issue on MIMOSIS-1

- The quality of the power grid is a key factor
  - The uniformity of the power supply and the pixels response are correlated
  - +/- 7 % threshold shift from IR drop
- Need to increase the quality of the power grid of analogue power supply by a factor of 3 to 4

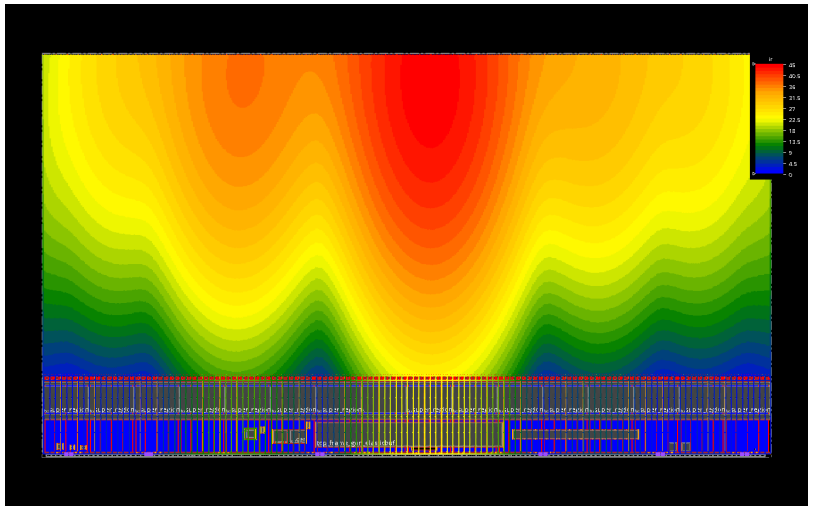




IR drop on AVDD for MIMOSIS-2 (simulations)



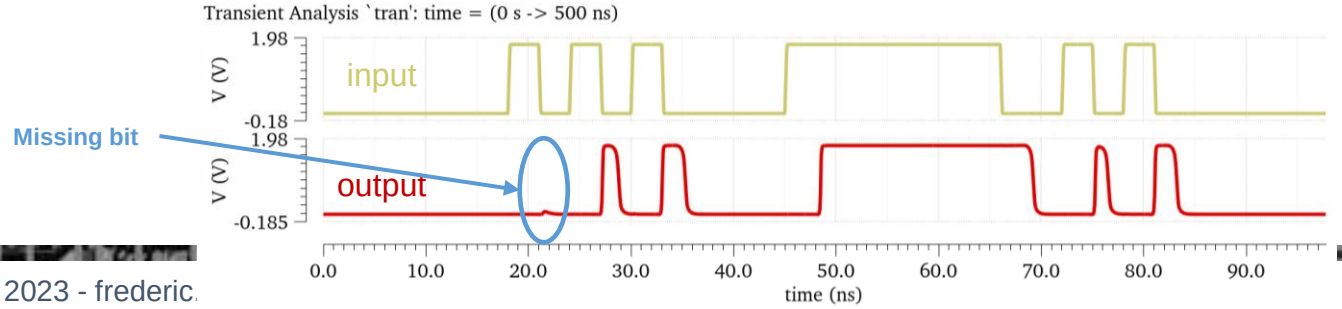
Correlation between IR drop and Threshold shift



IR drop on AVDD for MIMOSIS-1 (simulations)

MIMOSIS-2 bring-up

- Few bugs limit the functionality ➔ **lessons learned**
- Be cautious with analogue nets to avoid buffer insertion during the routing
  - After a discussion with Cadence experts the possibilities are:
    - Set “dont_touch” properties on nets ➔ **What we use**
    - Set “use analog” property in abstract (lef or oa) ➔ **What we use**
    - Set “is_analog” property to true in liberty files (very important for synthesis)
    - Use “set_analog_ports” command in CPF ➔ Checks are available with Conformal Low Power
  - One method is enough but don’t miss a net!
  - Not yet implemented in the flow
- Be cautious with models for post simulations
  - Homemade models
    - It can be hard to be **exhaustive** and accurate in **all conditions** ➔ check conditions with assertions
  - Liberty are timing model files
    - Some effects could not be seen
    - E.g. dynamic effects like bandwidth ➔



Analogue simulations for full chip advanced analysis is now emerging

- New simulators run **analogue simulations** on large-scale chip in **short runtime**
  - APS (~2017), **X (~2020)**, **FX (~2023)**
- Evaluation of Spectre FX, **preliminary results**
  - Conditions:
    - Import Verilog into schematics, blocks per blocks and the top
    - Extract parasitic in DSPF format within Innovus
    - Use a config view to ignore some cells
    - Transient simulation of 12 us (~2 frames)
    - ~1.2 millions of transistors and more than 500k nodes
      - Top + Clock generator + Slow control + Sequencer + Pads + small blocks
  - Still under evaluation on larger scale

Simulator	APS	++APS	X	FX
Total time	~5 h	~17.5 h	~2.3 h	~0.4 h
CPU	16	16	32	16
Memory	~11.5 GB	~11.5 GB	~11.5 GB	~4.9 GB
Preset	-	-	VX	VX
Completion	12% (convergence)	55% (blowup)	100%	100%

100% CPU in VX ➔ functionality
118% CPU in LX ➔ Low Timing, current
145% CPU in MX ➔ High Timing, current
175% CPU in AX ➔ For reference

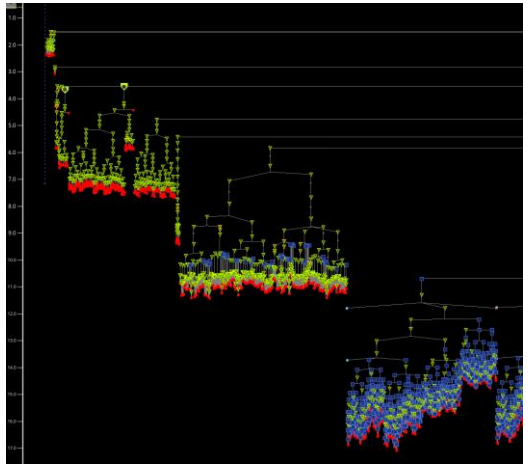
Conclusion

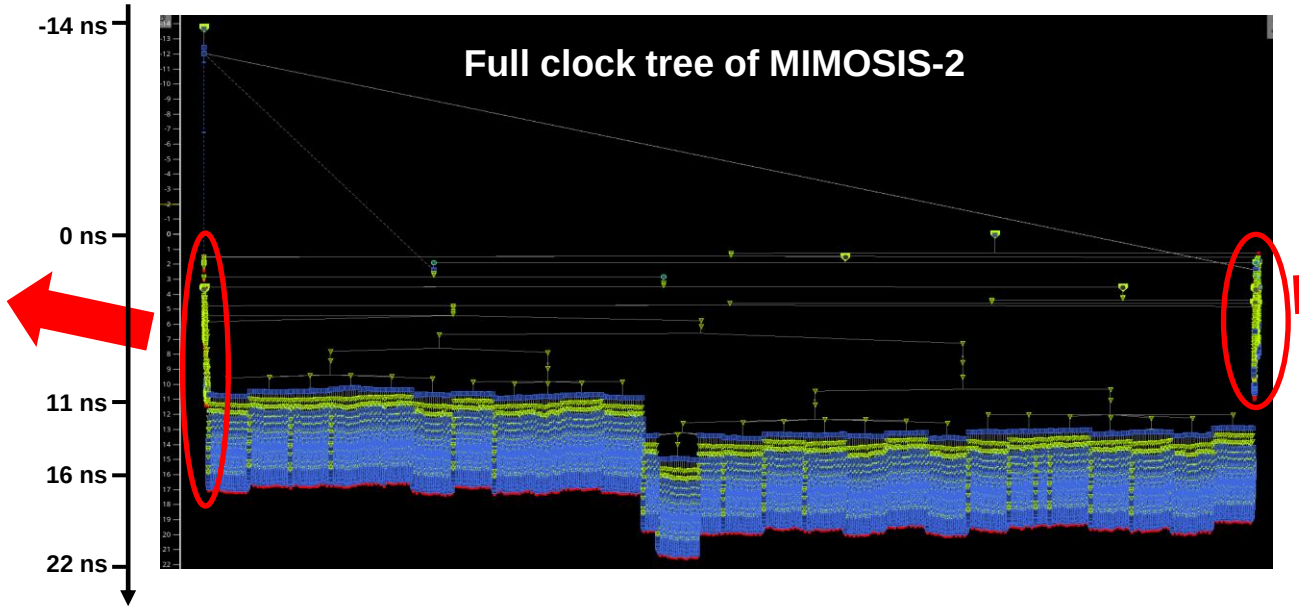
- Digital on Top methodology is suitable for MAPS design down to the pixel
  - Some expertise is needed to avoid pitfalls
- Use as much/far as possible the digital tools
  - There are really effective for such big and complex chip
- But analogue designers are still key to a successful submission
  - Analogue and digital tools are interoperable but not transparent/“plug and play”
  - New analogue simulators enables large-scale chip verification
- Now we are reaching best of both worlds

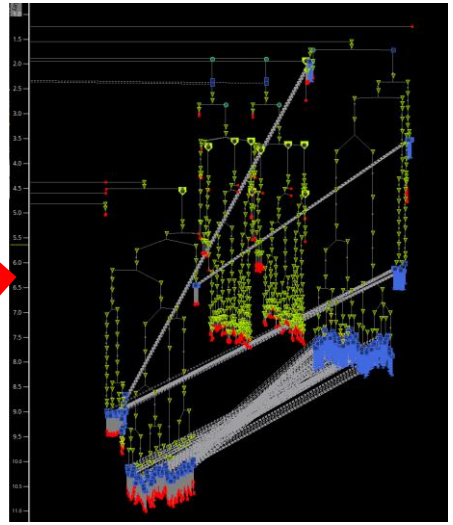
- Keep in mind: verify, verify and verify

Backup

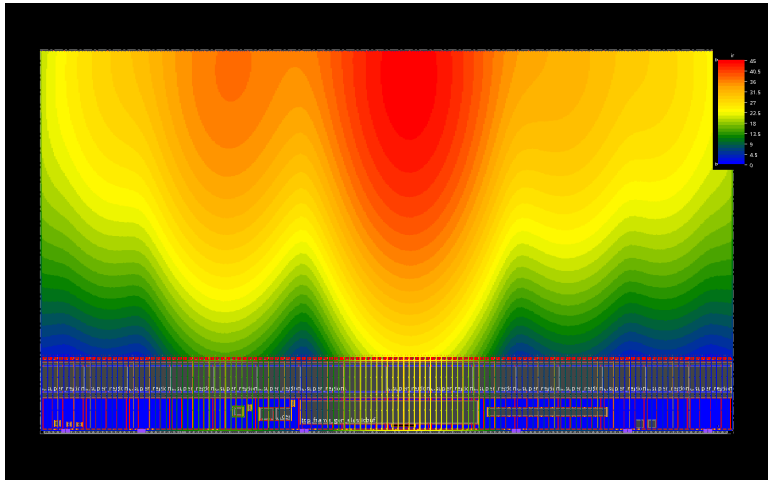
Full flat timing verification: results



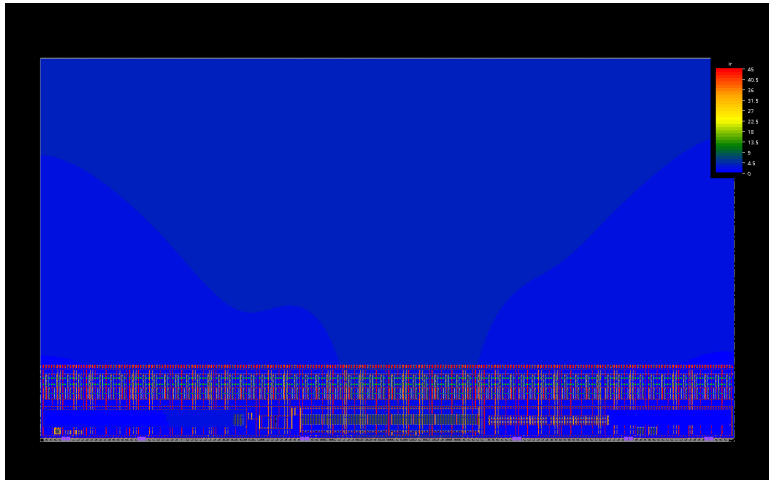




IR drop on AVDD
on MIMOSIS-1
0-45 mV scale



IR drop on AVDD
on MIMOSIS-2
0-45 mV scale



MIMOSIS Requirements

	Requirement
Spatial resolution	~5 µm
Time resolution Triggerless without dead-time	~5 µs
Sensor thickness	~50 µm
Radiation length	~ 0.3 % X_0 (first station) ~ 0.5 % X_0 (other stations)
Power dissipation	<100 - 200 mW/cm²
Operation temperature	- 40°C to +30°C
Temperature gradient on sensor	5 K
Radiation* (non-ionizing)	~ $7x10^{13}$ n_{eq}/cm²
Radiation* (ionizing)	~ 5 Mrad
Radiation gradient on chip	100%
Heavy Ions-tolerance	10 Hz/mm²
Rate (average/50 µs peak)	200/800 kHz/mm²

* No safety factor

Example of trade off: MIMOSIS

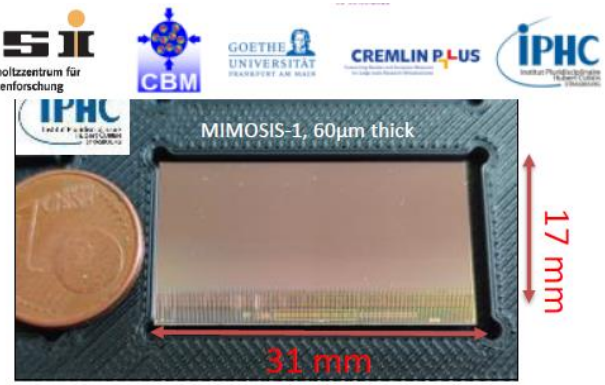
- MIMOSIS-1 chip for CBM-MVD @ FAIR

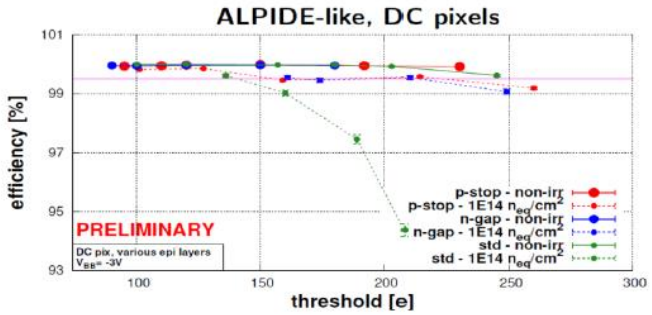
Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	~25 µm
Epi layer resistivity	$> 1 k\Omega cm$
Sensor thickness	60 µm
Pixel size	26.88 µm × 30.24 µm
Matrix size	1024 × 504 (516096 pix)
Matrix area	≈4.2 cm^2
Matrix readout time	5 µs (event driven)
Power consumption	40-70 mW/cm^2

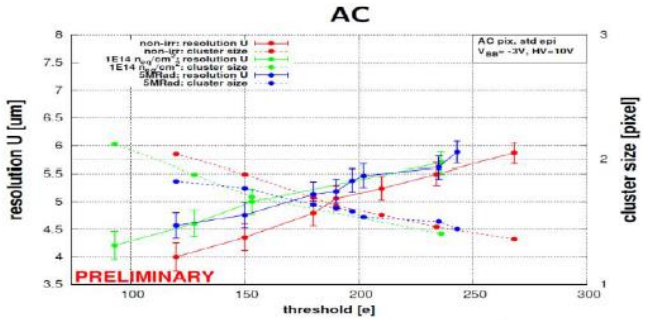
  - ✓ Based on ALPIDE architecture
    - Multiple data concentration steps
    - Elastic output buffer
    - 8 x 320 Mbps links (switchable)
    - Triple redundant electronics
  - ✓ Pixel variants: DC/AC (top bias up to >20V)
  - ✓ Different epitaxial variants tested

Pic from: Munker, Vertex 2019, States of silicon detector R&D at CLIC
Carlos, TREDI 2019, Results of the Malta CMOS pixel detector prototype for the ATLAS Pixel ITK

- Intense test beam campaign (2021-22)
  - ✓ Mimosis-2 submission these weeks
    - Thicker epi layer tests
    - Test prototype for 1 µs readout time







MIMOSIS = a milestone for Higgs factories (5 µm / ≤5 µs)

Courtesy Auguste Besson