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NAPA-P1: NANOSECOND TIMING PIXEL FOR LARGE AREA SENSORS

Tuesday 3 October 2023 18:00 (20 minutes)

NAPA-p1 is a prototype Monolithic Active Pixel Sensor designed in 65 nm CMOS imaging technology, developed to meet requirements for future e+e- colliders. The prototype has dimensions of 1.5 mm × 1.5 mm with a pixel pitch of 25 µm. In nominal conditions, simulations show a pixel jitter of 350 ps-rms and an Equivalent Noise Charge (ENC) of 12 e-rms. The prototype will be characterized this summer, and the results shall be available soon. A discussion will be presented on future strategies to allow the scalability of this design into a large-scale sensor of 10 cm × 10 cm.

Summary (500 words)

The detectors at future e+e- linear colliders will need unprecedented precision on Higgs physics measurements. These ambitious physics goals translate into very challenging detector requirements on tracking and calorimetry. To develop the next generation of ultralight trackers, a further reduction of dead material can be obtained by employing Monolithic Active Pixel Sensor (MAPS) technology.
Future e+e- Colliders require fast detectors with O(ns) timing tagging. This is feasible at the cost of a relatively high-power consumption that could not be compatible with large area constraints. Today some commercial imaging technologies offer the possibility to produce large, stitched sensors (with a rectangle area ˜30 cm × 10 cm). Such large sensors are very interesting from a physics point of view, but they are very challenging from an engineering point of view.
A first MAPS prototype 'NAPA-p1'is designed by SLAC in CMOS Imaging 65 nm technology. The prototype has dimensions of 1.5 mm × 1.5 mm with a pixel pitch of 25 µm. This work benefits from our collaboration with CERN, capitalizing on the improved sensor's performance after a decade of optimizations. This prototype will set the baseline for the sensor and the electronics performance which will serve future developments.
In the pixel, many design choices were motivated by the large-scale compatibility. The pixel is designed with auto-calibration schemes, thus avoiding the distribution of global signal, which would represent a high failure risk. The power consumption is kept to a minimum of 720 nW/pixel, which will be scaled down by a factor or 100 or more for low duty cycle e+e- machines.
Simulations show that to achieve our goal of 1 ns-rms jitter, the sensor capacitance has to be lower than 10 fF, and the Equivalent Noise Charge (ENC) lower than 25 e-rms. The nominal operating conditions correspond to a total current of 600 nA per pixel. In this case, the time resolution is 350 ps-rms and the ENC is 12 e-rms. The prototype chip will be characterized this summer, and the results shall be available for presentation soon. Moreover, a discussion will be presented about the design strategies to allow the scalability of this design into a large-area stitched sensor of 10 cm × 10 cm, with specifications compatible with future e+e- colliders.

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