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3D-integrated pixel circuit for a low power and small pitch SOI sensor

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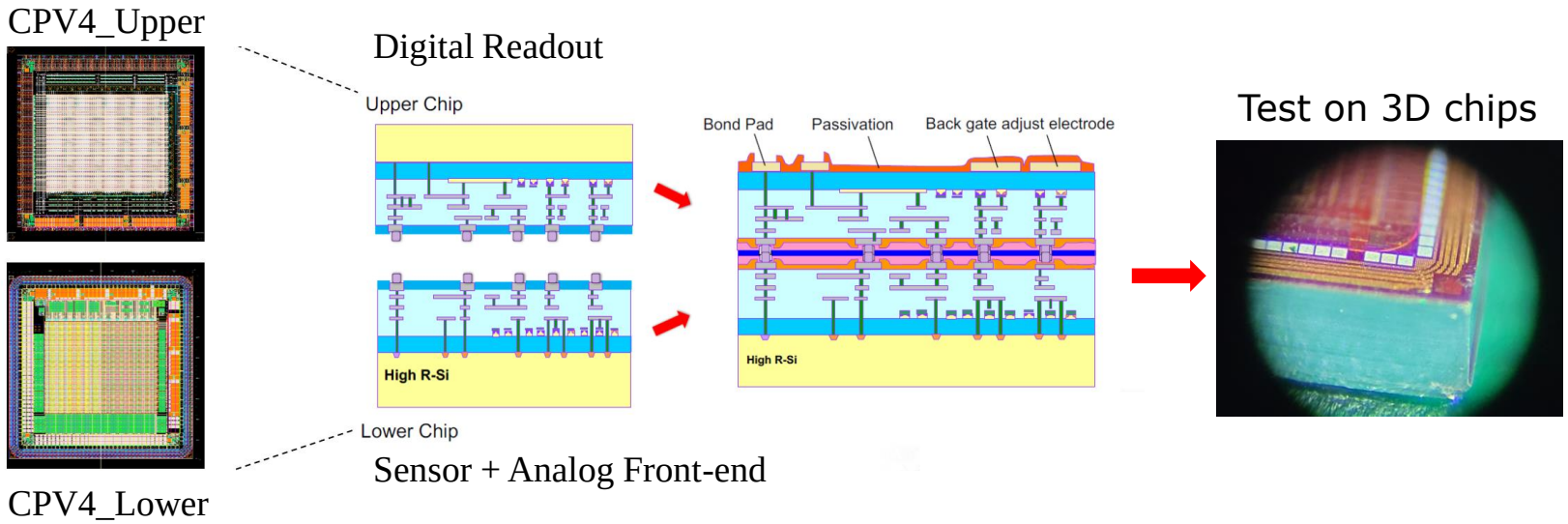
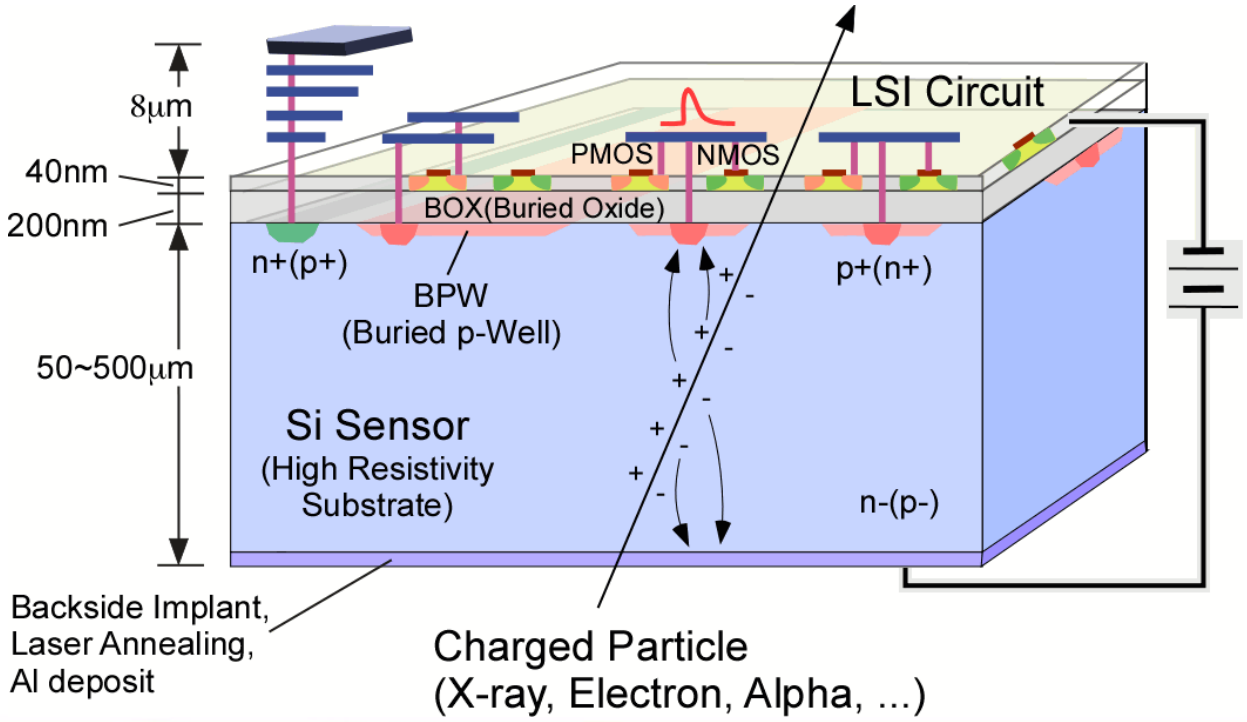
Outline

- Introduction
  - SOI pixel sensor and 3D integration
- Design of the CPV-4 3D chips
  - Sensing diode
  - Analog frontend
  - Digital readout
- Test results
  - Test on the upper tier
  - Test on the lower tier
- Summary and Outlook



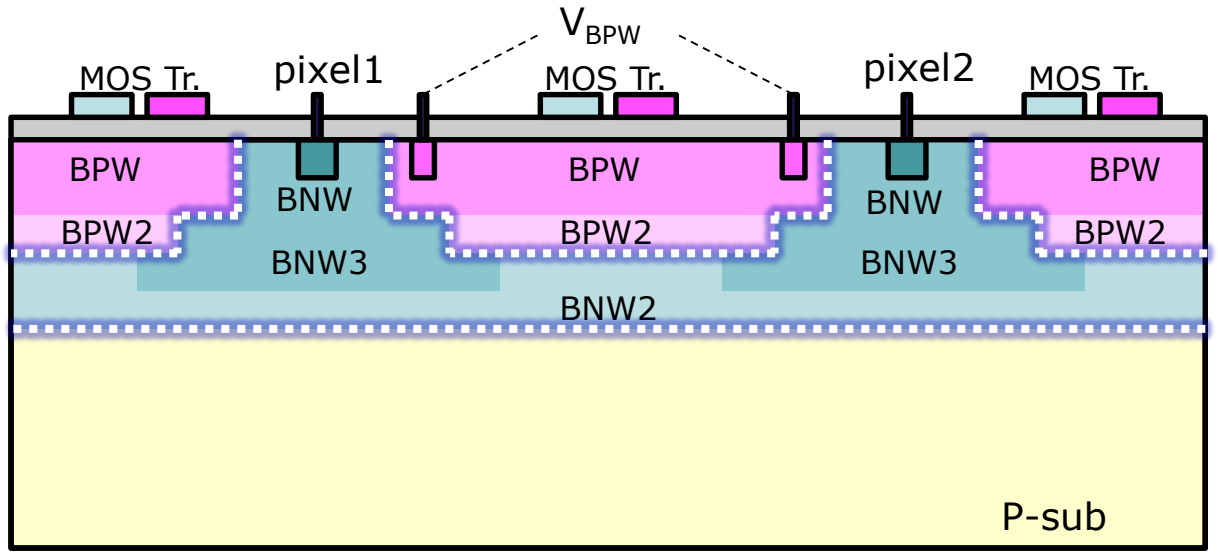
SOI pixel sensor

- Monolithic pixel sensor, based on a 200 nm FD-SOI CMOS process
  - Low leakage low power transistors
  - 1 Poly 5 Metal layers
  - MIM Capacitor (1.5 fF/um^2), DMOS (4 fF/um^2)
  - Core voltage = 1.8 V, IO voltage = 1.8/3.3 V
  - High Resistivity substrate (a few kΩ·cm) to detect charged particles and X-ray photons

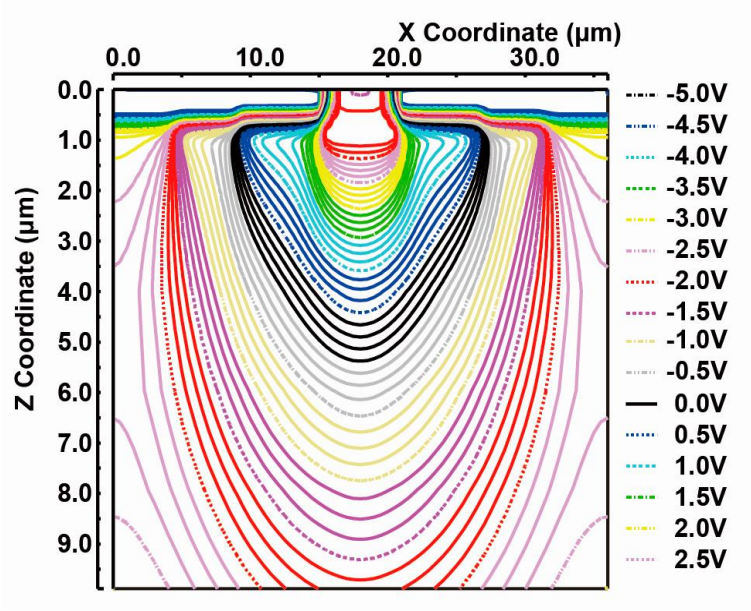


Pinned Depleted Diode (PDD)

- PDD structure consists of multiple sensor layers:
  - Buried N-Wells: BNW, BNW2, BNW3 (**collection electrode**)
  - Buried P-Wells: BPW, BPW2 (**shielding layer**)
  - P-type HR substrate: P-sub (**sensitive volume**)



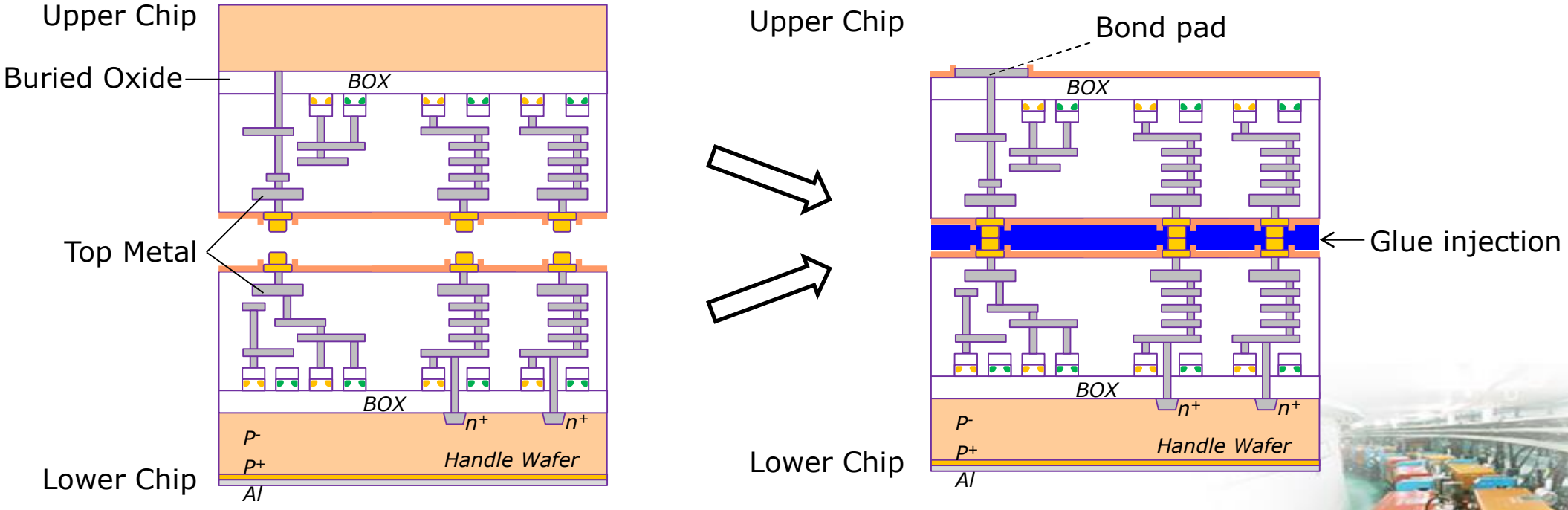
- PDD structure offers
  - Very small **diode capacitance** (a few fF)
  - Depletion volume up to substrate thickness
  - Optimization of lateral electric field
  - Shielding against **electrical coupling**
  - Suppression of **leakage current**



Electric field in PDD structure:
Ref: doi:10.3390/s18010027 by Shoji Kawahito

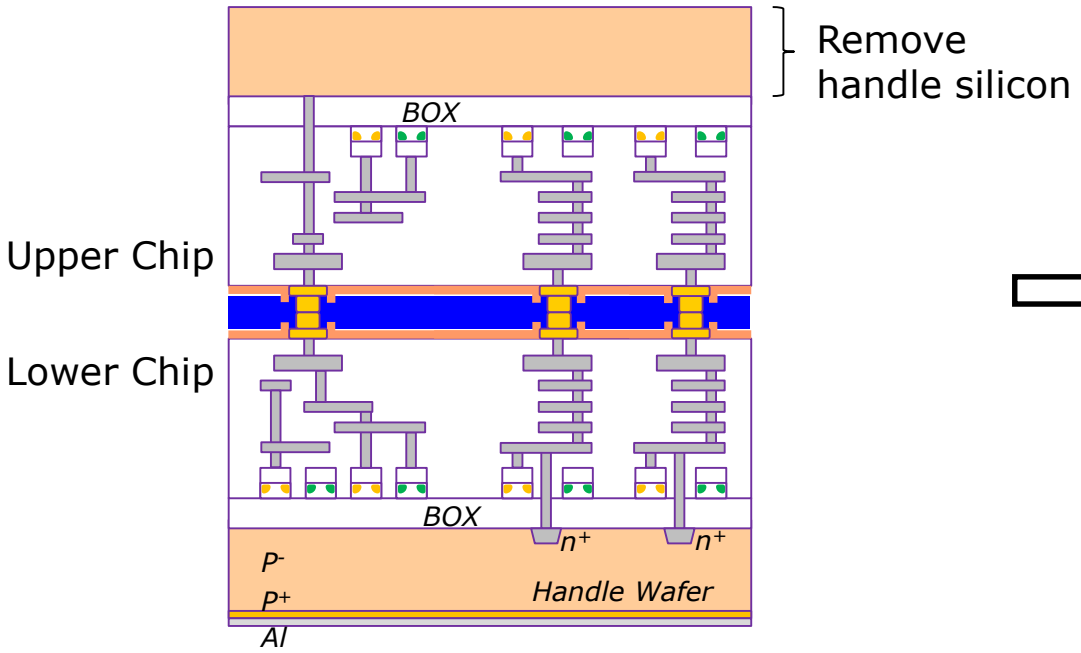
3D-SOI vertical integration

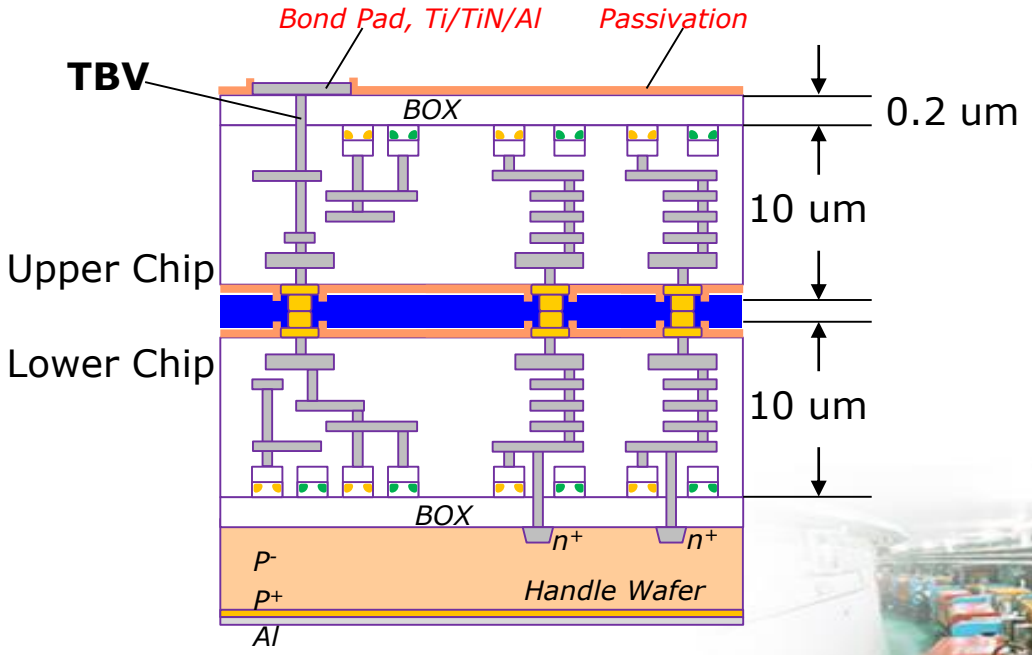
- Originally developed by T-micro and KEK in Japan and demonstrated on the SOFIST 3D chips for the ILC
  - Essentially, flip-chip and micro bump connections
  - Au bump, diameter ~ 3.5 um, pitch ~ 7 um, resistance 0.3 ~ 0.4 Ω
  - **Multiple bumps in each pixel**, for signals and power/ground connections
  - Glue injection for mechanical strength



Compatibility between SOI and 3D

- Through Box Via (TBV) used for the bond pad connections
  - The same type as the connection to the sensing diode (naturally a **Via-first** method)
  - Thickness of BOX layer, 0.2 um
  - **Very small holes**, 0.32 um in diameter
- Handle silicon of the upper chip removed **precisely**, reaching the thin BOX layer and exposing TBVs
  - Wet etching stopped automatically by the Buried Oxide (BOX)
- Bond pads and passivation on top of BOX

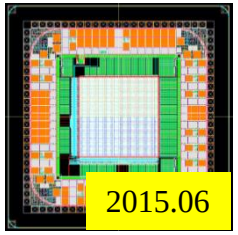




Development of the CPV SOI pixel sensor

- Targeting on a **position resolution ~ 3 um** and a readout scheme compatible with the continuous mode for the proposed CEPC experiment
  - CPV-1&2 for the study of position resolution of small pixels with binary readout (FEE2018)
  - CPV-3 for the study of PDD sensing diode (NIMA 1040 (2022) 167204)
  - CPV-4 for the 3D architecture (this talk)

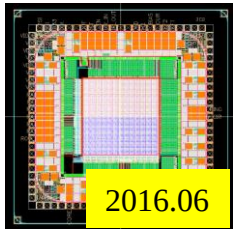
Pixel size:
16 um × 16 um



CPV-1

Process assessment

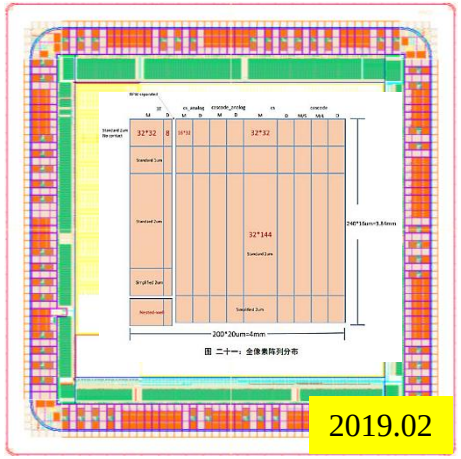
Pixel size:
16 um × 16 um



CPV-2

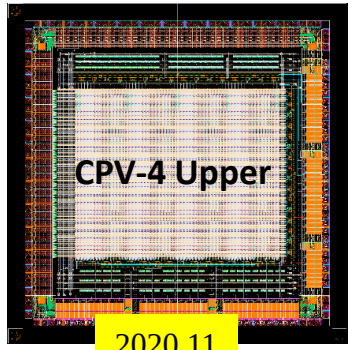
S.P. Resolution 2.3 μm;
Thinned to 75 μm

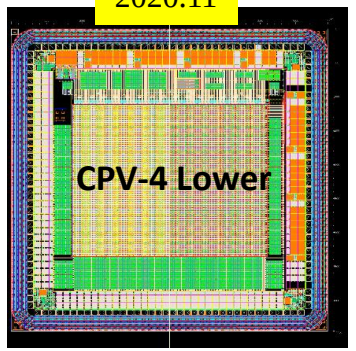
Pixel size:
16 um × 20 um



CPV-3

Pinned Depleted Diode;
Optimized for low FPN 12 e⁻





Pixel size:
17 um × 21 um

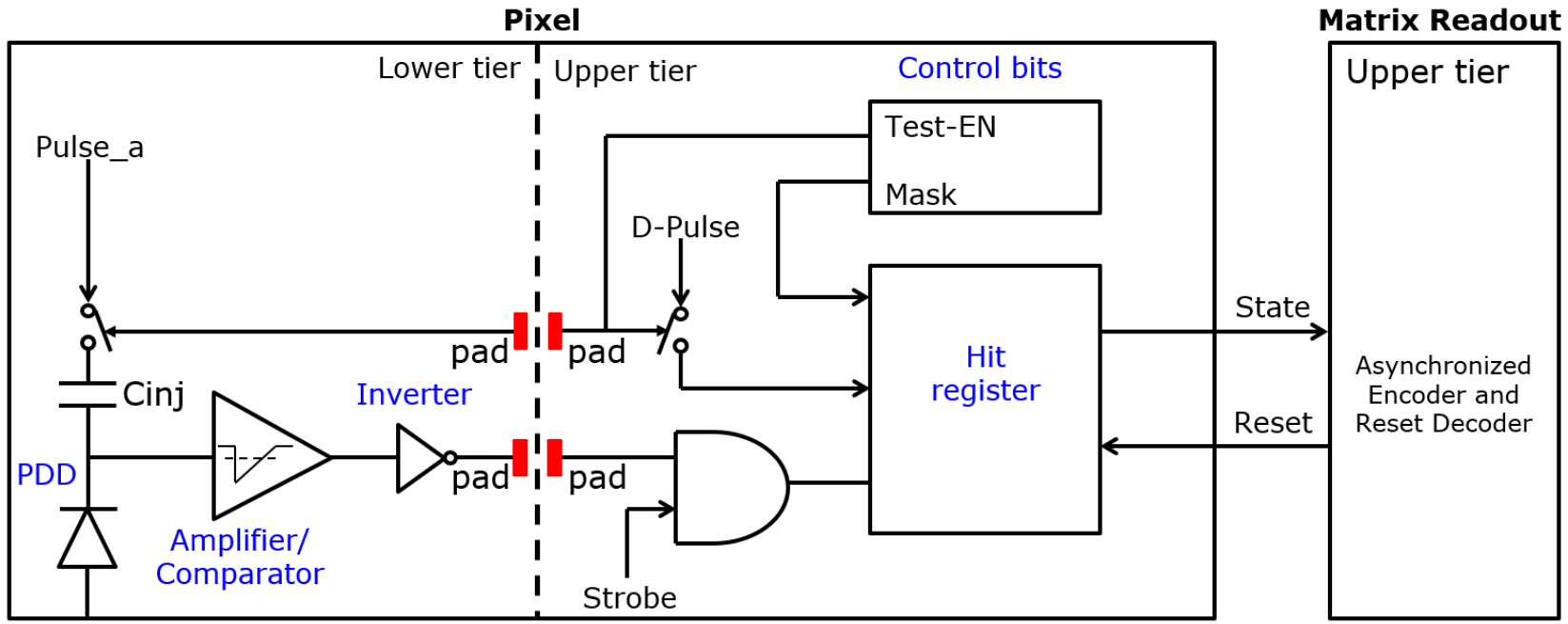
CPV-4

3D architecture;
Stacking process;

Compact Pixel for Vertex (CPV)

CPV-4 design scheme

- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit register + 2 Control bits + Matrix readout
  - Bit 1 for mask, bit 2 for pulse test
- **2 vertical connections** in each pixel: comparator output and configuration bit for pulse test
  - Transition from Analog to Digital domain at the Inverter
  - Analog power/ground has dedicated connections in the chip peripheral

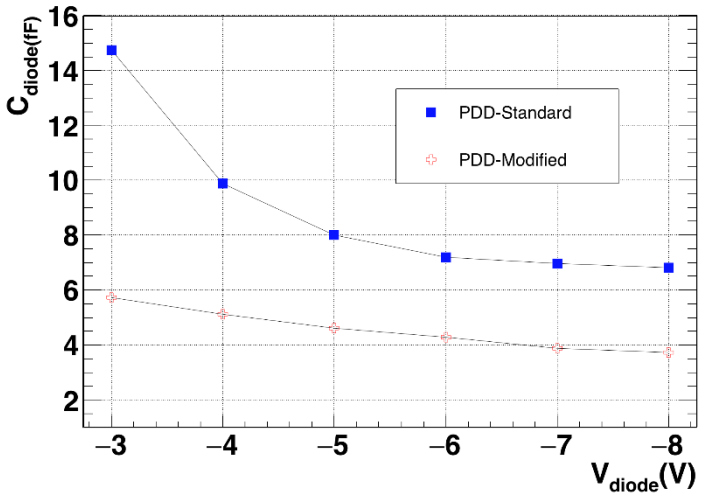


Sensing diode design

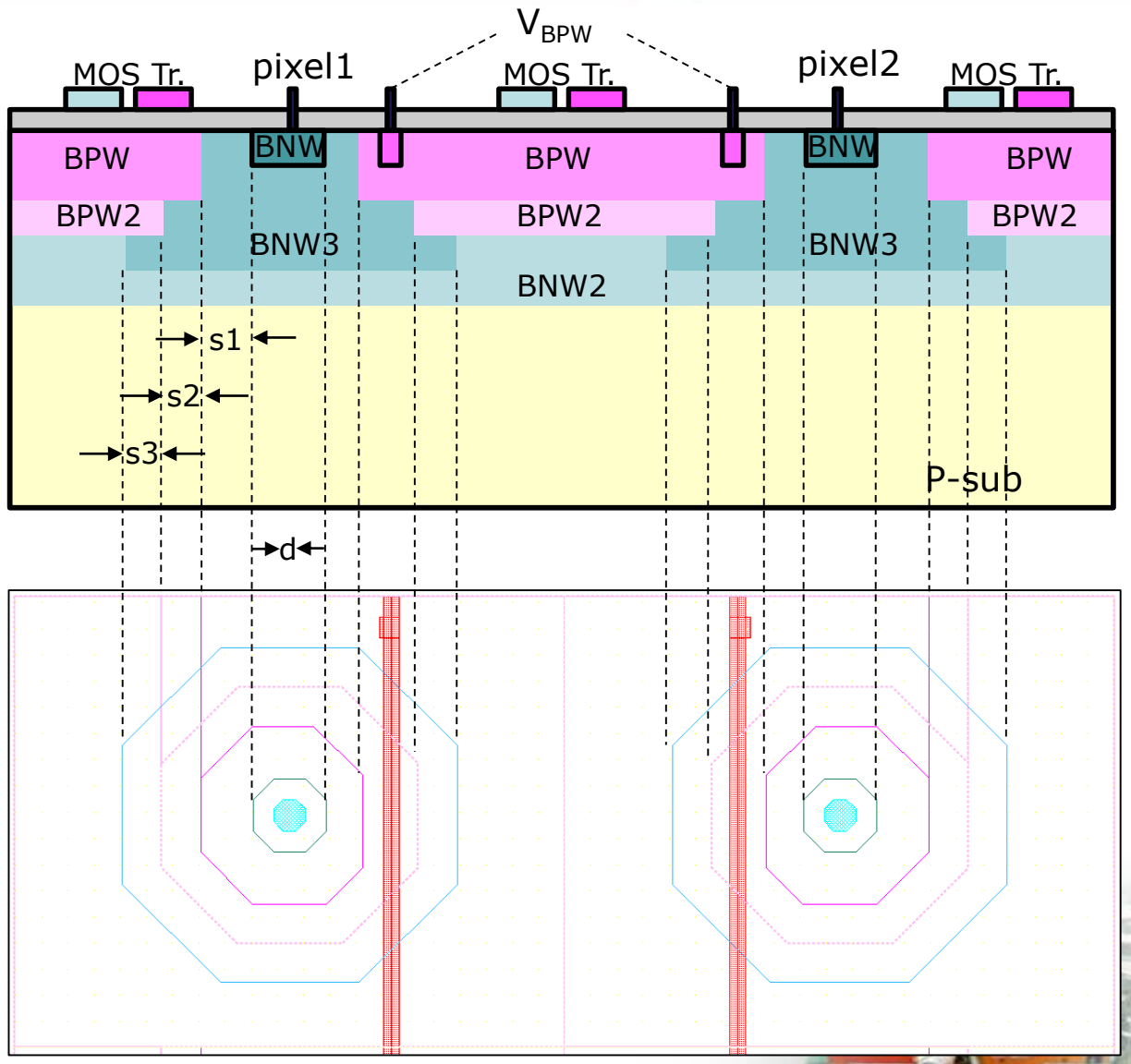
- Geometry parameter optimized for **small pixel pitch**
  - Indicated in the diagram as d, s1, s2, s3

	d	s1	s2	s3
Standard	2.8 um	2 um	1.5 um	1.5 um
Modified	2.8 um	2 um	N/A	N/A

- PDD "Modified" has the BNW3/BPW2 removed
  - Lower diode capacitance than PDD "Standard"

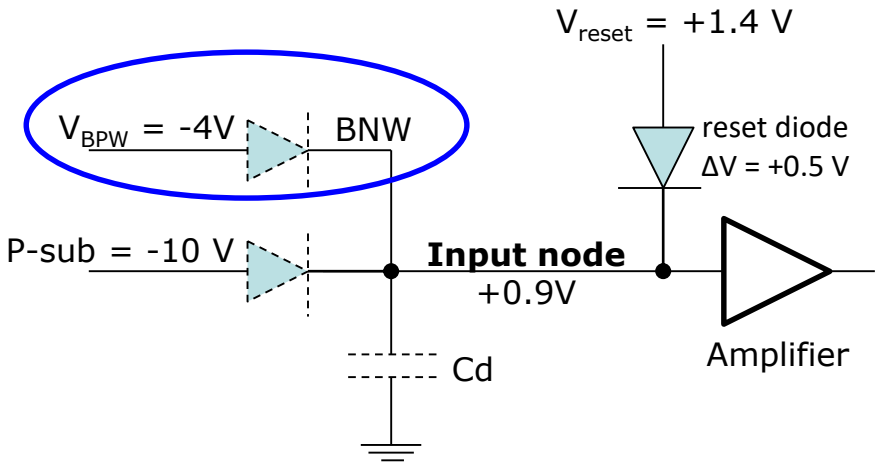


Diode capacitance measured on CPV-3 chip



Bias of sensing diode

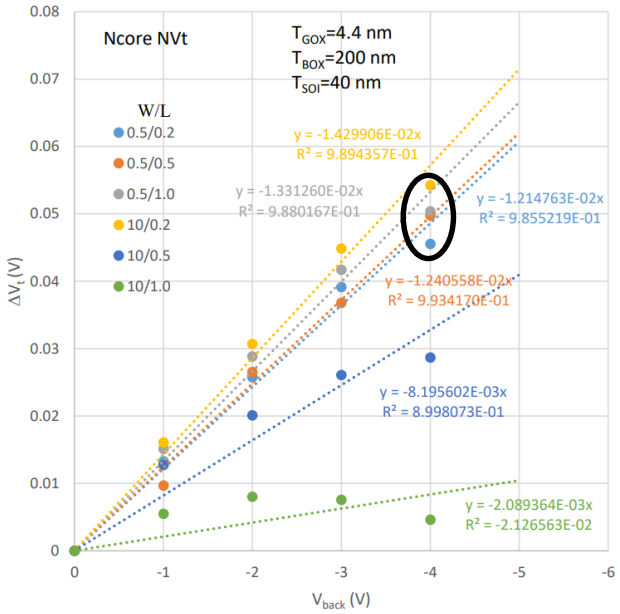
- Bias voltage on the PDD nodes
  - +1.4 V @ V_{reset} to set the DC voltage of input node
  - -4 V @ V_{BPW} to reduce the diode capacitance
  - -10 V ~ -200 V @ P-sub for charge collection
- Cd dominated by the BPW/BNW junction
  - 5 ~ 8 fF @ reverse bias = -4.9 V

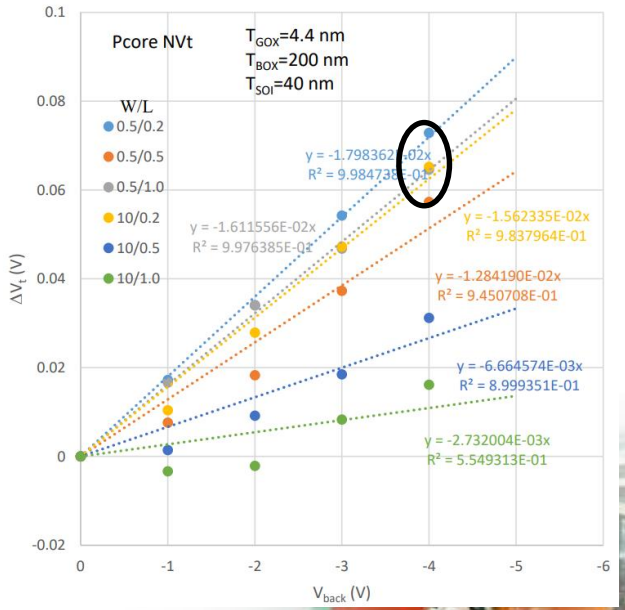


- Transistor threshold shifted due to **back-gate effect**
  - $\Delta Vt = k\, V_{back}$ ($k \sim 0.02$, $V_{back} = V_{bpw}$)

$$\Delta V_t = \frac{T_{GOX}}{T_{BOX} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} T_{SOI}} V_{back} = kV_{back}$$

- ΔVt measured by KEK and modeled in HSPICE
  - +50 mV @ V_{bpw} = -4V for NMOS
  - -70 mV @ V_{bpw} = -4V for PMOS



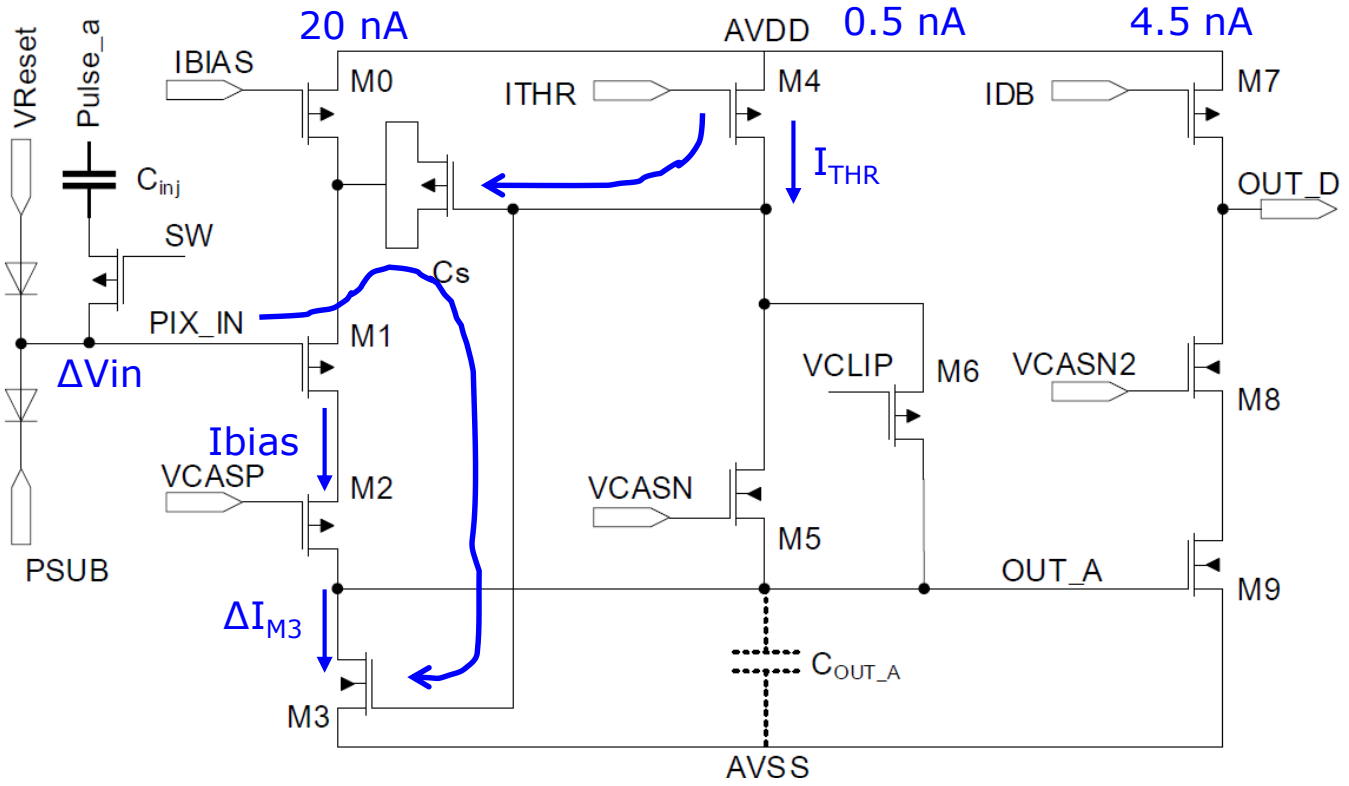


Analog Front-end

- $\Delta V_{IN} < 0 \rightarrow \Delta V_{g\_M3} < 0 \rightarrow V_{OUT\_A}$ charged by $-\Delta I_{M3} \rightarrow C_S$ charged by $I_{THR} \rightarrow V_{g\_M3}$ restored $\rightarrow V_{OUT\_A}$ restored
- **Peaking time** $= \Delta V_{OUT\_A} \cdot C_{OUT\_A} / -0.5\,\Delta I_{M3} = -\Delta V_{IN} \cdot C_S / I_{THR} \sim us$
- $\Delta V_{OUT\_A} = \frac{Q_{IN}}{C_{IN}} \cdot \boldsymbol{V_{GAIN}} = \frac{Q_{IN}}{C_{IN}} \cdot \left(\frac{C_S}{C_{OUT\_A}} \cdot 0.5 \frac{-\Delta IM_3}{I_{THR}}\right)$
  - Q_{IN} / C_{IN} ~ a few mV
  - C_S / C_{OUT_A} ~ 50
  - $-\Delta I_{M3} / I_{THR}$, 1.5 ~ 2 @ small signal
- *OUT_D* passes **HIT threshold** when

$$V_{OUT\_A} = Baseline + \Delta V_{OUT\_A} > V_{T\_M9}$$

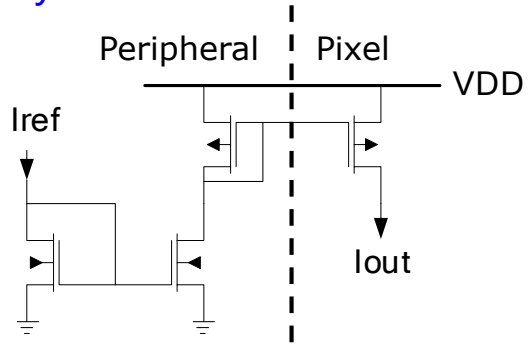
  - Baseline = V_{CASN} - V_{T_M5} = 710 mV
  - ΔV_{OUT_A} > 100 mV



Original design from the ALPIDE chip for the ALICE tracker upgrade, **very low current**, reported on TWEPP 2016 by Thanushan Kugathasan, CERN

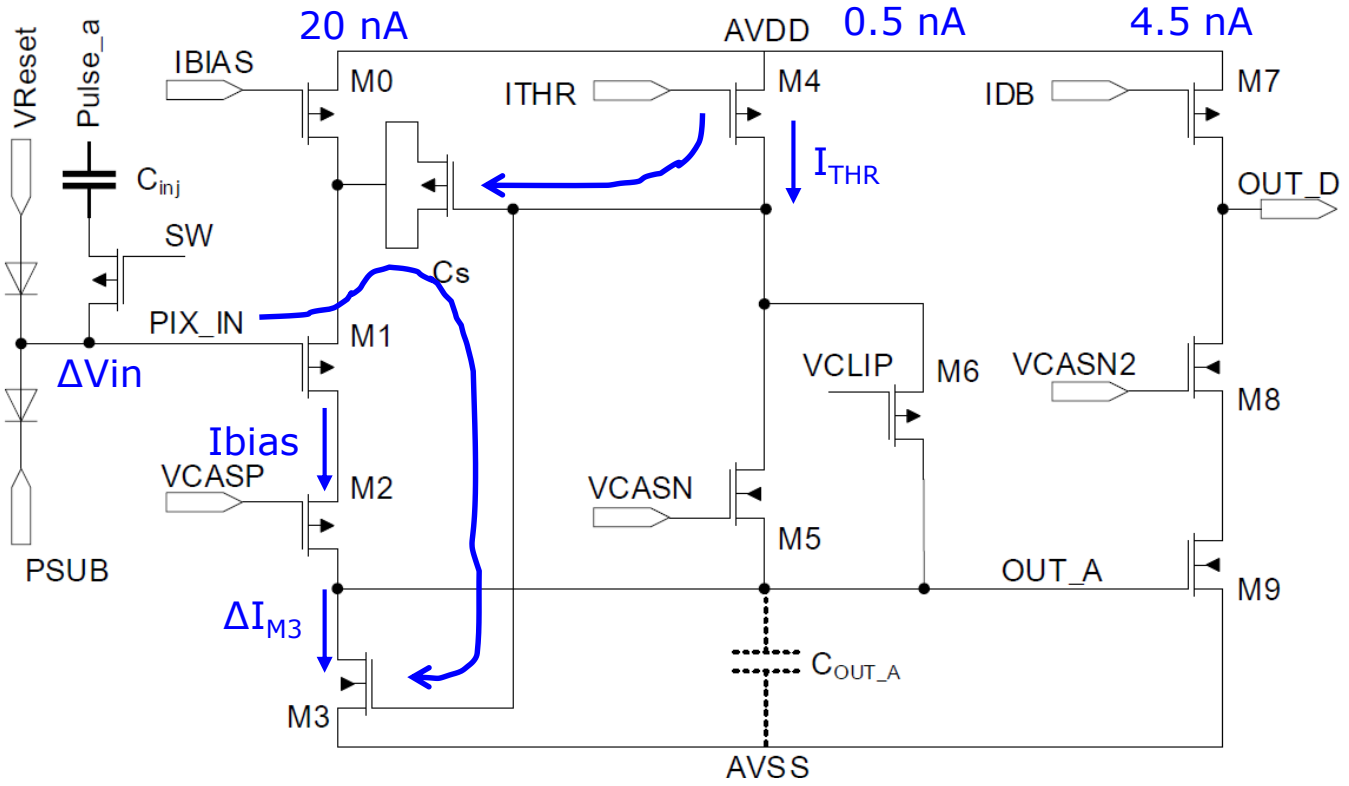
Mitigation of back gate effect (shifted V_T)

- Current mirror biased @ BPW = -4V in the peripheral
  - V_T shifted by the same amount as that of the current source (M0, M4, M7) in pixel



- Other pixel transistors
  - Compensated by gate voltage

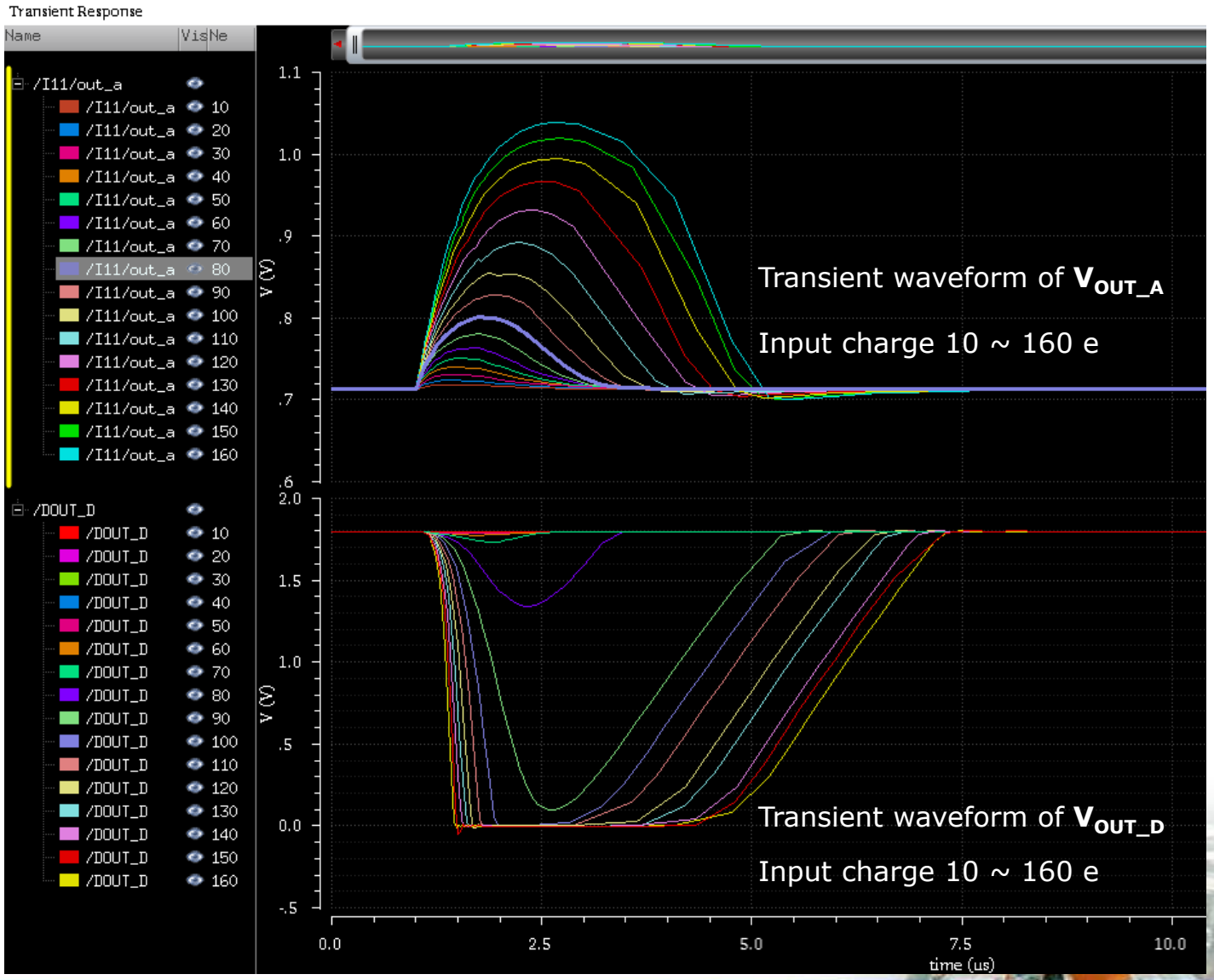
Transistor	Gate voltage
M1	V_{reset}
M2	V_{CASP}
M3	feedback via M5
M5	V_{CASN}
M6	V_{CLIP}
M8	V_{CASN}
M9	V_{CASN2}



Original design from the ALPIDE chip for the ALICE tracker upgrade, **very low current**, reported on TWEPP 2016 by Thanushan Kugathasan, CERN

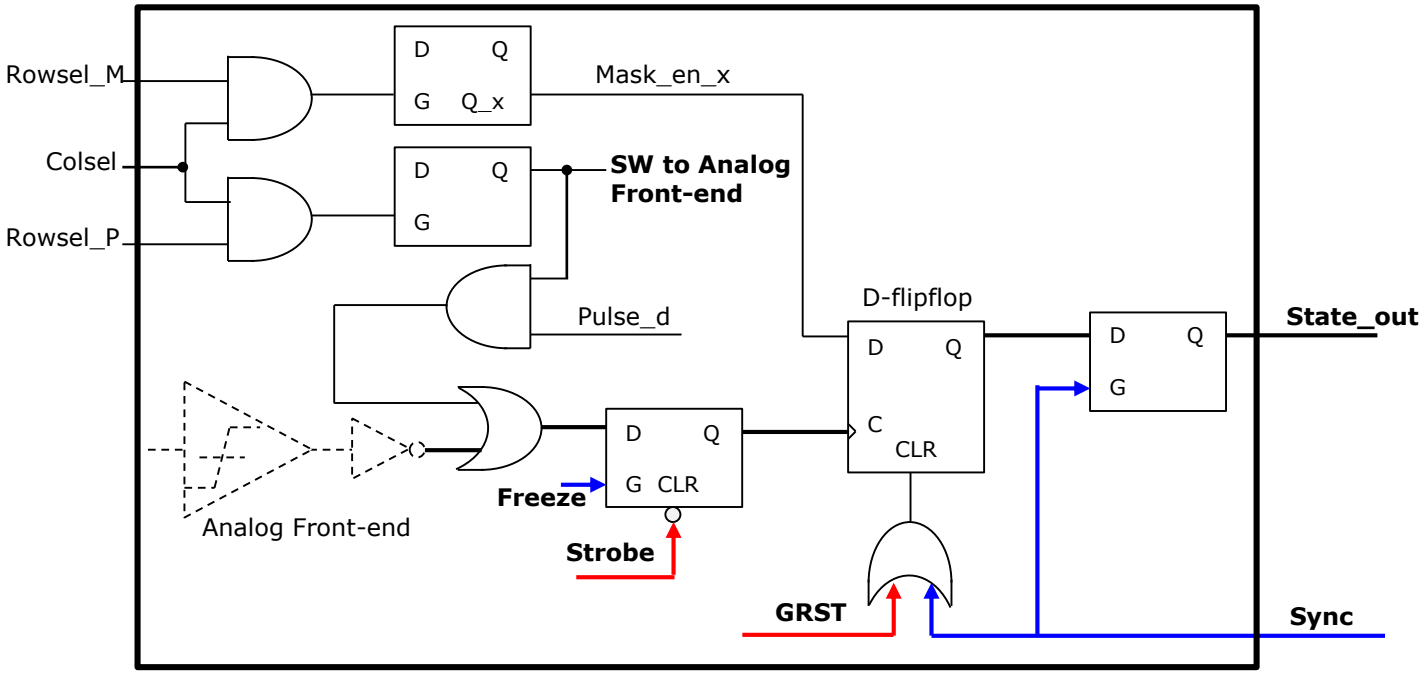
Simulation

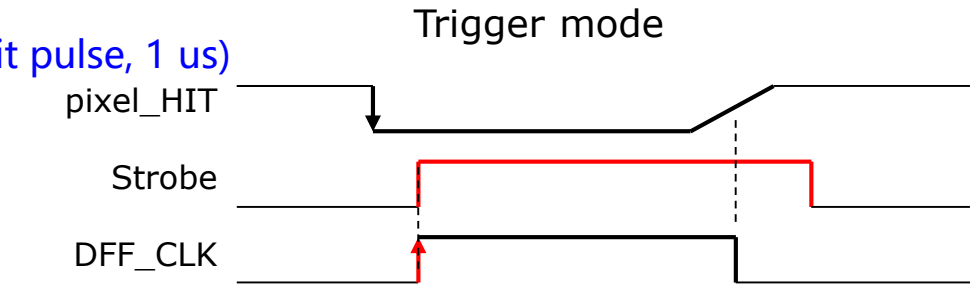
- **Threshold** ~ 85 e^- @ I_{THR} = 0.5 nA and V_{OUT_A} *baseline* = 0.71V
  - Gain = 2.6 mV / e^-
- Noise voltage @ V_{OUT_A} = 3.5 mV
  - ENC = 1.3 e^-
- V_{OUT_D} pulse duration < 6 us
  - **Time walk** < 1 us, still an essential capacity to exploit to provide timestamps and reject the hits from radiation background as many as possible (offline)
  - Hit to be registered at the leading edge

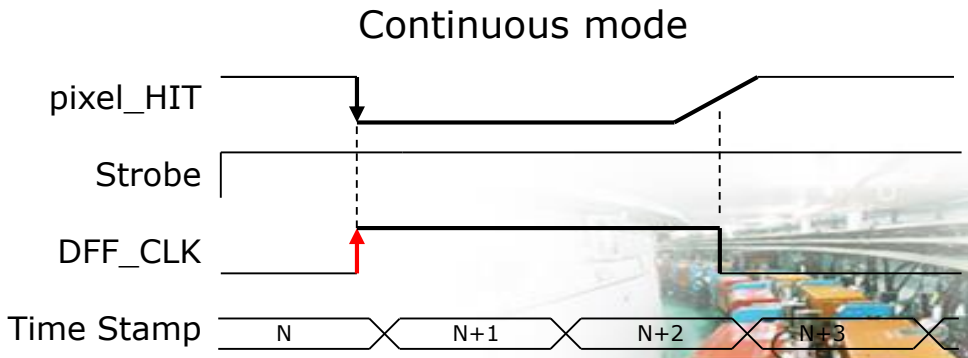


Pixel logic

- D-latches for *Mask* and *Pulse* configuration
- D-flipflop to store the hit pulse
  - **Trigger mode**: only hit pulses that coincided with external *Strobe* pulse
  - **Continuous mode:** all hit pulses with constant *strobe = 1*
- Time of hit can be derived offline
  - Either from the *Strobe window* (plus 2 × hit pulse duration, 2 × 6 us)
  - Or from the *time stamp* attached in the peripheral (plus time walk of hit pulse, 1 us)







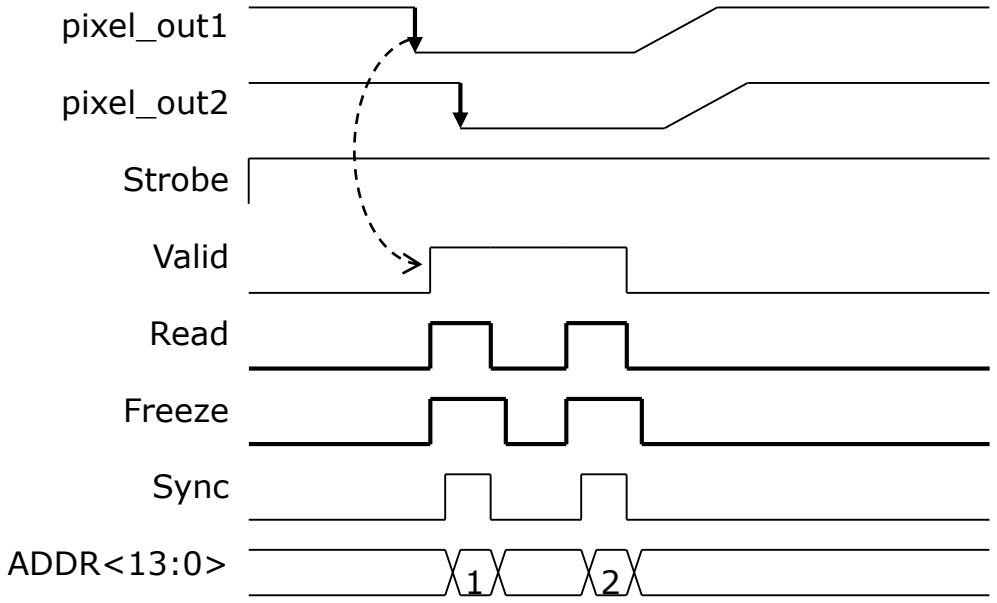
Sparsified readout of Matrix

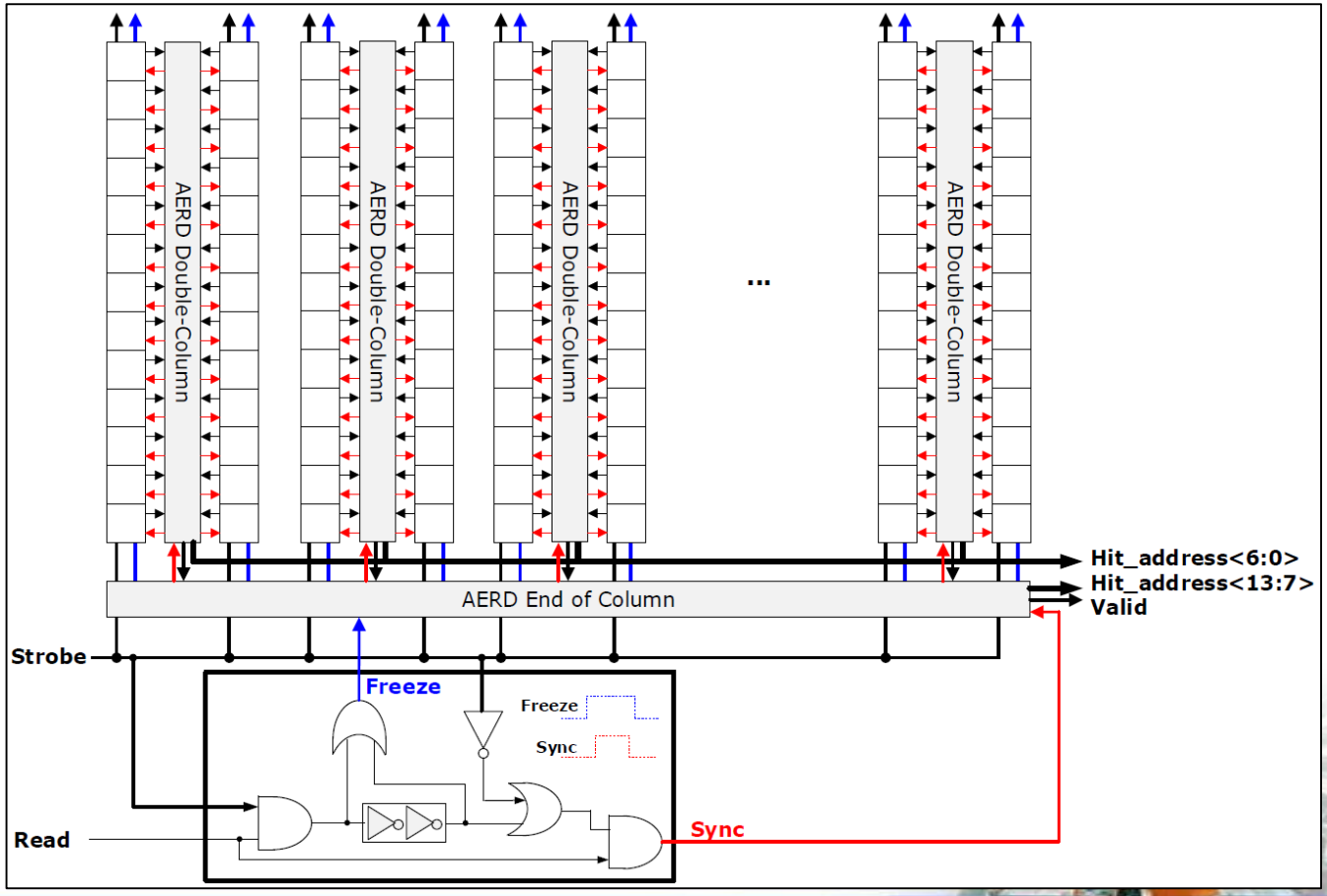
- Hit Readout and Reset scheme following the ALPIDE design (**100 ns / pixel hit**)
  - **HIT** address encoded: low bits from the columns and high bits at the EoC
  - **SYNC** signal decoded in the reverse way, to clear the HIT bit

  } Asynchronized Encoder and Reset Decoder (**AERD**)
  *Ping Yang et al., NIMA 785 (2015) 61-69

- **Freeze the pixels** to prevent possible interruption of readout sequence
  - Synchronized with the readout sequence
  - Applied to one double-column at a time,

  to minimize overall dead time

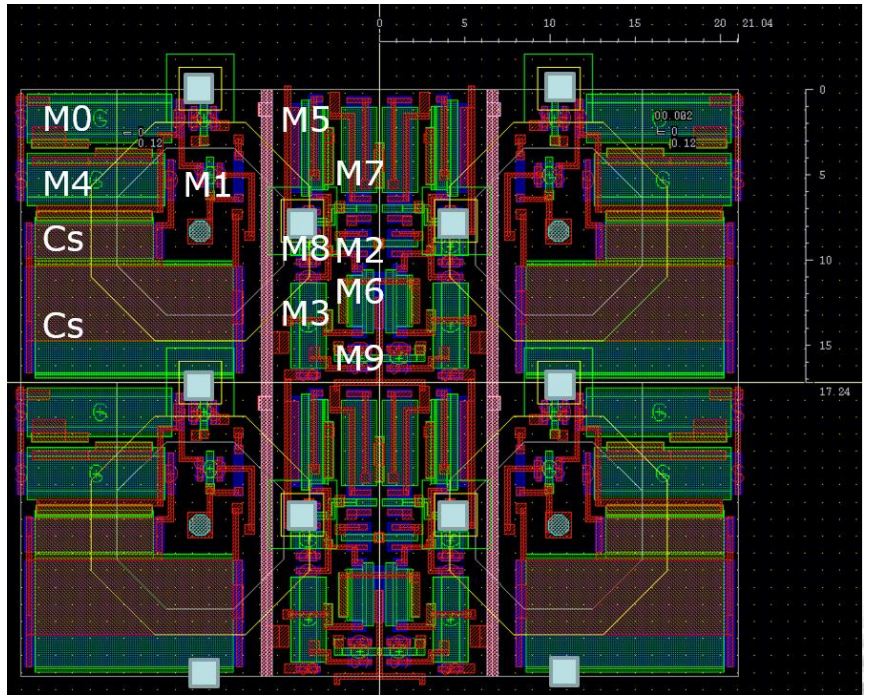




Layout of Pixel Array

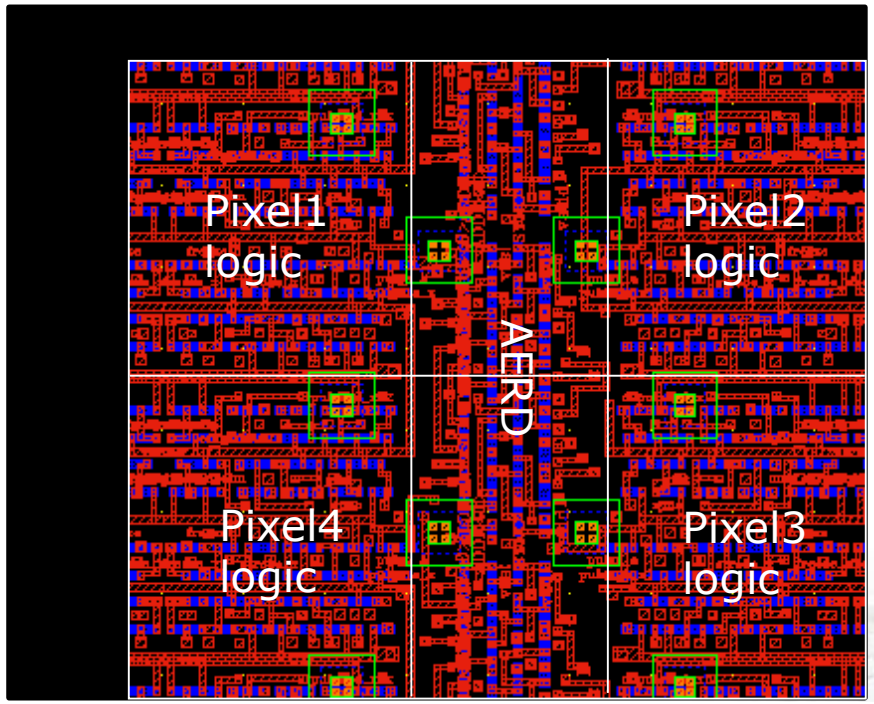
- Pixel pitch: 17 um × 21 um (compared to 16 um × 20 um in CPV-3 with only amplifiers in pixel)
- Sensing diode guarded against the dynamic part of Analog Front-end
  - To minimize the electric coupling between them
- Pixel logic and AERD by manual drawing, 110 transistors / pixel on average

3D bumps marked with ▢



CPV4_Lower (2 × 2 pixels)

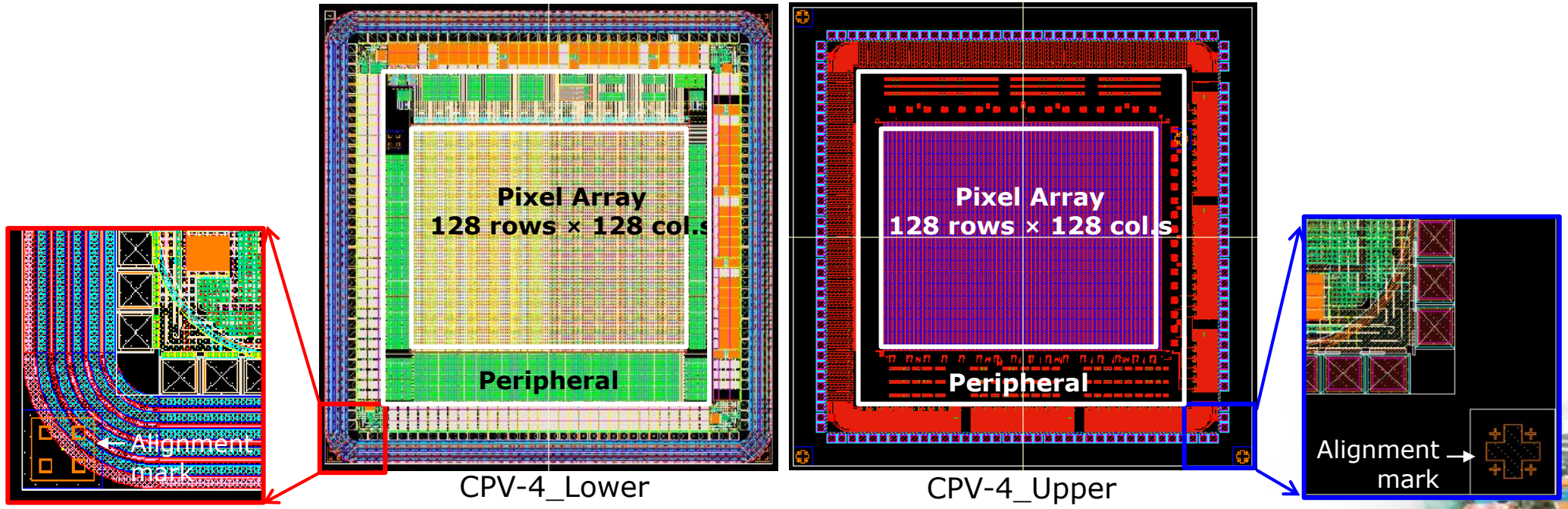
3D bumps marked with ▣



CPV4_upper (2 × 2 pixels)

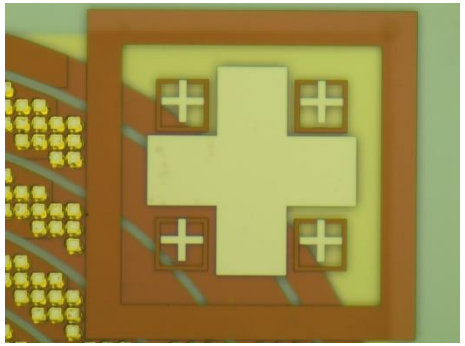
Layout of full chips

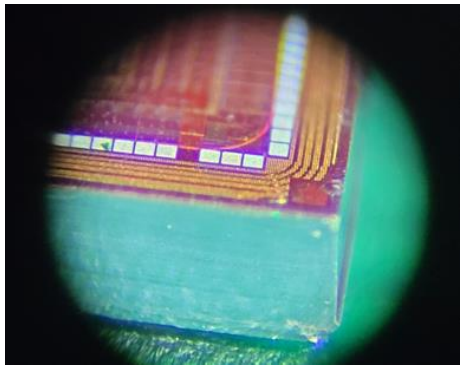
- Single chip area: 4.45 mm × 4.45 mm, with sensor guard-rings included
  - Pixel array 128 rows × 128 columns, covering 2.2 mm × 2.7 mm
  - Peripheral circuits: current mirror, pulse generator / AERD EoC, I/O interface logic
  - Alignment marks for 3D stacking

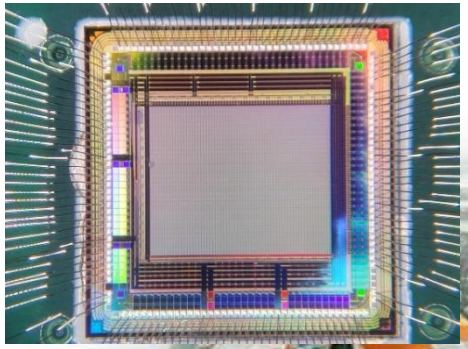


Manufacturing and 3D processing

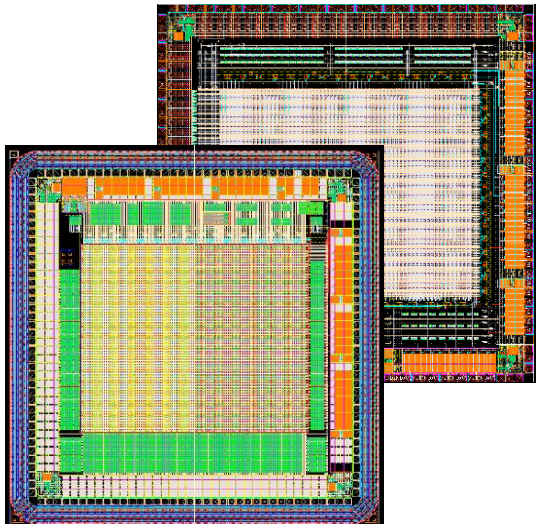
- CPV-4_L and CPV-4_U submitted to SOI foundry in Dec. 2020
  - Single chips delivered in June 2021
- 3D integration done by T-Micro in Japan
  - Chip-to-chip, staring from one single wafer
  - 3D chips delivered in the summer 2022





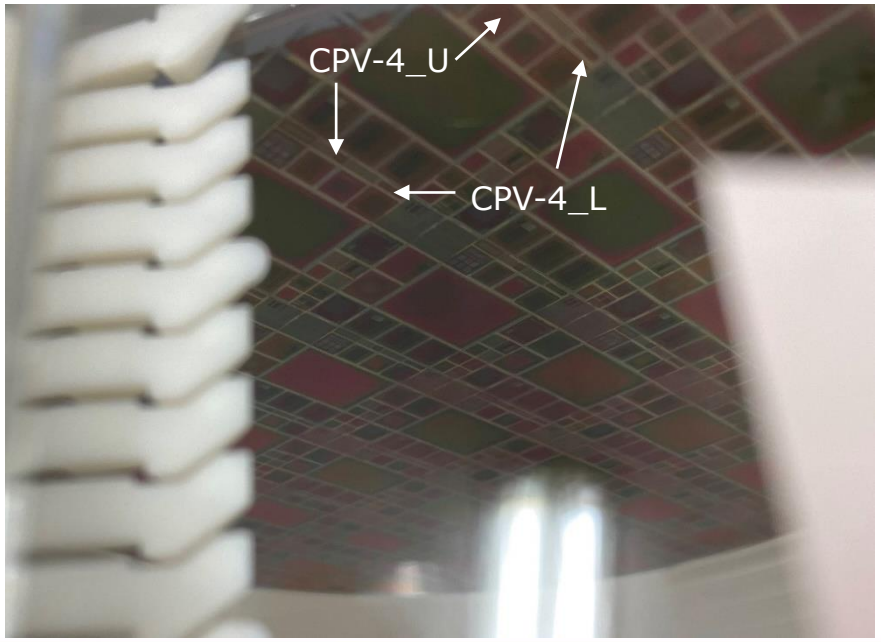


Layout of CPV-4_U



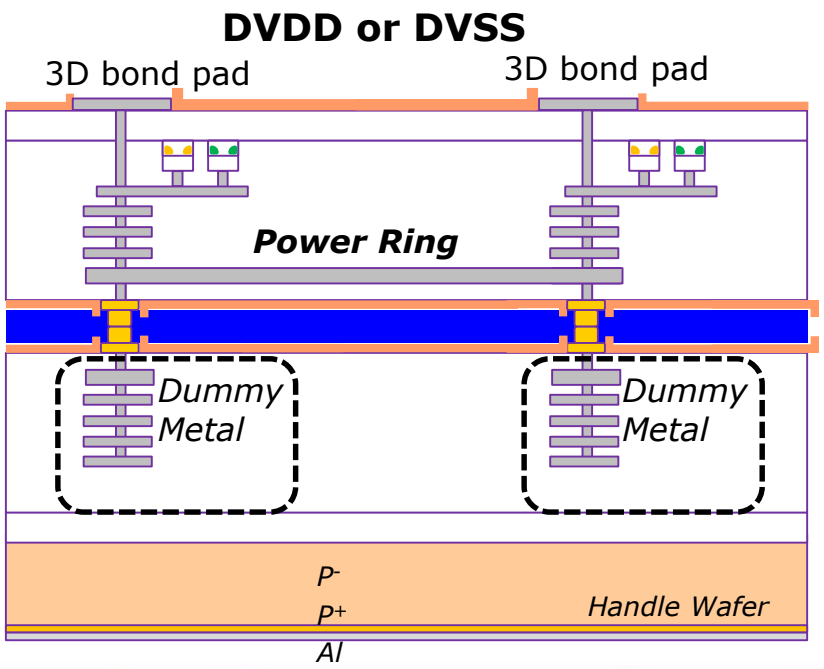
Layout of CPV-4_L

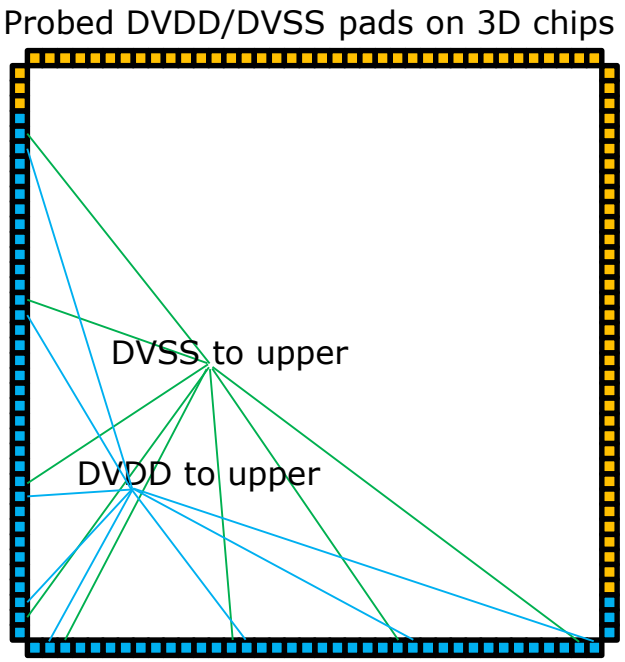
CPV4_L/U on the WMP Wafer

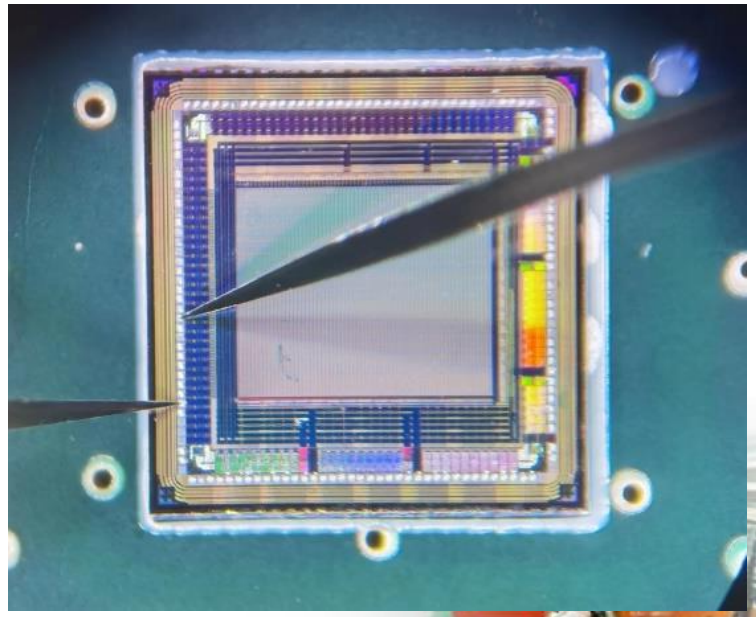


Measurement of 3D connection to upper tier

- Probe test on the 3D chips: from 3D bond pad to **the upper tier**
  - Measure the resistance between two power pads (DVDD) or two ground pads (DVSS)
  - 2 ~ 6 Ω, electrical connection established
  - Yield 100% on 3 tested chips

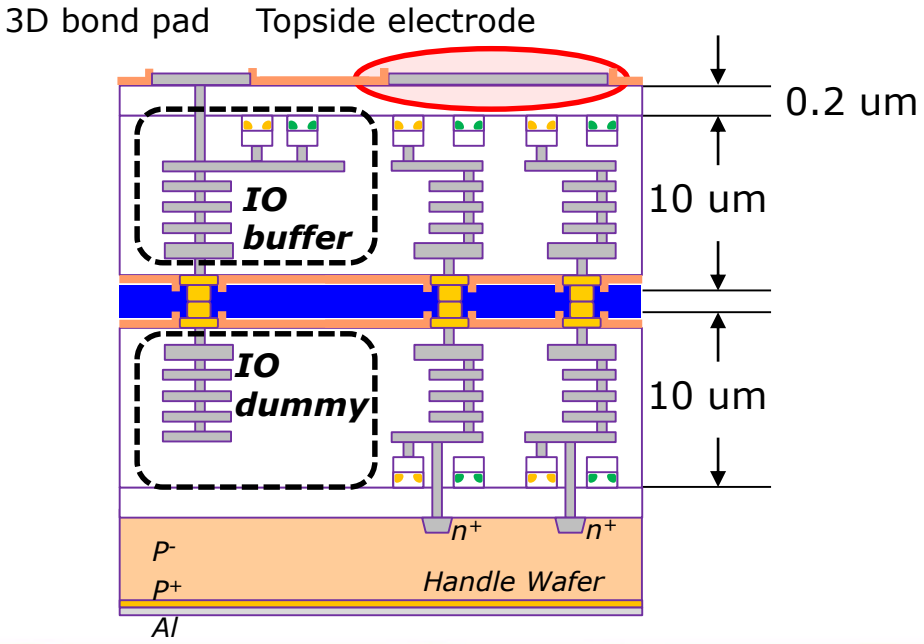


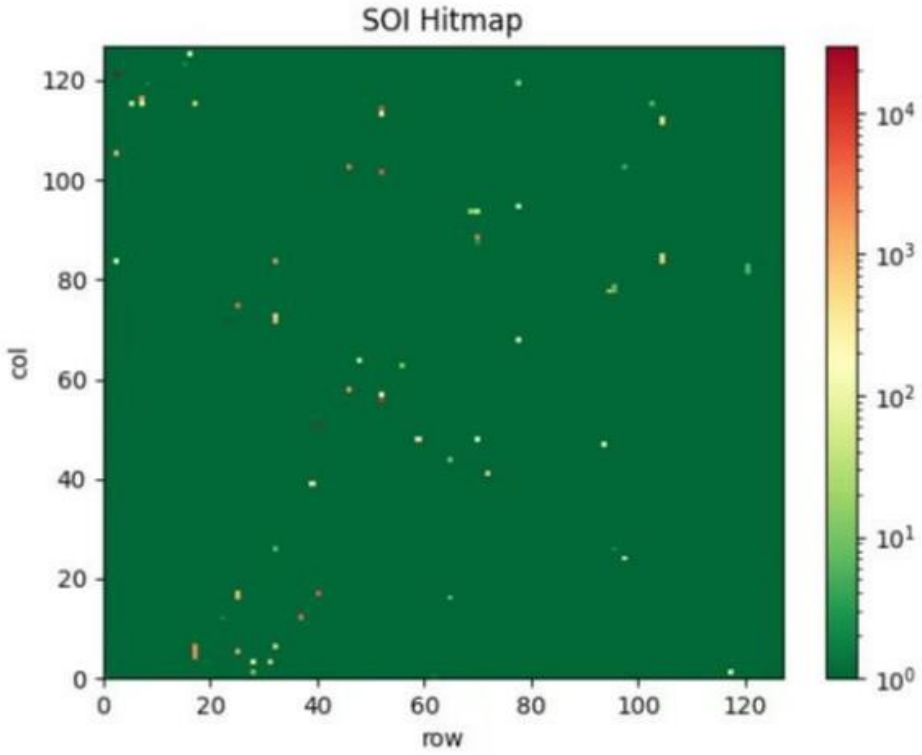




Tests on the upper tier

- Logic interaction with an FPGA readout board
  - Write to pixel configuration bits
  - Injection of digital test pulse and hit readout
- One 3D chip was found **fully functional** so far
  - A couple more chips partially functional
- Necessity of topside electrode is under study
  - To define the back gate conditions for the upper tier

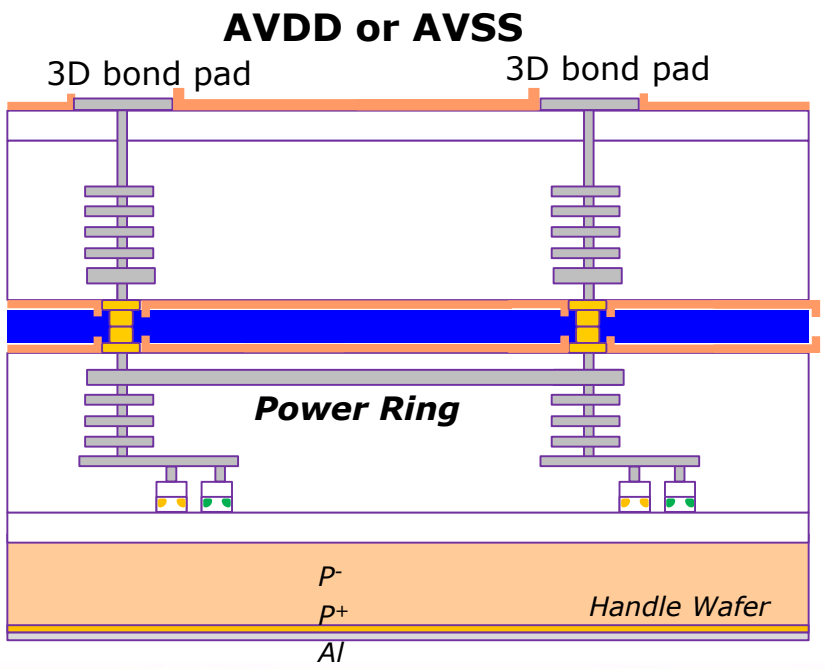


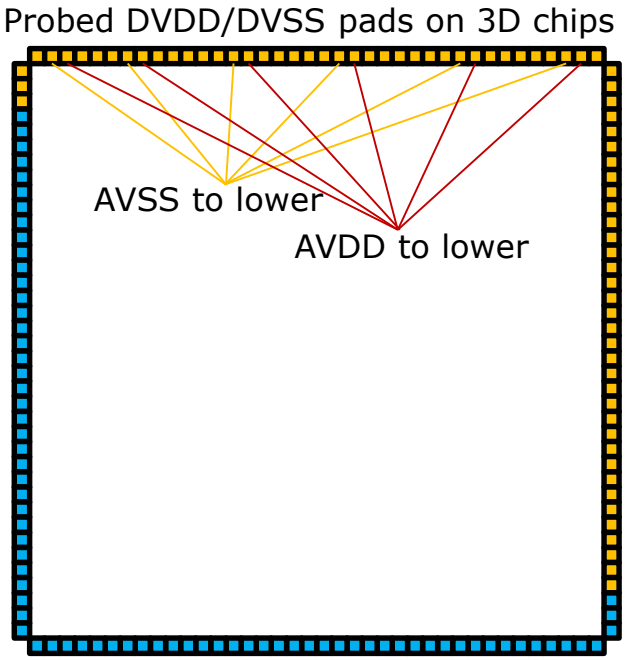


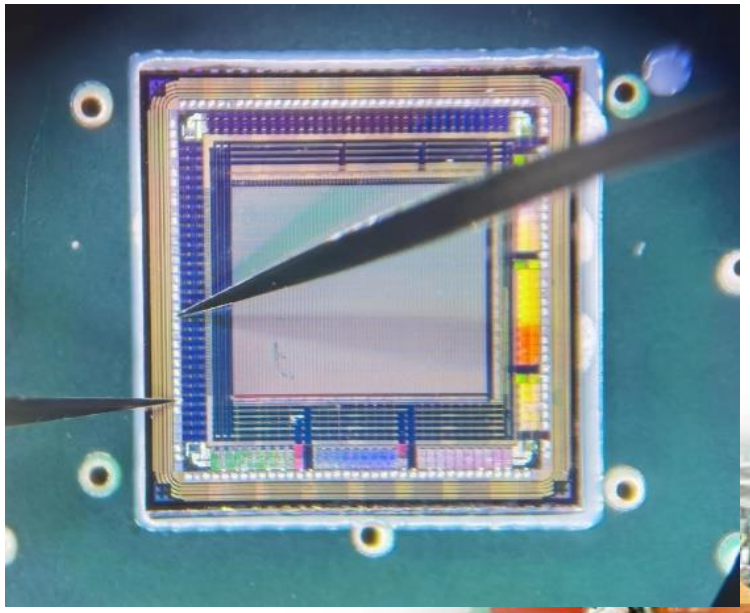
Hit map of the full matrix in digital pulse test, with masked pixels and noisy pixels visible.

Measurement of 3D connection to lower tier

- Probe test on the 3D chips: from 3D bond pad to **the lower tier**
  - Measure the resistance between two analog power pads (AVDD) or two analog ground pads (AVSS)
  - Hundreds of kΩ, poor connections
  - Yield 30% on 3 tested chips
- Fortunately, some other chips were found functional
  - Analog Front-end was tested

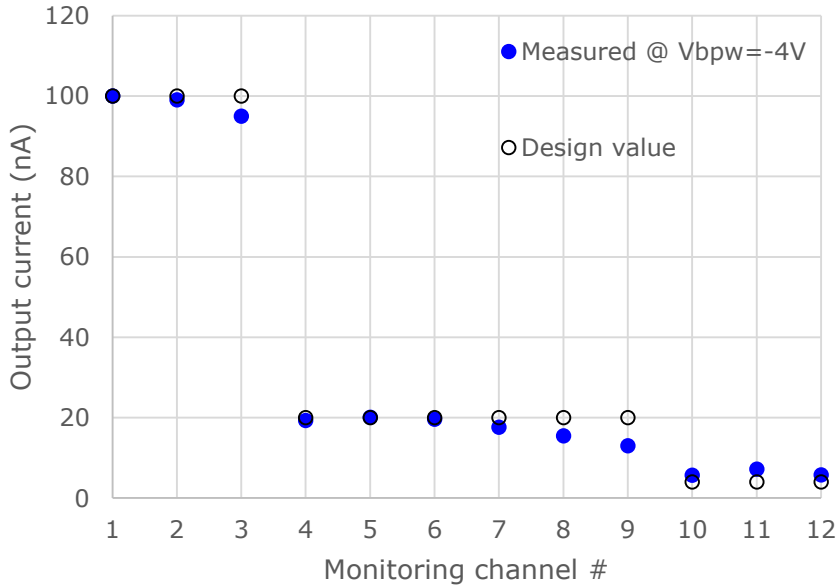




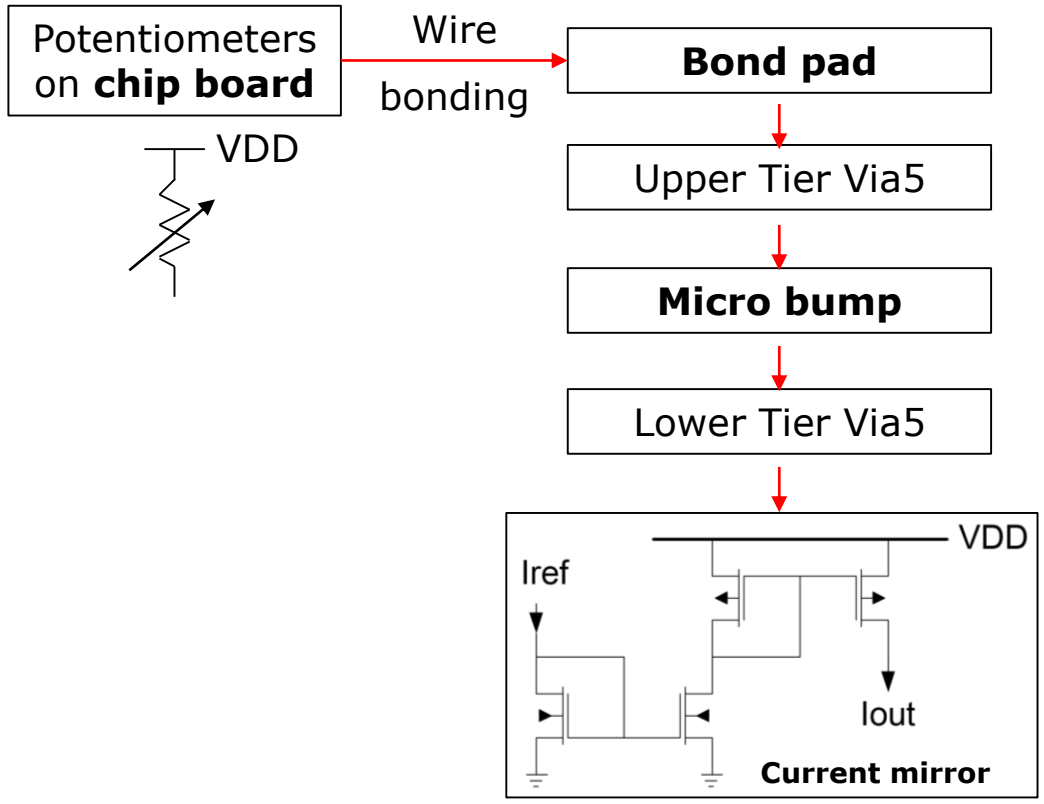


Tests on the current mirror

- Current mirrors in **Lower Tier** worked properly
  - Verification of the vertical connection to the lower tier
- Measurement on 12 different monitoring channels (I_{OUT})
  - With design values ranging from 4 nA to 100 nA
  - All set to the target value with **back-gate** biased @ V_{BPW} = -4 V

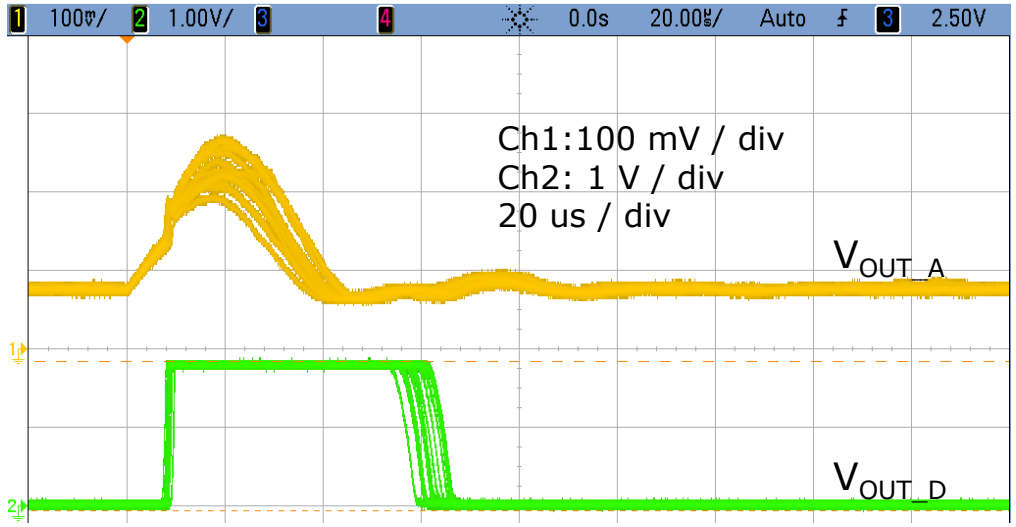


Electrical connection to the current mirror in lower tier

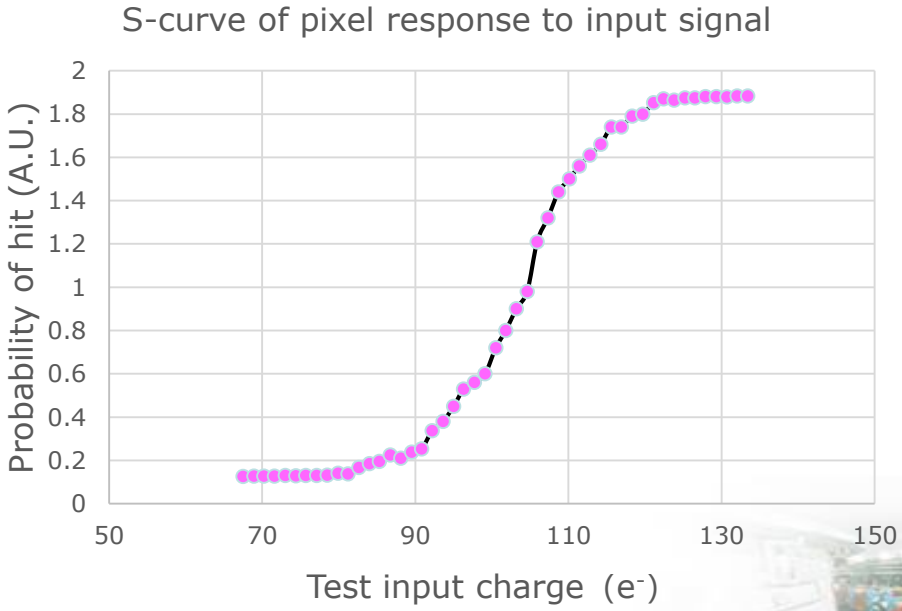


Tests on the Analog Front-end

- Injected test pulses and observed waveforms @ V_{BPW} = -4V
  - Baseline of V_{OUT_A} = 750 mV (calibrated for the buffer chain) @ V_{CASN} = 1.52V
  - Threshold charge = 103 e @ I_{THR} = 0.5 nA
  - Gain = 1mV / 1e with amplitude @ threshold
  - Noise = 4.5 e^- from s-curve measurement

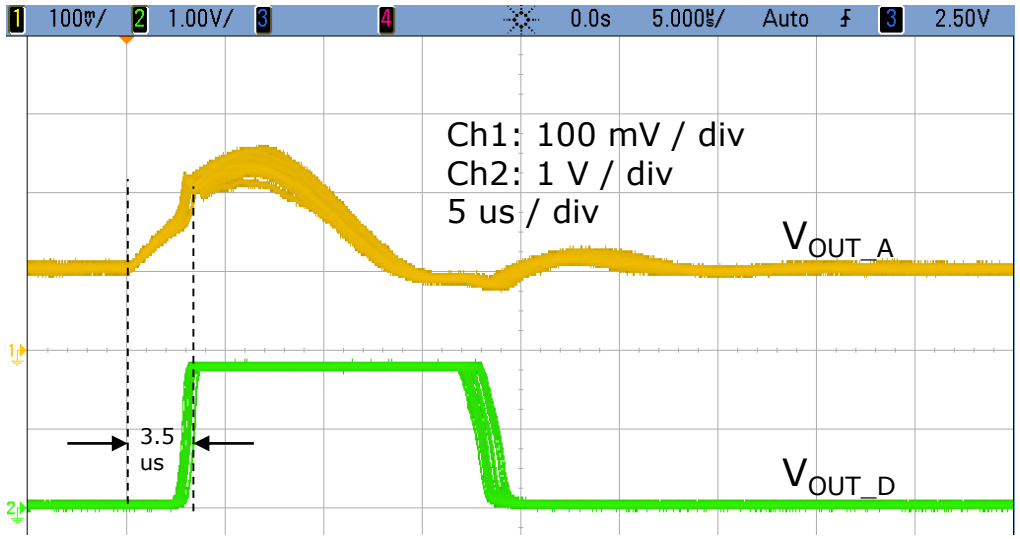


Analog frontend @ V_{BPW} = -4V
Test charge injected ~ 150 e^-

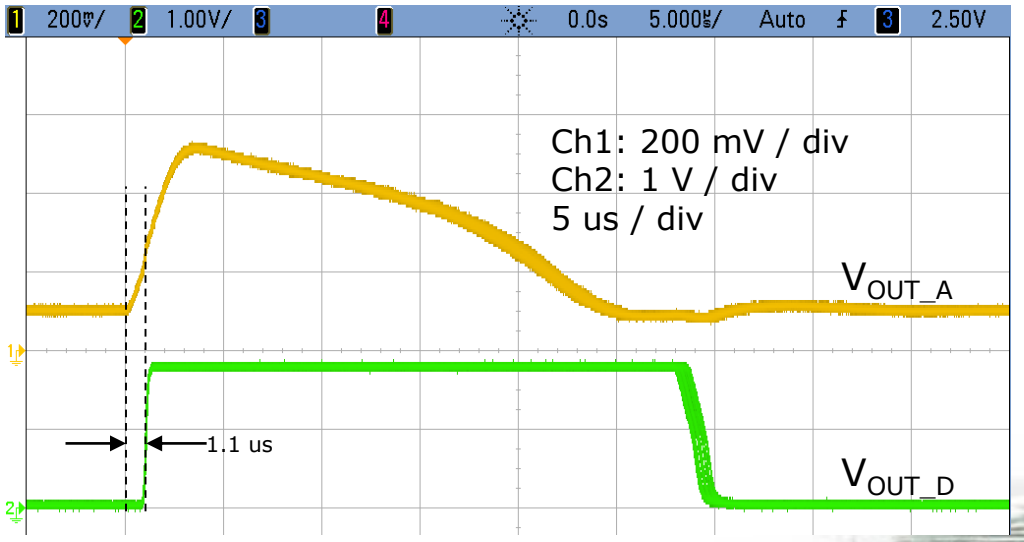


Tests on the Analog Front-end

- Estimate of time walk on V_{OUT_D} ~ 2.4 us
  - Maximum delay 3.5us @ 150 e^-
  - Minimal delay 1.1us @ 600 e^-
  - Pulse width greater than in simulation, I_{BIAS}, I_{THR}, I_{DB} set to twice the nominal value



Analog frontend @ V_{BPW} = -4V
Test charge injected ~ 150 e^-



Analog frontend @ V_{BPW} = -4V
Test charge injected ~ 600 e^-

Summary and outlook

- 3D chip-to-chip bonding being pursued for high granularity of pixel with complex functionality
  - Micro bump pitch down to 7um, providing multiple connections in pixel level
  - Compatible with the existing SOI process, including low temperature stacking, TBV, thinning
- First trial of CPV-4 finished with encouraging results
  - A few samples with lower and upper tier operational
- Investigation of 3D connection yield will continue on the second wafer
  - Process tuning with T-micro based on the present results

Acknowledgment

- The SOI pixel detector and 3D bonding process have been developed in the framework of SOIPIX collaboration. The authors thank all the collaborators, especially Yasuo Arai, Ikuo Kurachi, Makoto Motoyoshi and Miho Yamada.

- This work is supported by the National Natural Science Foundation of China under grant number 11935019, 11575220.

Grazie!

Thanks for your time!

Backup slides

Specification of Vertex detector

- high spatial resolution, low material budget and fast readout required by the flavor tagging
  - Pixel sensor, the core part to construct a vertex detector

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs → Pixel sensor specs

$\sigma_{s.p.}$ ~ 2.8um → **Small pixel** ~ 16um

Material budget ~ 0.15% X_0/layer → **Thinning to** ~ 50um

→ **low power** ~ 50mW/cm^2

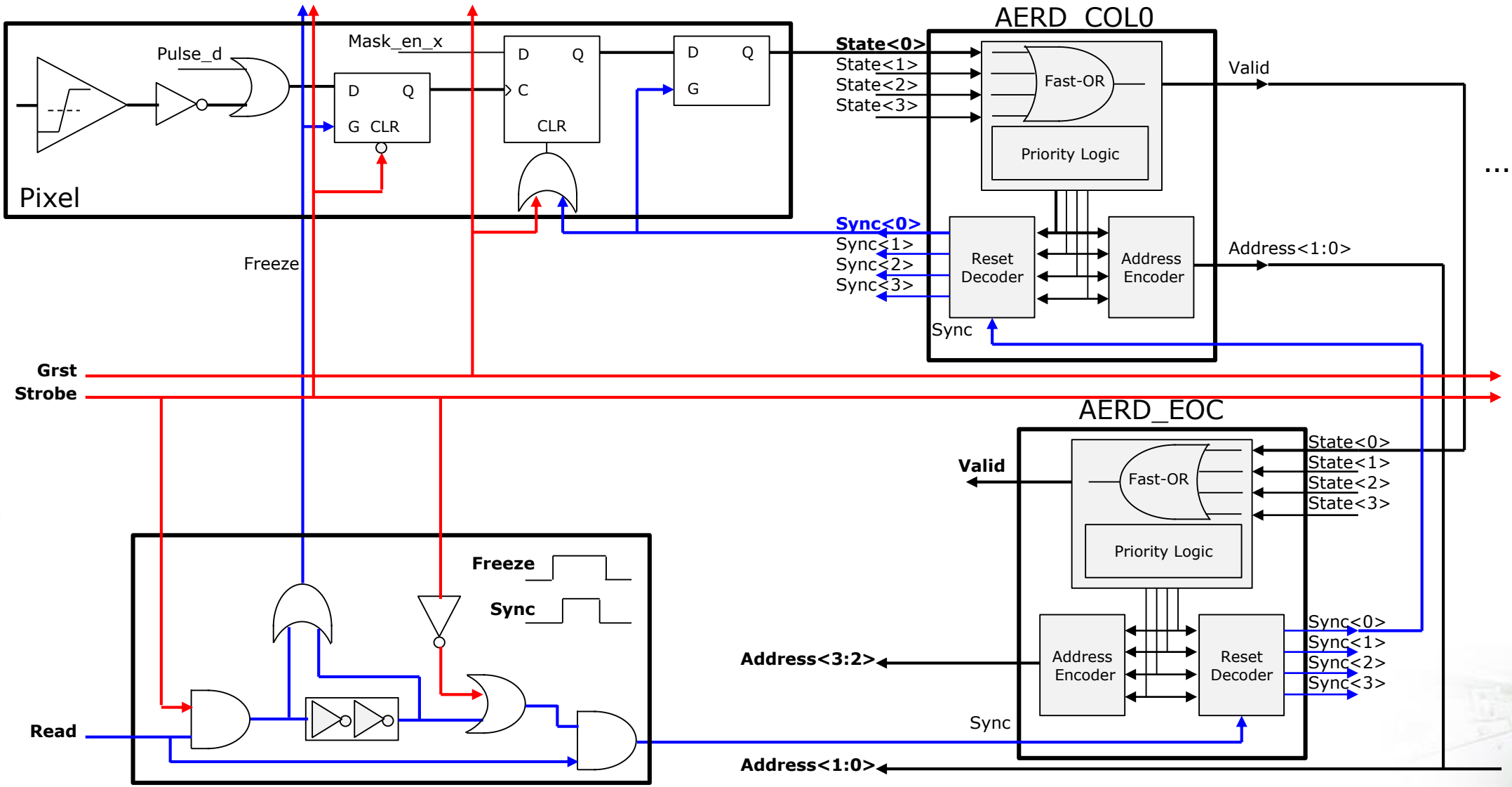
r of Inner most layer ~ 16mm → **fast readout** ~ 1us

→ **radiation tolerance** ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\,year)$

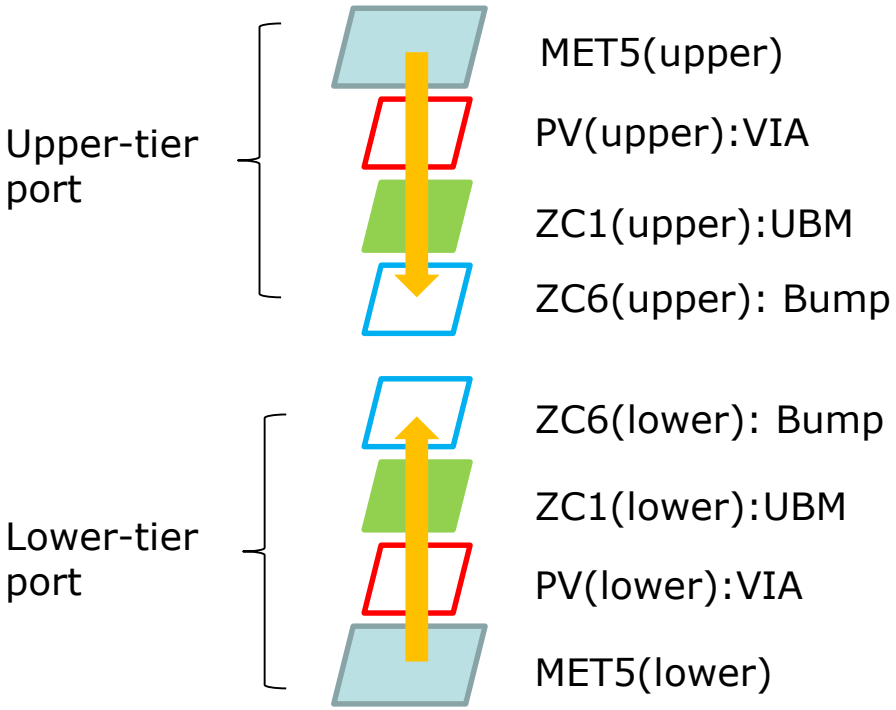
Readout Architecture



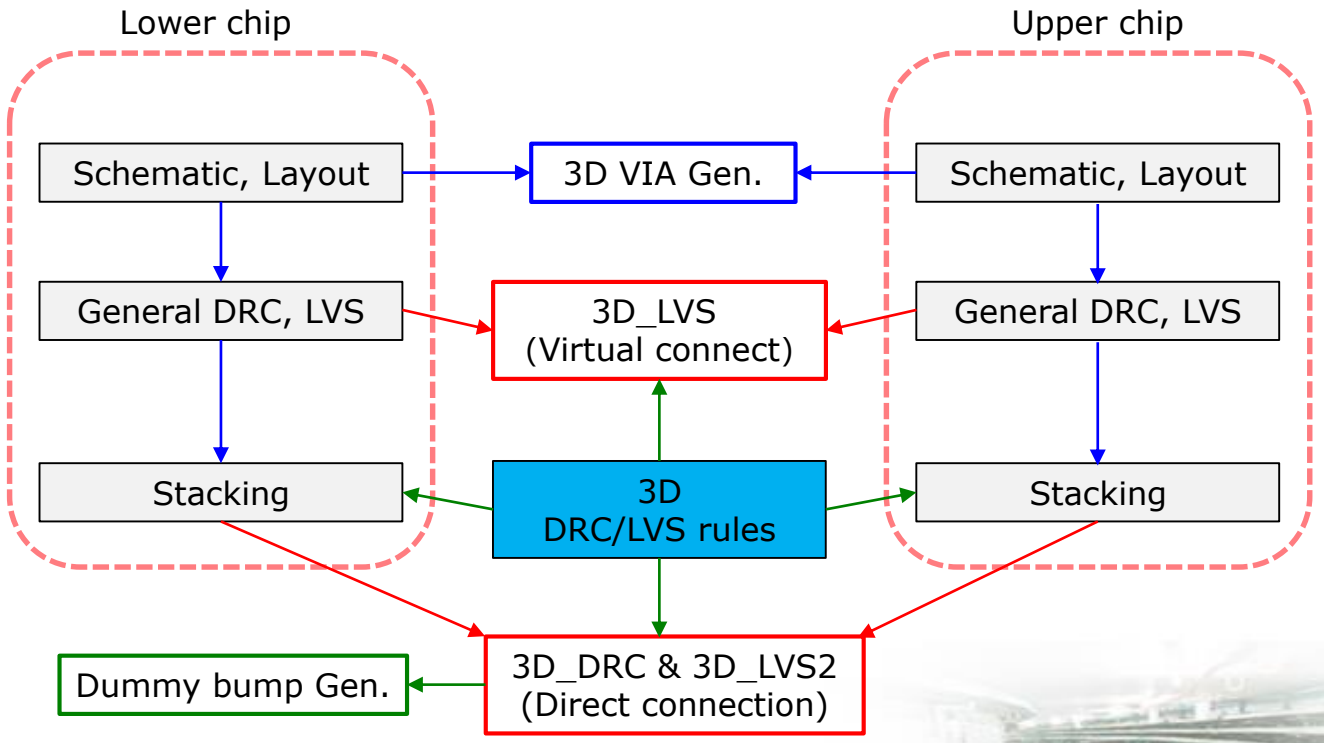
Design flow

- Conventional SOI tape-out plus a special 3D add-on process
  - 3D related **rules** integrated into the EDA tools
  - On the basis of single layer SOI design flow

stack-up of 3D layers

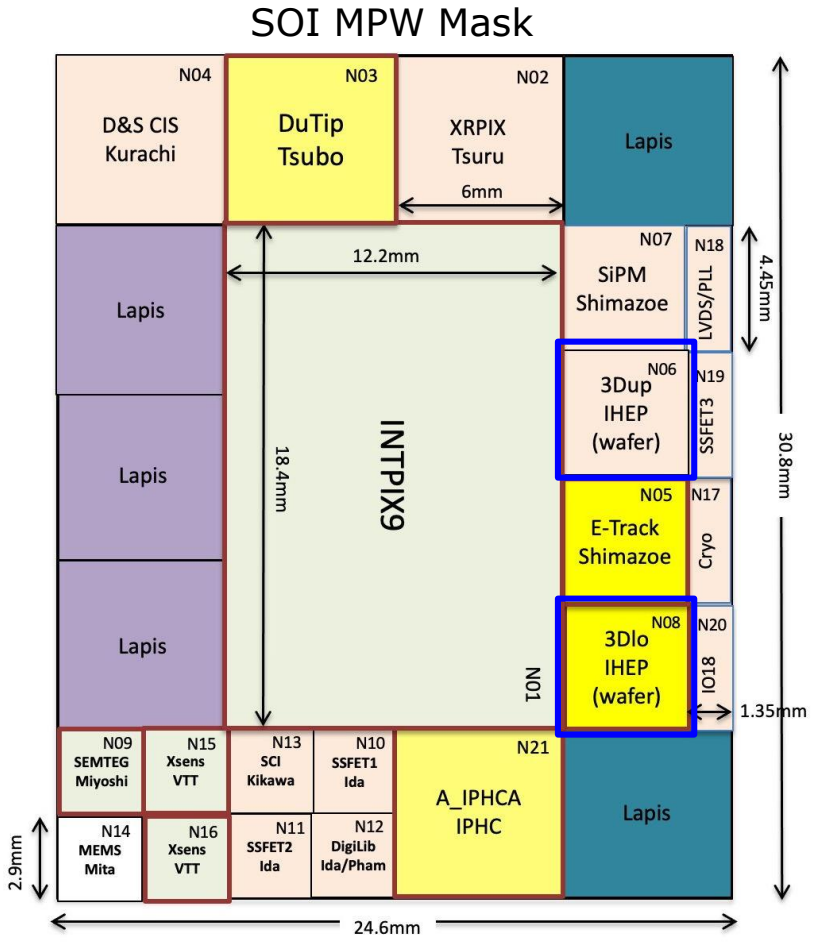


flow chart of SOI-3D design



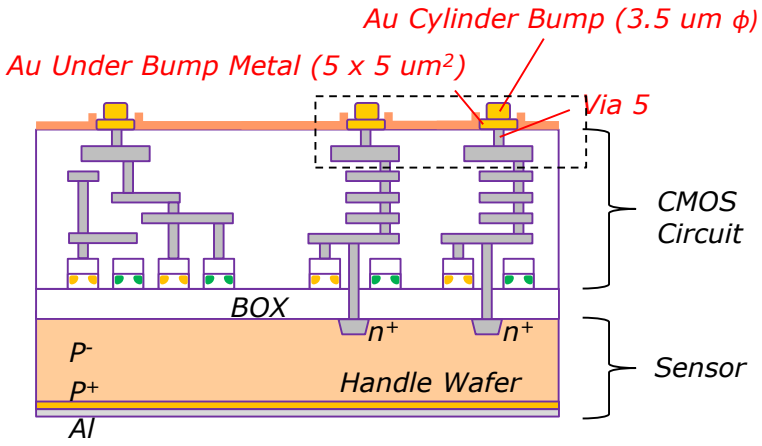
Chip-On-Chip bonding

- Tape-out at LAPIS and 3D-bonding at T-Micro
  - All the data stored in a single GDS file, including the 3D layers
- Multiple reticles firstly diced from a dedicated wafer (but still MPW)
  - for the formation of Via 5, UBM, Au-Bump
- Single chip diced again for
  - Stacking, Glue injection, Thinning, Bond pad

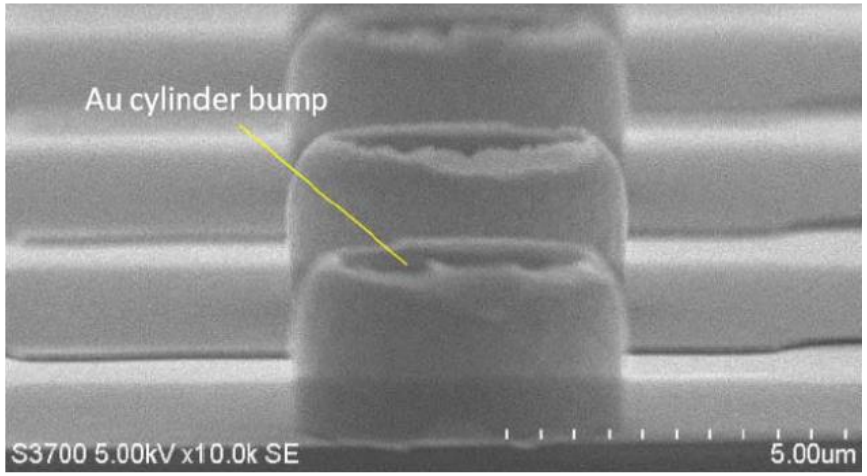


Micro bump

- Au cylindrical (hollow) bump on top of MET5 (top metal)
  - Thin wall of Au ~ 100 nm
  - **Bump resistance 0.3 ~ 0.4 Ω**
- Features large bonding margin and low temperature
  - Cylindrical bumps easy to deform (self-adapted to variation of bonding gaps)
  - Process temperature < 200 °C

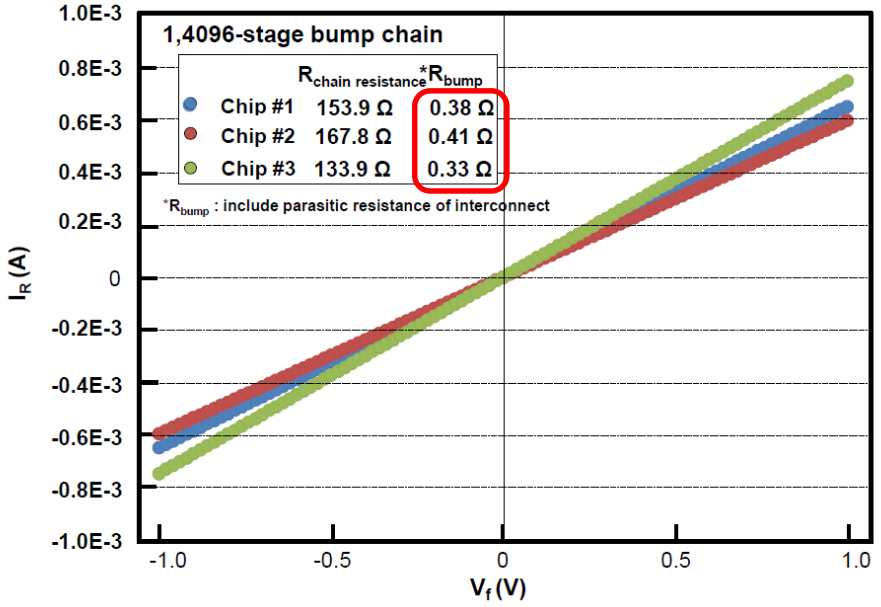


SEM image of Au micro-cylinder bump



Processed by T-Micro

Bump Resistance (0.3 ~0.4 Ω)



Design for test

- Configuration of Bond pads and IO buffers
  - Original bond pads remained on both lower and upper chips, **accessible before 3D integration**
  - Functional IO buffers always stacked up with dummy IO to avoid conflicts of buffers
- Internal signal waveform are routed out of test pixels with buffers for oscilloscope observation
  - **Critical node** in the analog front-end
  - Two-stage buffers: Source-Follower and Operational Amplifier

Configuration for the access to ***lower tier***(left) and ***upper tier***(right)