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3D-integrated pixel circuit for a low power and small pitch SOI sensor

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Targeting on low power consumption and high spatial resolution, the CPV-4 SOI pixel sensor requires about 100 transistors to implement the analog-digital mixed circuit functionality within a given pixel area around 16 um x 20 um. By utilizing 3D vertical integration, signal amplification and threshold discrimination are achieved in the lower-level circuitry, while hit information storage and sparse readout are achieved in the upper-level circuitry, thereby maximizing pixel size reduction and power consumption reduction. This work will present the pixel circuit design and the test results on the completed 3D chips.

Summary (500 words)

This work starts from the design challenges of the vertex detector for the future Circular Electron Positron Collider (CEPC) and introduces the main design constraints on the pixel sensor design. In the development of the Compact Pixel for Vertex (CPV) series of pixel sensors, a high spatial resolution implementation method is proposed, especially the overall solution of the CPV-4 chip using 3D-SOI design. Based on the conventional 200nm SOI pixel process, 3D-SOI technology adds a vertically stacked upper circuit layer and a high-density micro-bump array connection. This provides the technical conditions for reducing the pixel pitch while maintaining the pixel circuit function. The CPV-4 design uses a low-power analog front-end circuit placed in the lower tier, while hit information storage and sparse readout are placed in the upper tier, successfully reducing the pixel size to 17μm x 21μm. Currently, the lower tier and upper tier of the chip have been functionally verified and the first vertical integration trial has been carried out. The control of the lower tier and upper tier has been achieved on the completed 3D chip, and the successful 3D connection of the IO Pads has been verified. However, this was obtained on different 3D chips, and no single 3D chip has been able to control both the lower tier and upper tier simultaneously. Improving the yield of 3D integration seems to be very challenging.

This work provides an alternate technical route for achieving pixel sensors with extremely high spatial resolution. Compared with another technical route of shrinking the pixel pitch by reducing the size of transistors using the new generation of smaller CMOS process, this method has the advantages of depleted layer thickness and high signal-to-noise ratio, and is expected to meet the comprehensive requirements of the CEPC vertex detector for spatial resolution of 3μm, average power consumption of 50mW/square (cm), and time resolution of a few μs.

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