A low *crosstalk* 768-channel of 14-bit analog to digital converters for high resolution array of detectors.

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15 Years of constant effort


Xdigit
Extract the best signal
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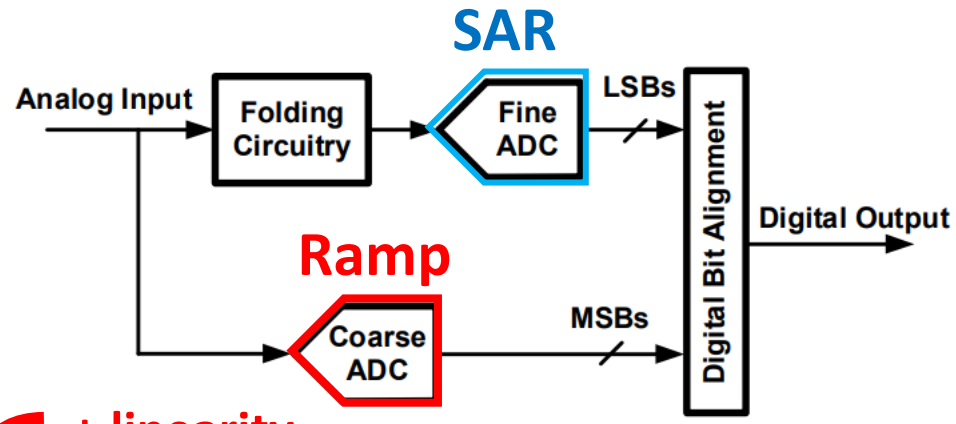
MASSAR is a patented hybrid architecture

This prototype is made on request in a ST H9A process (***0.5µm*** & 130nm digital)

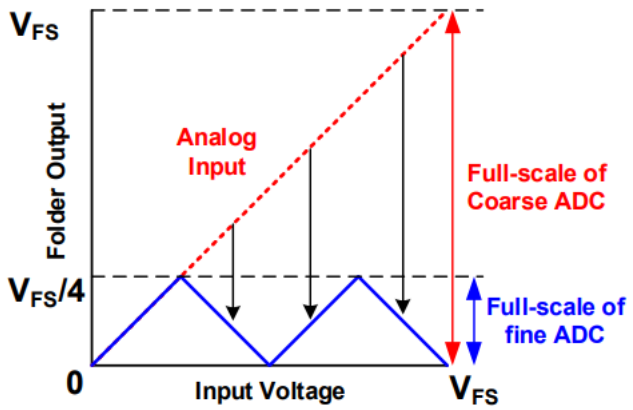
- 384 ADC in a pitch of 17µm for 3mm length
- But **2 inputs** signals are sampled instantly through each ADC channel, hence **addressing 2*384 = 768 columns of pixels 8.5µ large.**
- Each sampled signal is converted at the frequency of 40 KS/s but we could run faster (>100KS/s)
- The total power dissipation for each channel with all include, is 110µW

Schematic simulations in a 180n displayed a power dissipation reduced dowto 70µW

MASSAR ADC architecture & principle



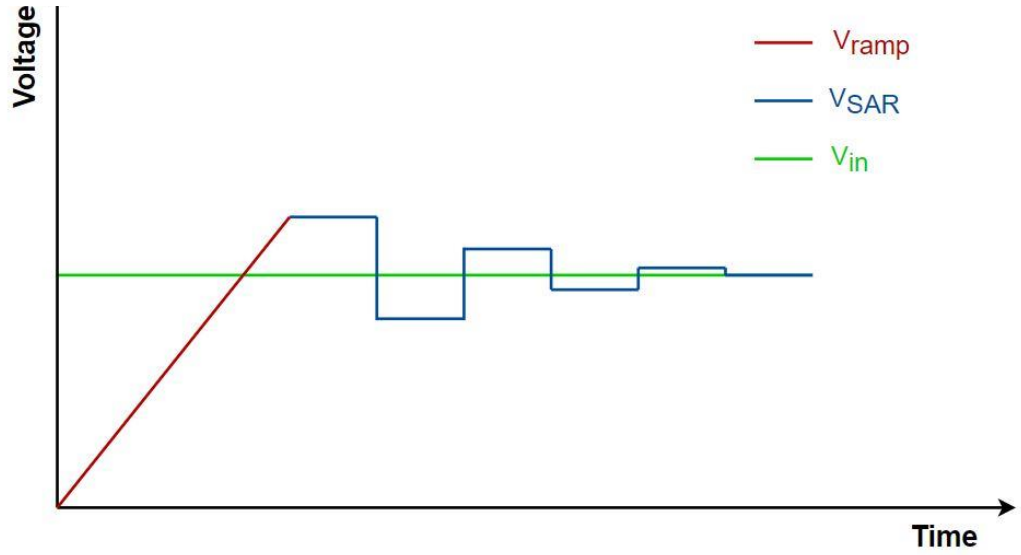
(a)



(b)

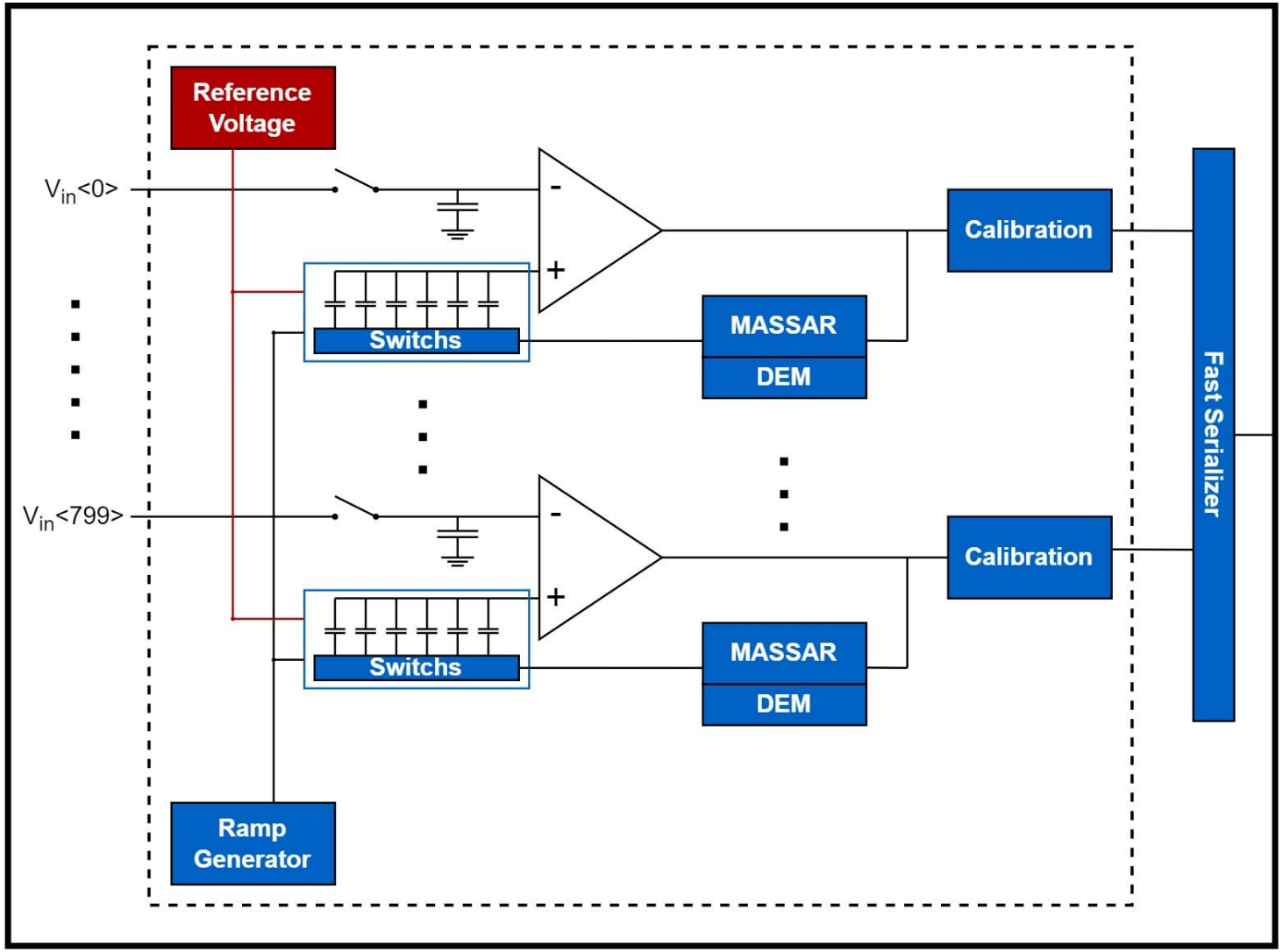
Ramp
- + linearity
- + monotonicity
- + Low pitch & low surface
- - Slow (2^N) clk

SAR
- + Faster (M*clk)
- - Mismatch issues
- - large surface (2^M *Cu)



MASSAR => 2^N + M CLK

MASSAR5 chip: Bloc diagram



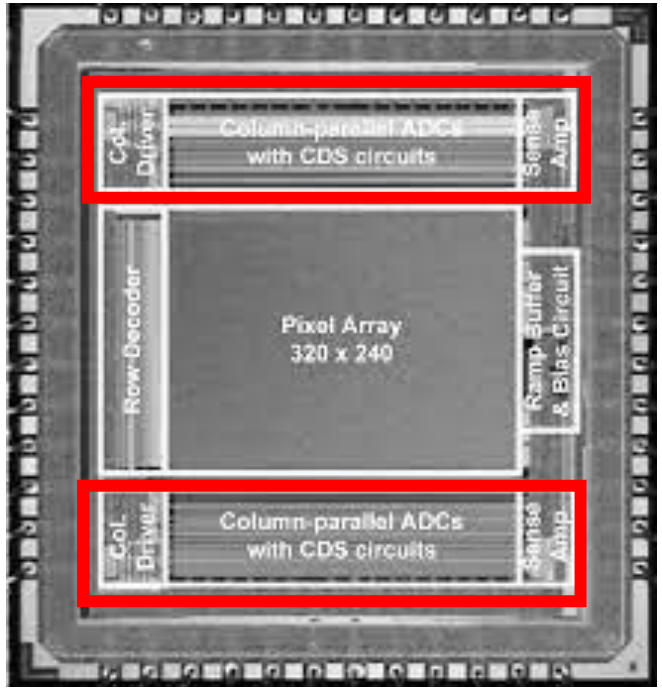
MASSAR: Goals & Challenges

- Our main goal was more than just to reach one channel high resolution ADC
- We targeted hendreds up to 2 000 channels of ADC
- We want to make it compatible with low pitch pixels
- We need to reduce the total power including rampe generator and reference voltages
- FPN (fixe pattern noise) and cross-talks are some of great issues, as well as clock distribution.
- We wanted the same layout to be reused for different sampling rate: **2^N + M clk**

2 different strategies of collaboration

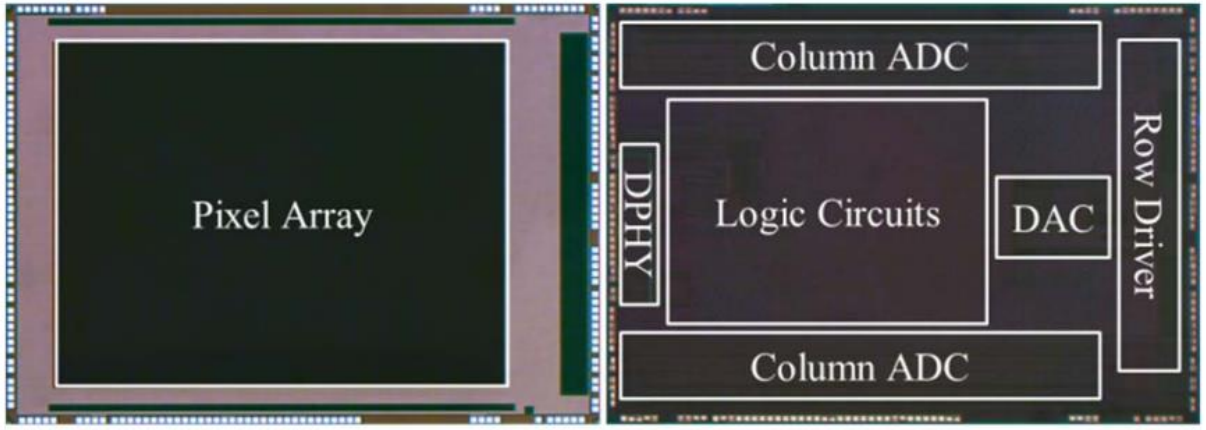
2D custom designs

- Process dependent
- Power optimized by design
- High level model + Layout XXL



3D custom products

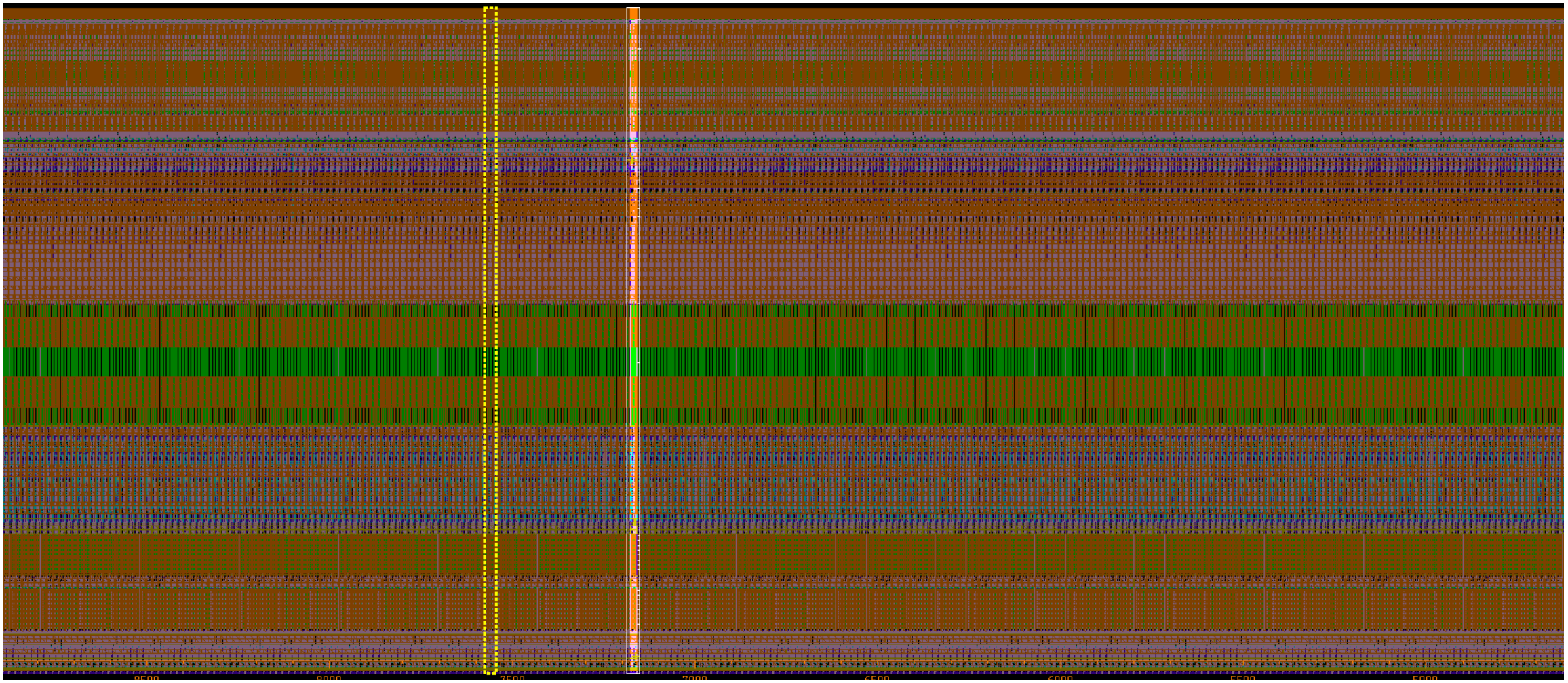
- 2 different chips stacked via TSV
- Power optimized by the aggresive process
- 3D processing cost but time saving



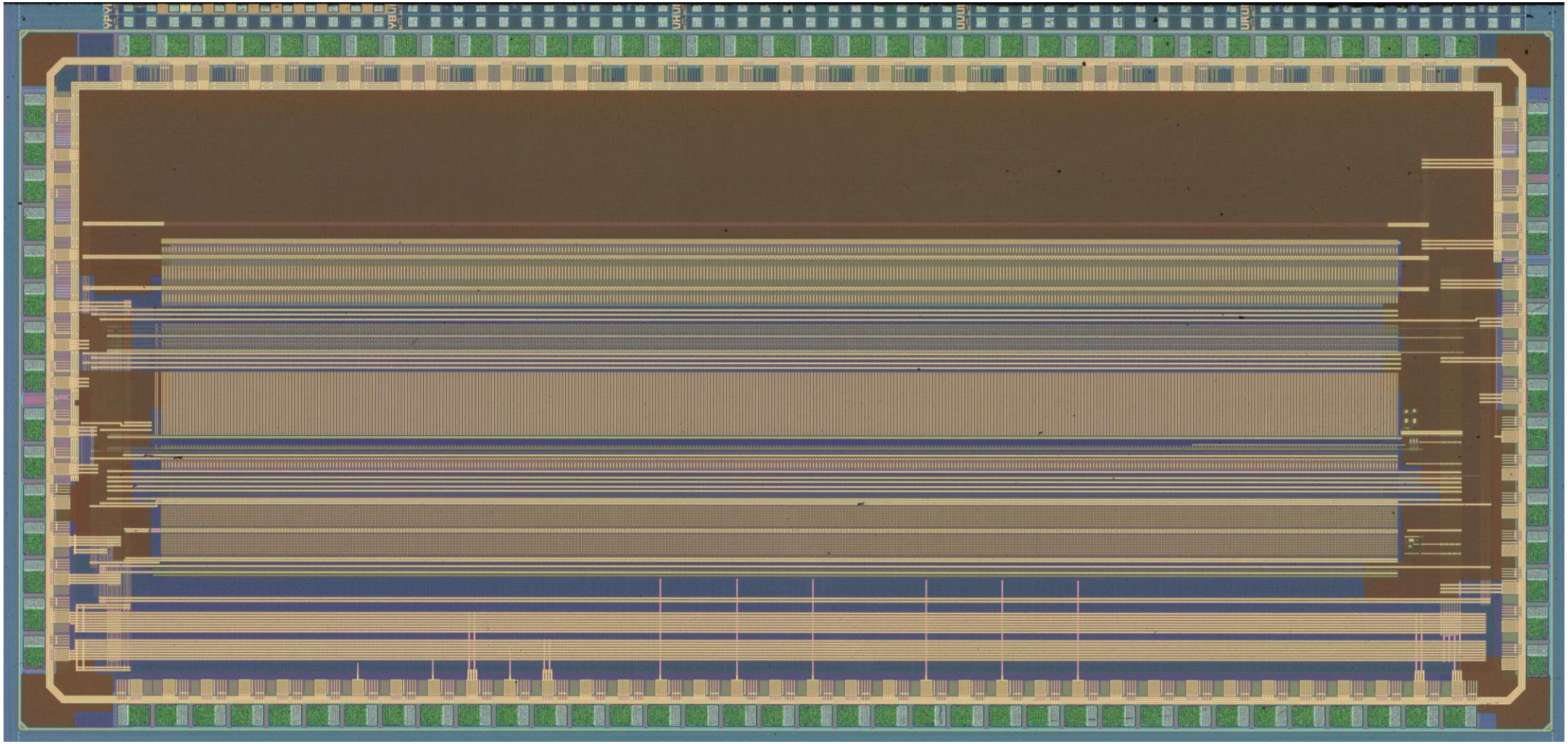
(a) Top chip (65nm) (b) Bottom chip (14nm)

Stacked CMOS Image Sensor, *Document Samsung Electronics, Hwaseong, South Korea*

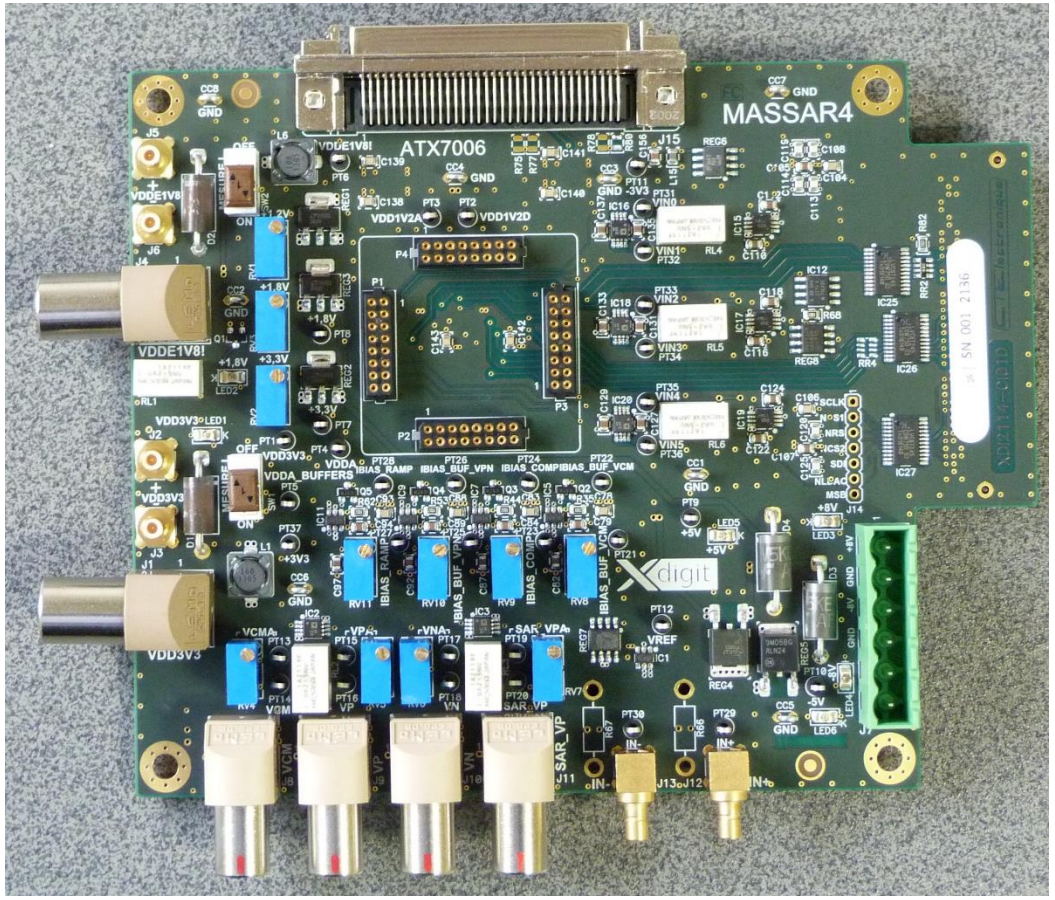
Layout screen shot: notice 1 channel shadow



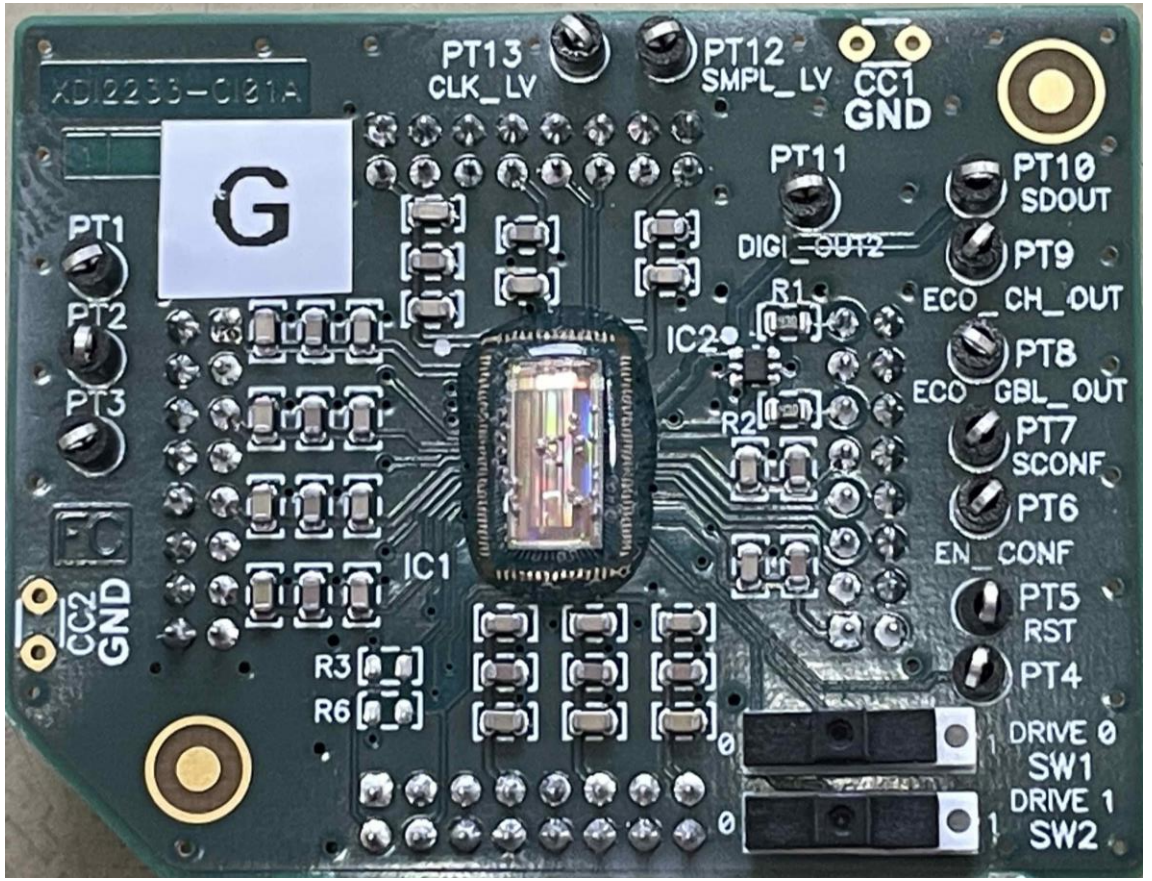
768 CH of MASSAR 14 bits 40KS/s; 6mm*4mm



Testing set-up MASSAR 5: hardware & software

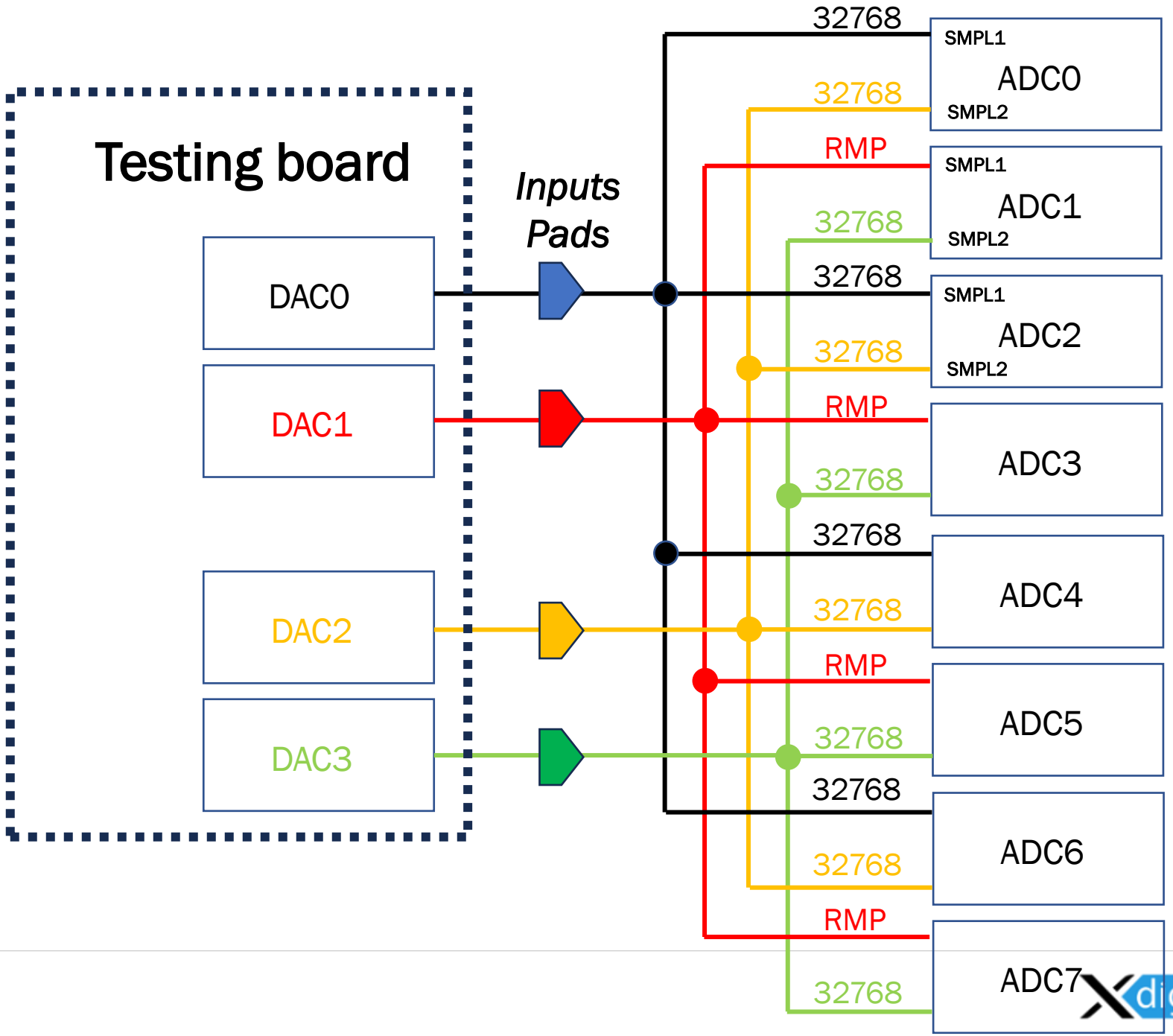


Mother board



Daughter board

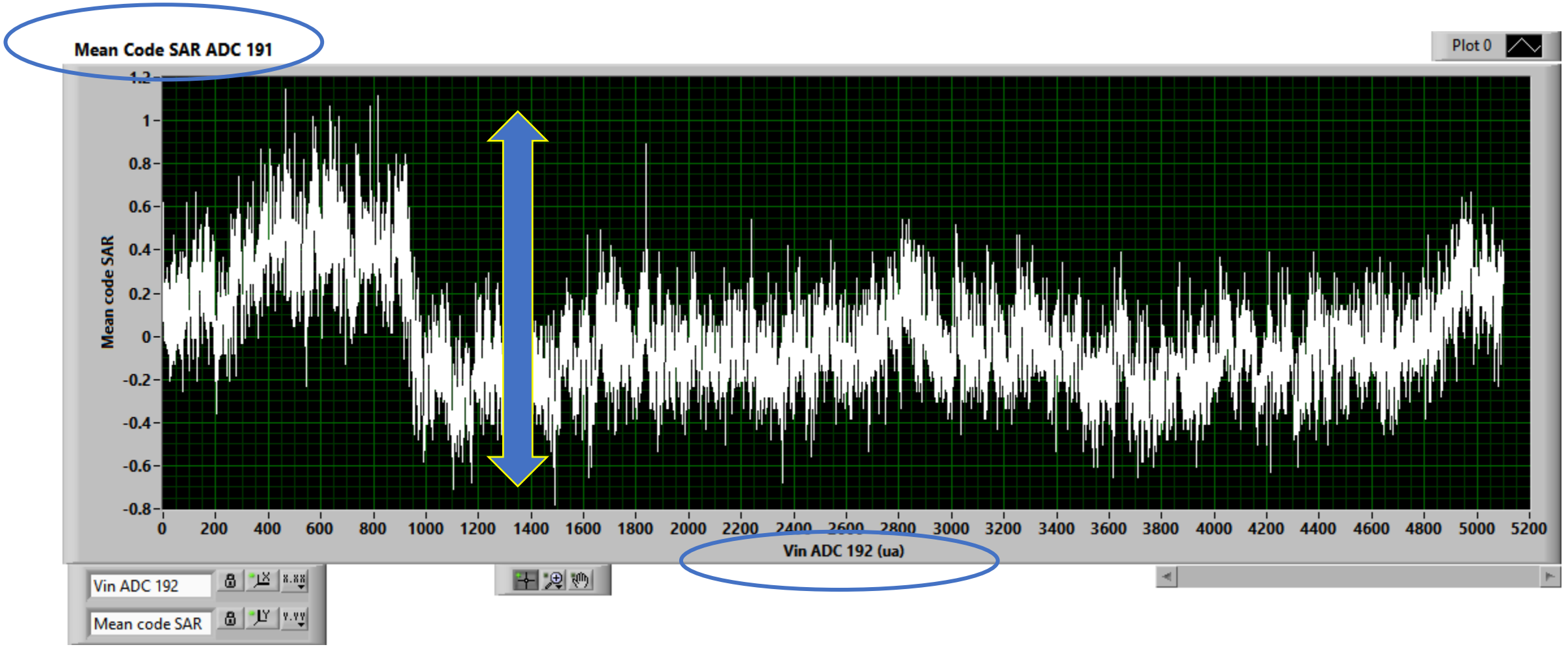
Chip on board 5


Testing board
Inputs Pads
DAC0
DAC1
DAC2
DAC3
32768
SMPL1
ADC0
SMPL2
32768
RMP
SMPL1
ADC1
SMPL2
32768
32768
SMPL1
ADC2
SMPL2
32768
RMP
ADC3
32768
32768
ADC4
32768
RMP
ADC5
32768
32768
ADC6
32768
RMP
ADC7
32768

MASSAR 5 testing results

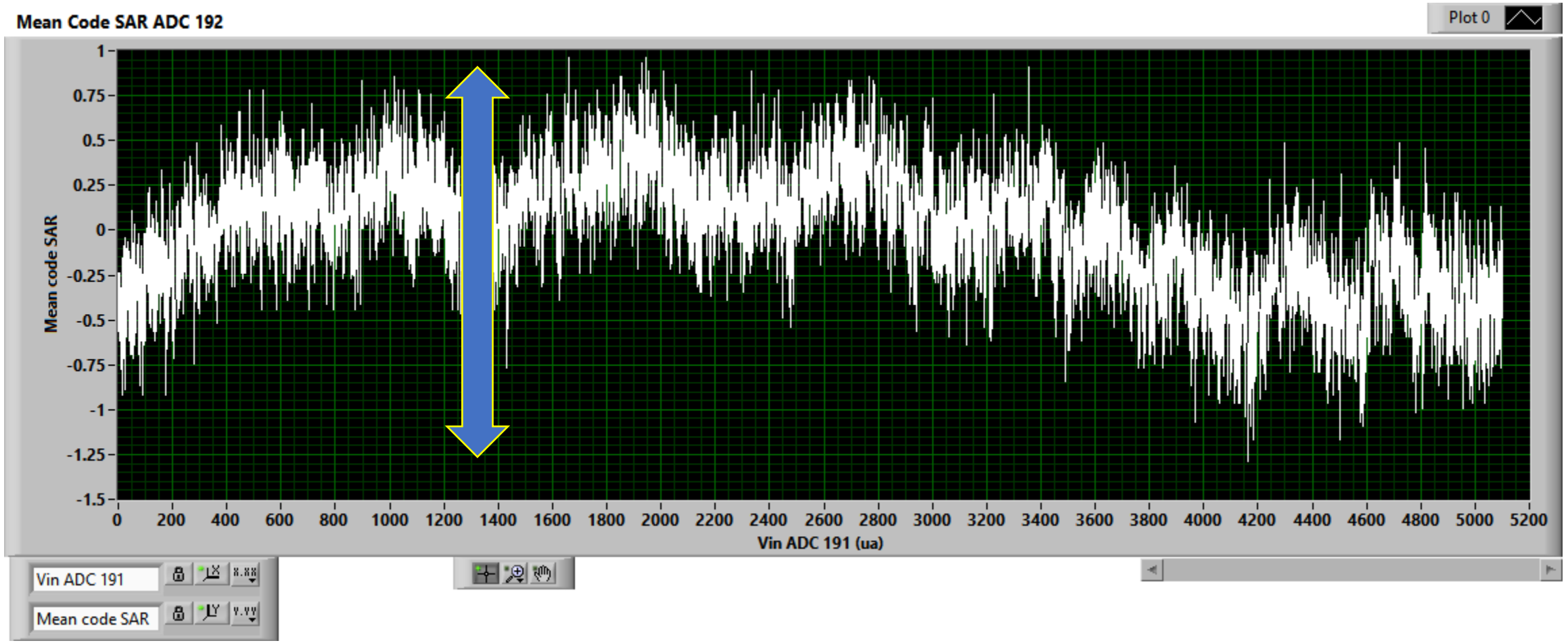
Cross-talk expressed as a dispersion over a average value= +/-1LSB

Code of channel 191 while nearby input 0V6 <-> 2V9 on Channel 192



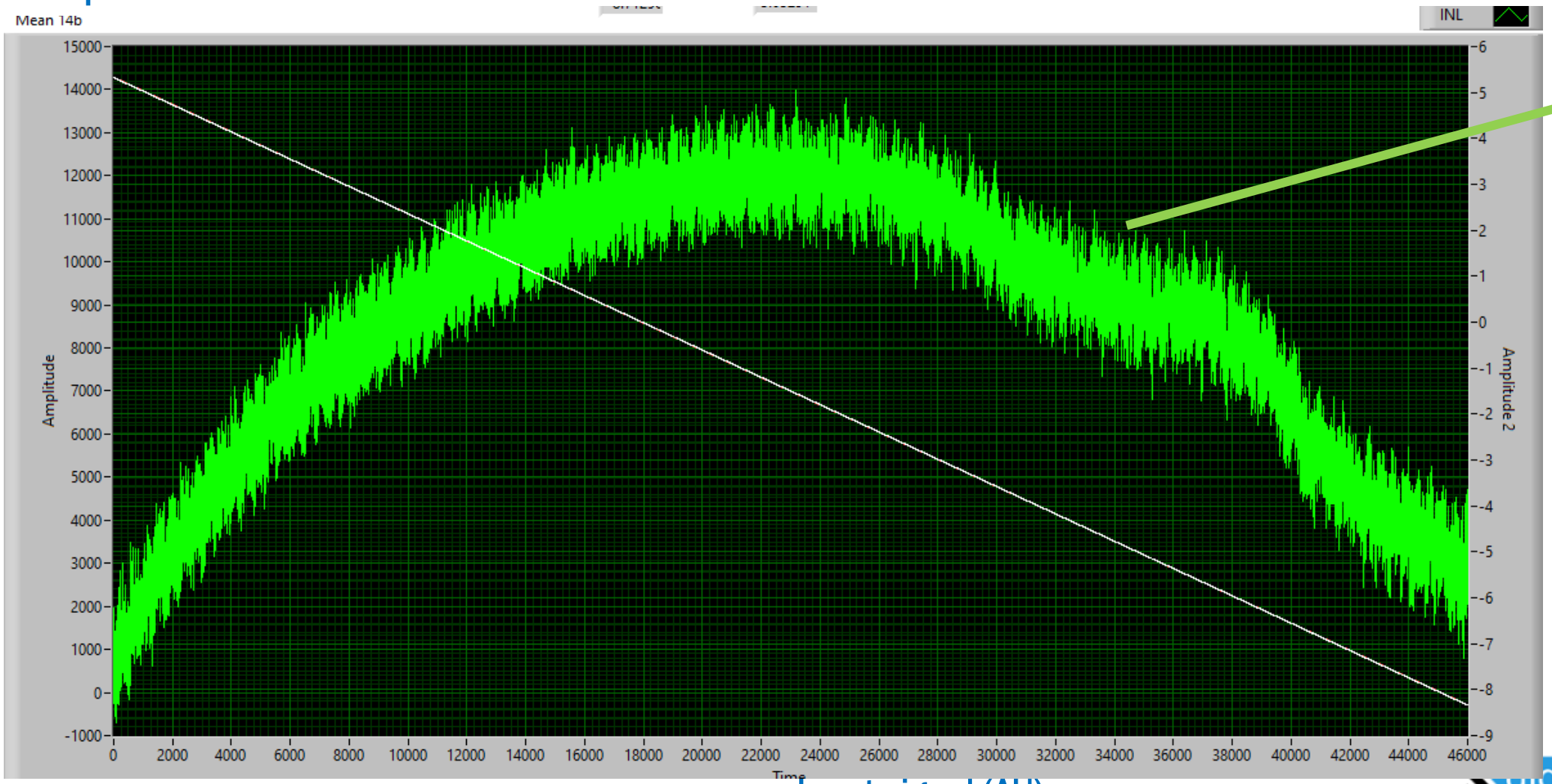
Cross-talk results n°2: +/-1LSB

Output codes on channel 192; while input 0V6 <-> 2V9 on Channel 191



Transfert curve & Linearity testing results

Output mean codes

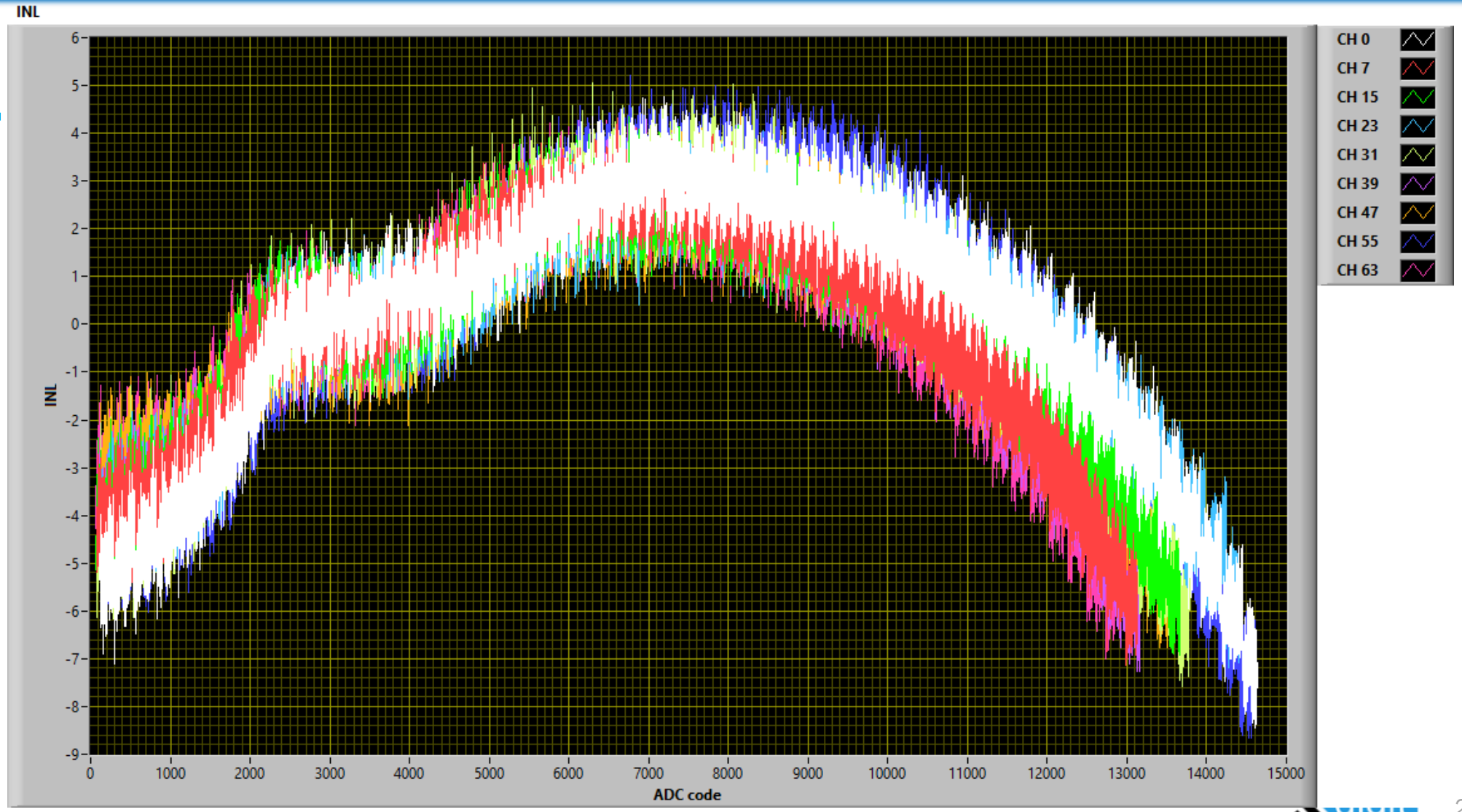


Linearity
INL (LSB)

Input signal (AU)

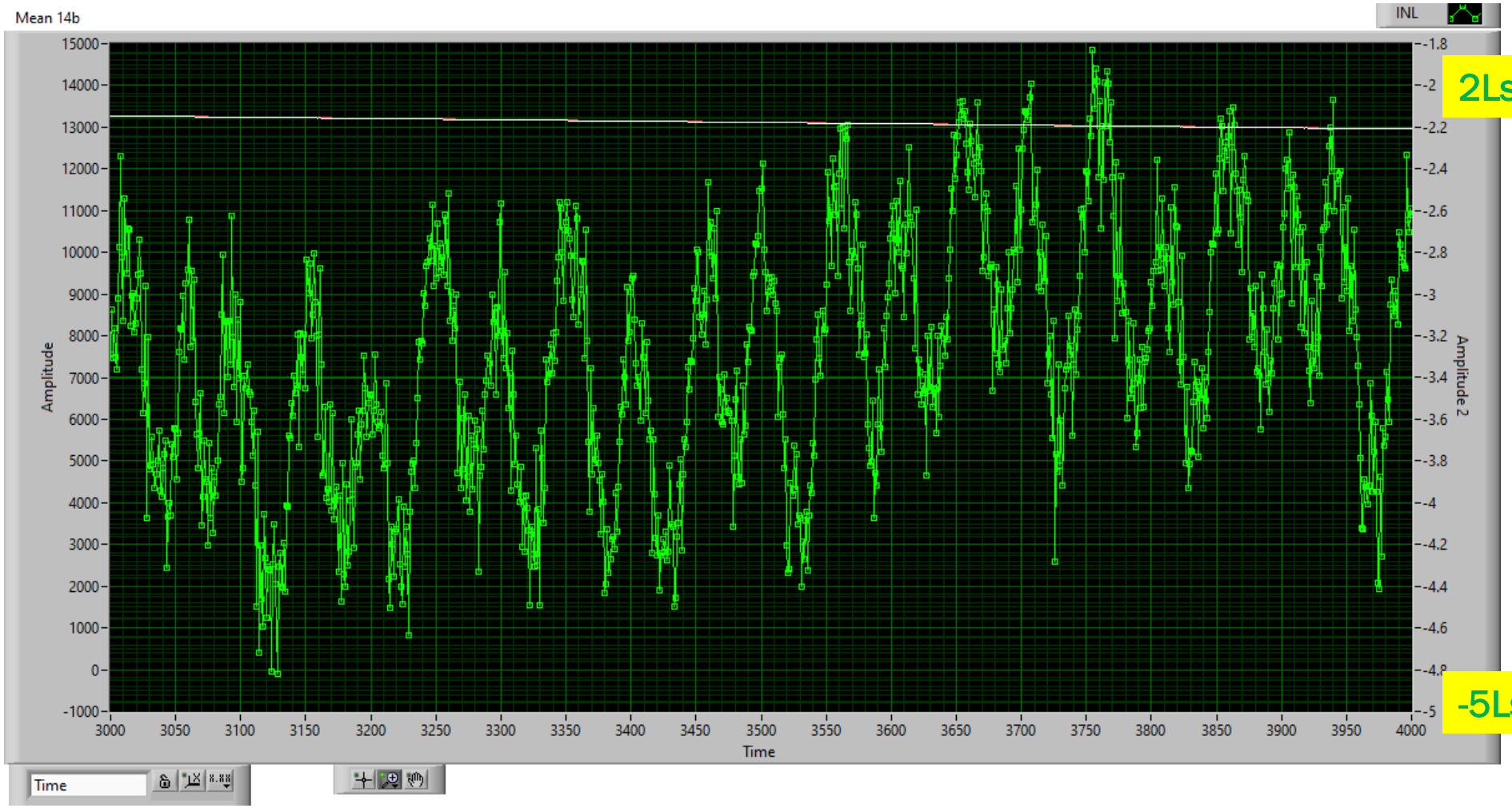
Linearity for different channels in the same chip

INL

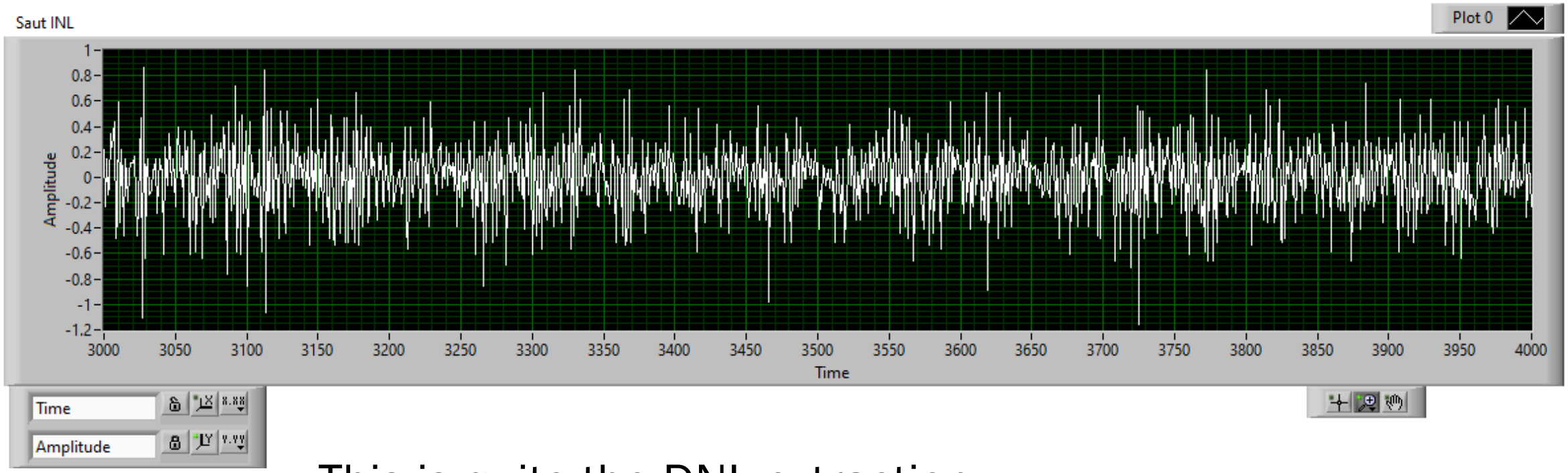


Linearity testing results: zoom on INL

Gap in linearity curve is limited



Gap along INL curve INL(n+1) – INL(n)



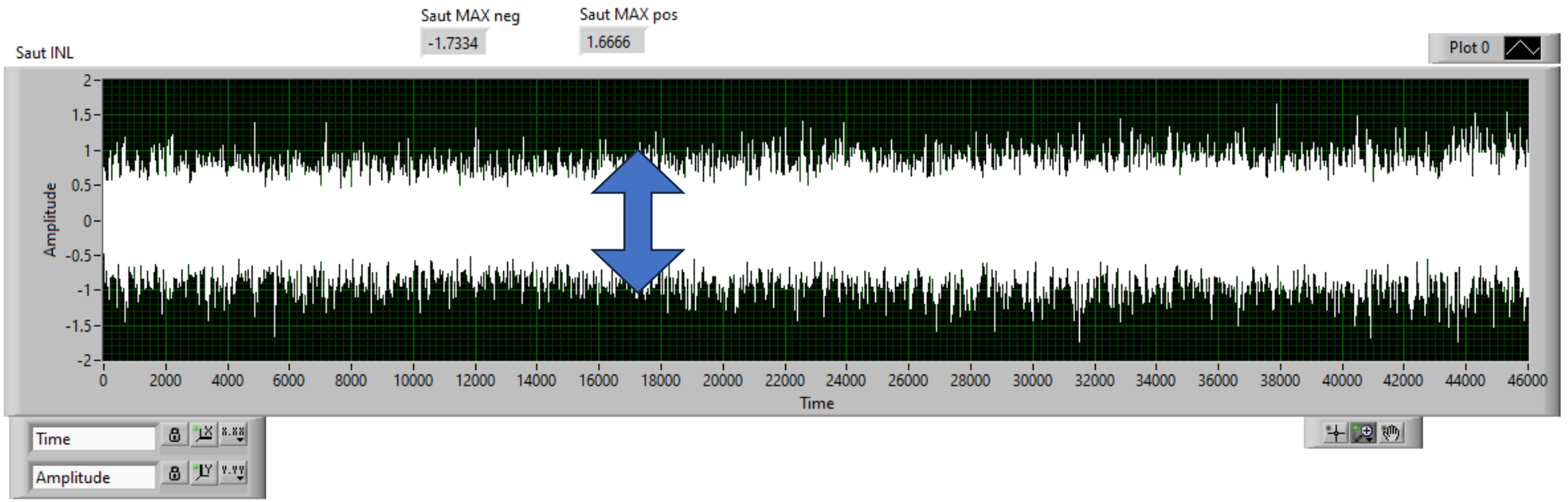
This is quite the DNL extraction

A few codes seem missing but

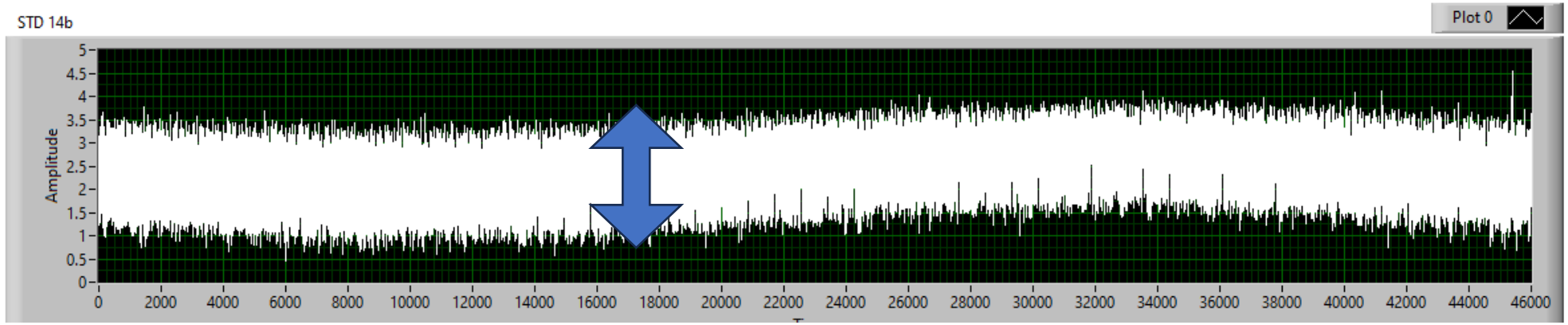
These will appear due to the DEM impact

Noise (1 to 3.5Lsb rms) & Gap in linearity (-1 to +1 LSB)

Gap of linearity
INL(n)-INL(n-1)



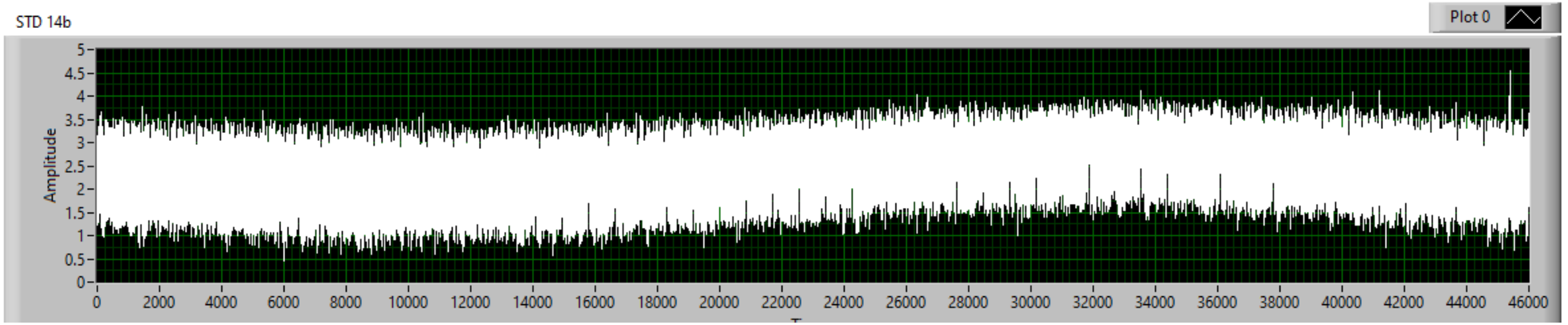
Noise(LSB rms)



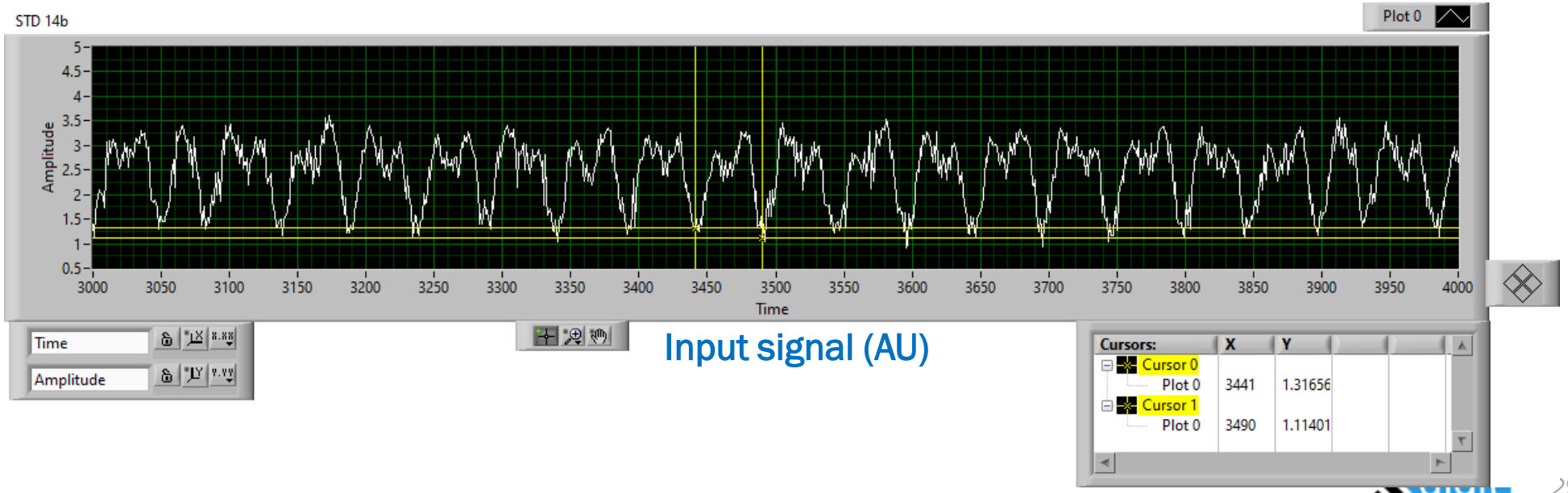
Input signal (AU)

Noise (3.5 Lsb rms) & Zoom on noise => modulation, this is identified as coupling in the layout so 1LSB rms is at hand

Noise (LSB rms)



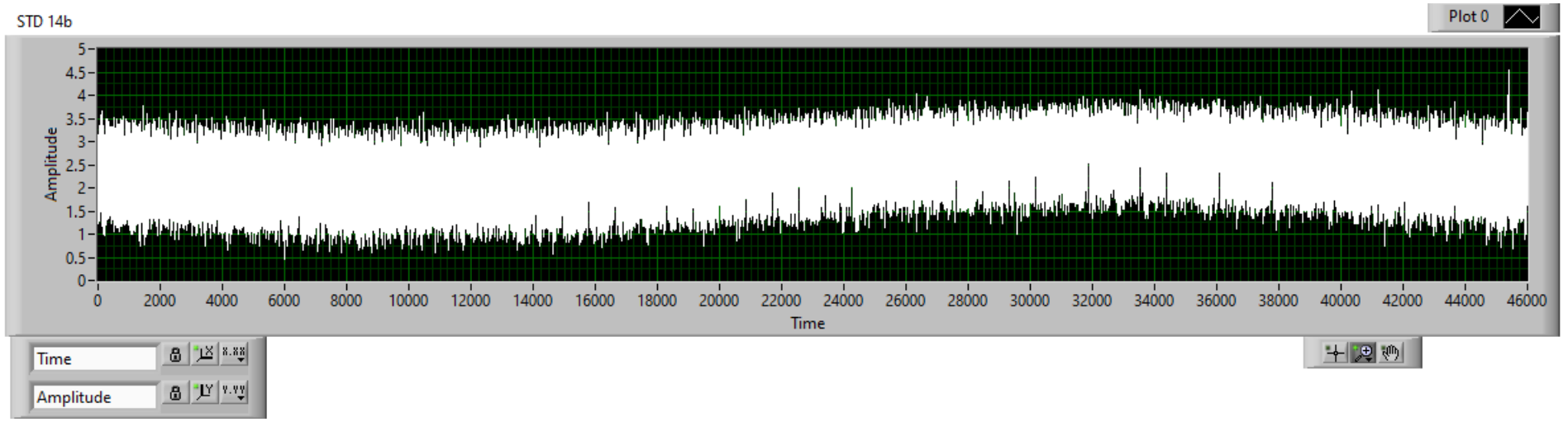
Zoom on Noise (LSB rms)



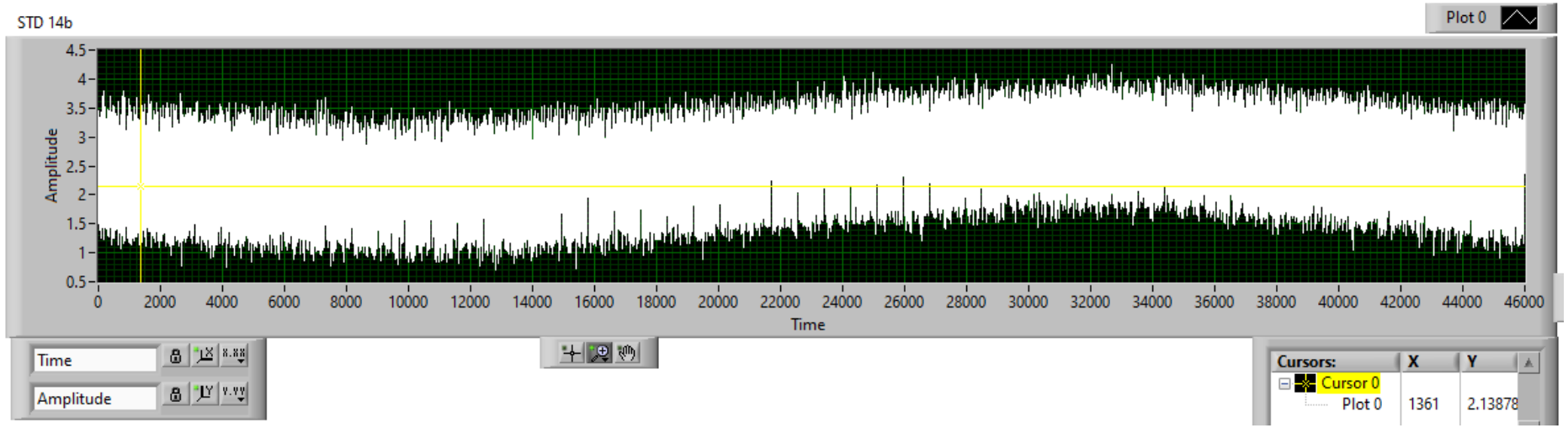
Input signal (AU)

Noise (if all ch converting) versus when only 1 CH is working => No increase

Noise (LSB rms)
ALL ch working



Noise (LSB rms)
Only 1 ch working



Conclusions

- MASSAR is now a ***mature***, ***optimized*** and ***flexible*** column ADC for HR sensors
- Results displayed a leading edge **figure of merit** (speed/power)
- The speed of this prototype can be increased beyond 100KS/s
- A last coupling issue is idendified and now removed for our next iteration
- This noise modulation dominated the noise feature, so DEM is not evaluated.
- We have the « know how » for larger frame design: 1024 ch
- Scaling to 65nm would help to reduce more the power dissipation.