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A low crosstalk 768-channel of 14-bit analog to digital converters for high resolution array of detectors.

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This paper reports the design and measurement results of a 768-channel of 14-bit analog to digital converters. Each channel's layout pitch is only 8.5µm with a sampling rate from 40KS/s up to 100KS/s. Testing results show a crosstalk about only +/- 1 LSB. The architecture of the circuit and the structure of the layout make it extensible to exceptionally large format of detectors beyond 1000 channels. The circuit is produced to be used as a side element for multi-channel readout systems or alternatively as an IP to be transferred inside very dense integrated circuits.

Summary (500 words)

For many physics and photonics applications, silicon detectors are increasingly used, and their density will continue to grow for next generations. This creates the need of very dense readout circuits in which the analog to digital stage will play a crucial role. The reduced pitch makes the layout particularly challenging for high resolution mixed signal circuits as converters. We report here the results of 14-bit array of analog to digital converters compatible with pixels'pitch of 8.5µm. The crosstalk is measured about +/- 1 LSB. This hybrid architecture of converter dissipates in total 110µW/channel when sampling at 40KHz rate. Each channel includes its own reference voltage buffers. This strategy paves the way for more dense arrays beyond one thousand channels of 14-bit resolution in the future. This prototype was produced in a 130nm process, and the total surface of the die is 6mm*4mm. The integral non-linearity (INL) is +5/-9 LSB over a single-ended dynamic range from 0.6V to 2.9V with a power supply of 3.3V. The noise is less than 4 LSB rms when all the channels are fully working. We show the die photograph in an additional document.

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