Performance of H2GCROC3, the readout ASIC of SiPMs for the back hadronic sections of the CMS High Granularity Calorimeter.

CMS collaboration

G. Bombardi, F. Bouyjou, E. Delagnes, P. Dinaucourt, F. Dulucq, M. El Berni, M. Firlej, T. Fiutowski, **J. González**, F. Guilloux, M. Idzik, C. de La Taille, A. Marchioro, J. Moron, L. Raux, K. Swientek, D. Thienpont, T. Vergine

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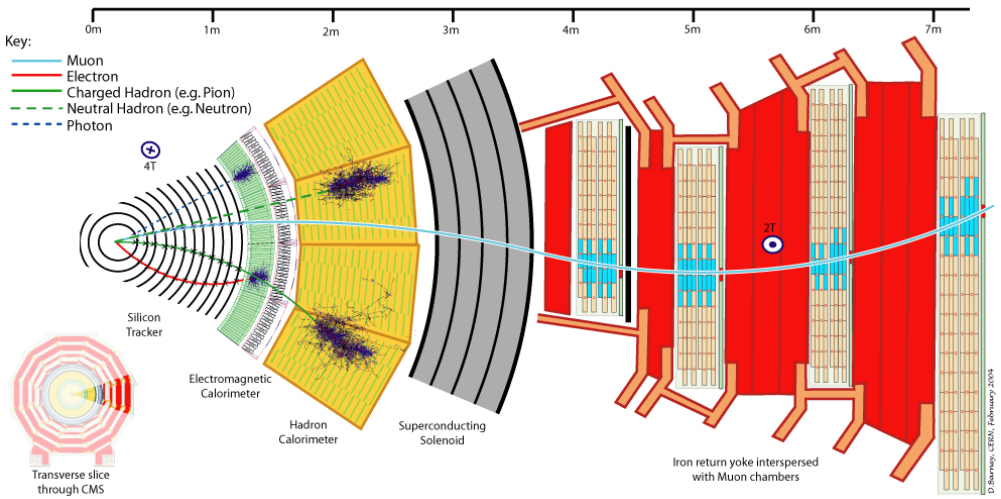
Organization for Micro-Electronics desiGn and Applications

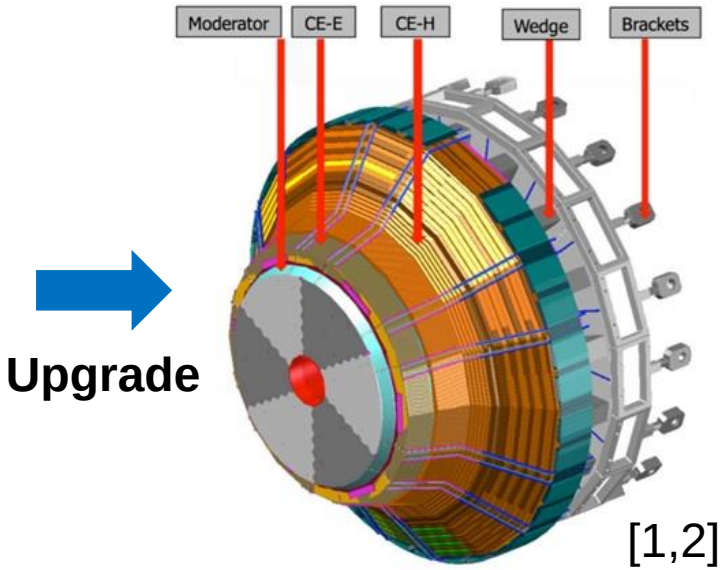
Outline

- **Introduction: HGCAL**
- **HGCROC**
  - Requirements and Architecture
- **H2GCROC: SiPM version**
  - Requirements and differences
  - Analog channel overview
  - Calibration mode
    - Setup
    - SiPM oscilloscope measurements
    - Single-photon-spectrum
  - Physics mode
    - Setup
    - Measurements
  - Irradiation campaigns and test beam
- **Conclusions**

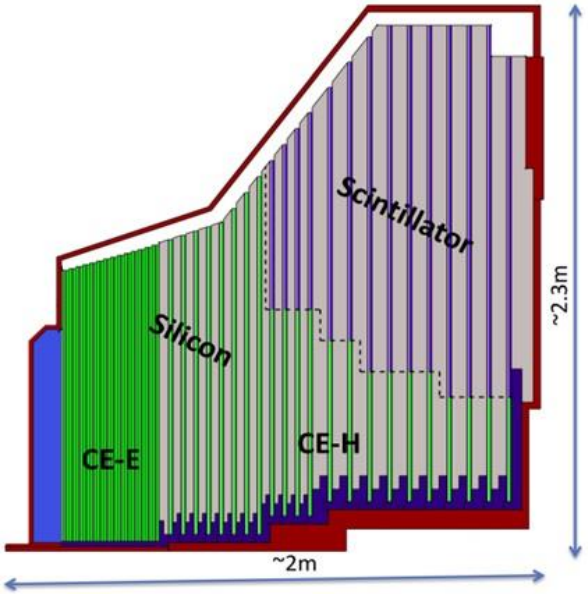


[3]

**Present endcap calorimeter will not work beyond Run3*



[1,2]



[5]

	CE-E Silicon	CE-H Silicon	CE-H Scintillator	Total
HGCROC	60 324	31 596	8 496	100 416
Motherboards	5 004	2 556	384	7 944
Bidirectional data/control links	5 004	2 556	384	7 944
Trigger links	4 020	2 556	768	7 344

Requirement: Use very similar FE electronics for the readout of both detectors

- Si (~ 4 fC / MIP)
- SiPM-on-tile (~ 1.7 pC / MIP) [2]

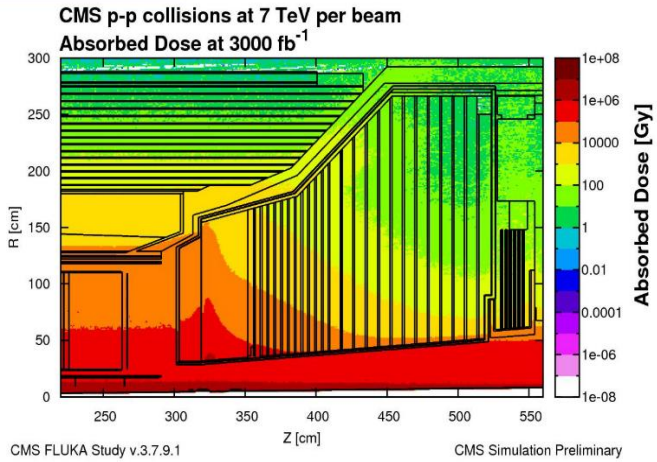
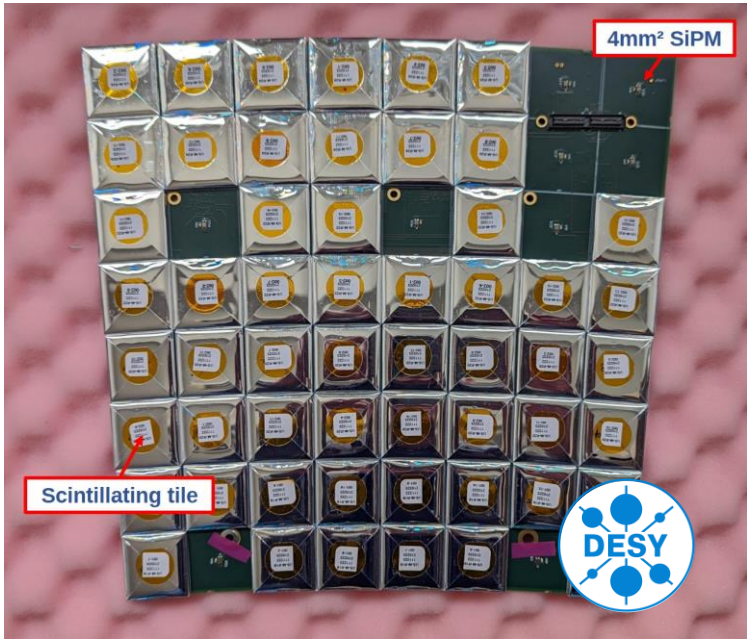
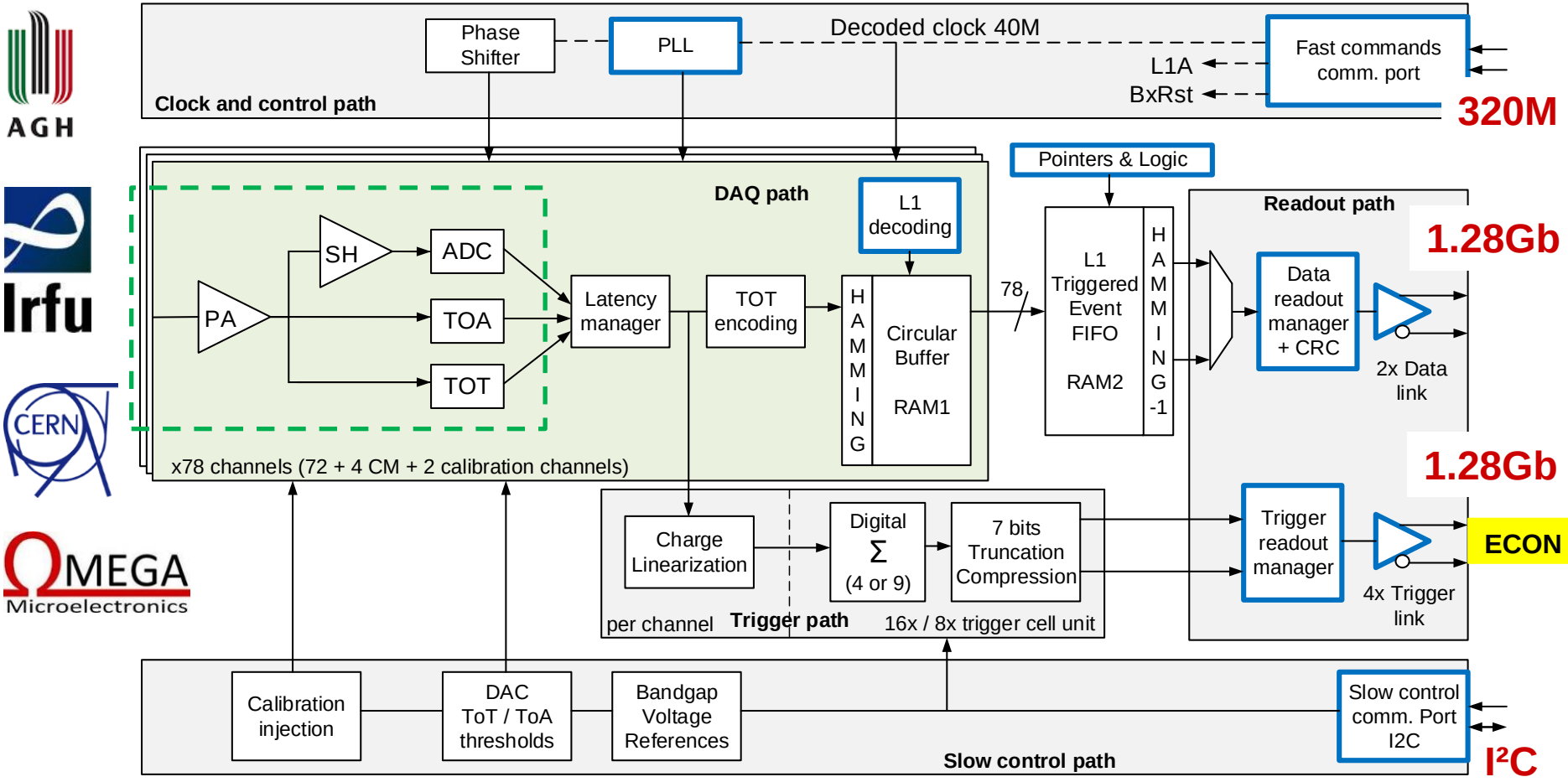


Figure 1.1: Dose of ionizing radiation accumulated in HGCAL after an integrated luminosity of3000 fb^{-1}, simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z.

[2]



HGCROC3: Architectural overview



Measurements

*Next talk: by ***Cristina Mantilla***
*Tomorrow talk: by ***Raghunandan Shukla***

- **Charge**
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.25% full range resolution. TOT: 0.025% full range resolution
- **Time**
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

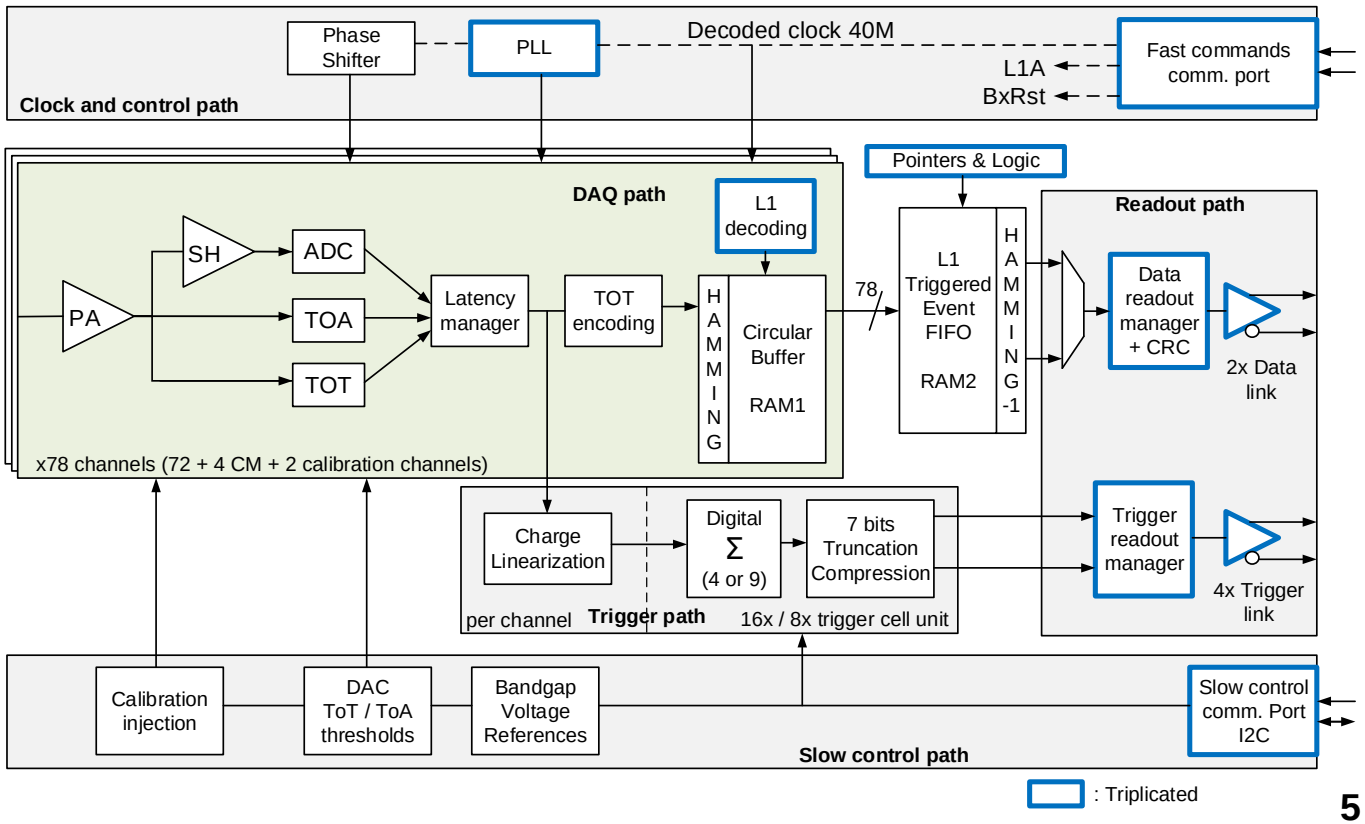
HGCROC: Si version. Requirements

Requirements for HGCROC (The Si version of the ASIC):

- 1.2V power supply for the very front-end
- Charge dynamic range: **0.2 fC to 10 pC**
- Timing accuracy **< 100ps for pulses above 3 MIPs (12fC)** for a $C_{det} = 65pF$
- Compensation of the leakage current up to **50µA**
- Radiation resistance up to **200 MRad**

Friday talk by **Fakhri Alam Khan*

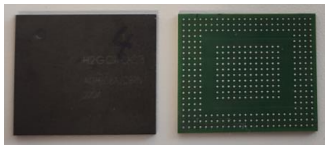
HGCROC3:
High density [4]



H2GCROC: SiPM version. Requirements

Requirements for H2GCROC (The SiPM version of the ASIC):

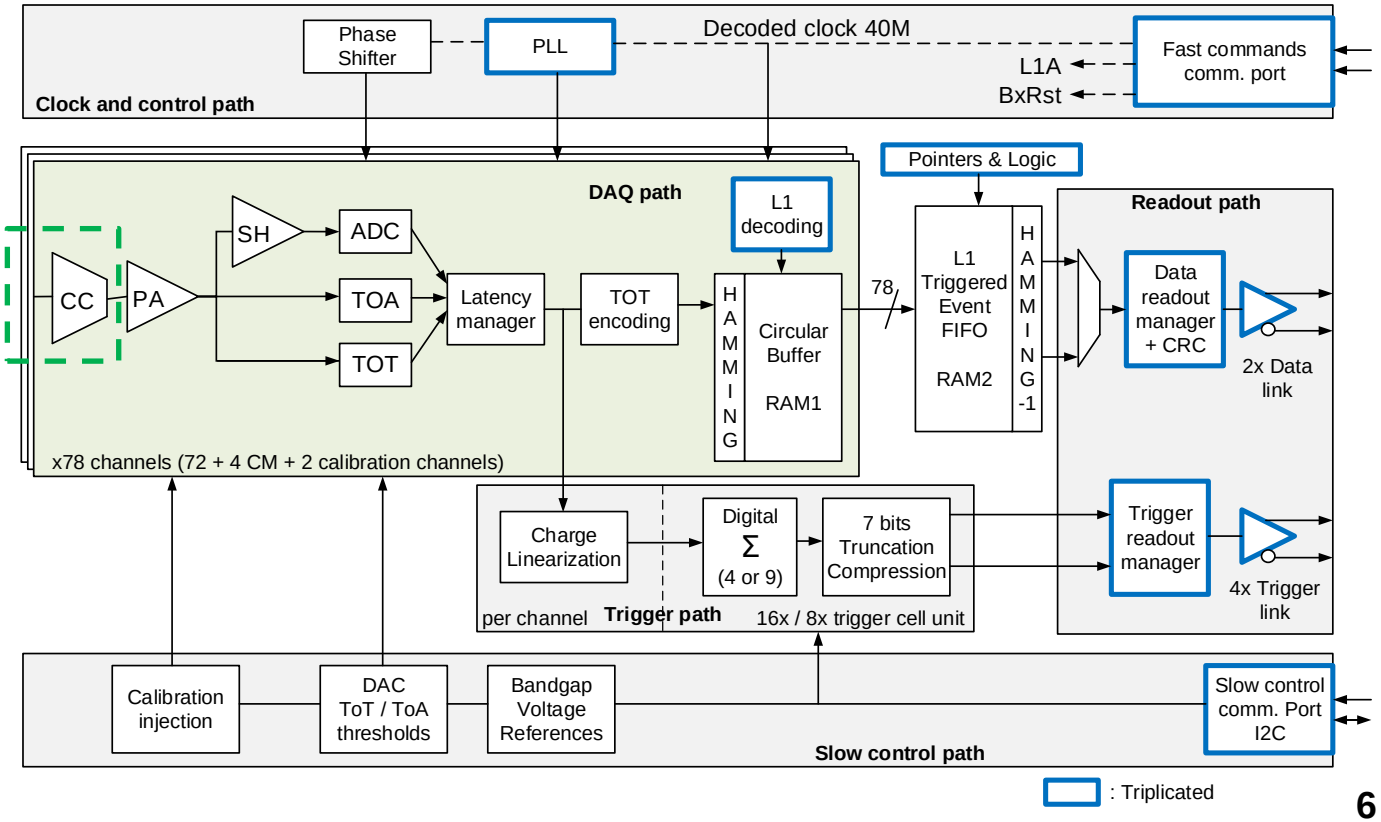
- 2.5 V power supply for the very front-end to cope with SiPM bias voltage
- Charge dynamic range : **160 fC to 320 pC**
- Timing accuracy **< 100ps for pulses above 3 MIPs (4.5pC)** for a $C_{det} = 100pF$
- Compensation of the leakage current up to **1mA**
- Radiation resistance up to **300 kRad**
- **Input DAC** to tune the input voltage in order to compensate for breakdown voltage fluctuation



H2GCROC3:
Low density

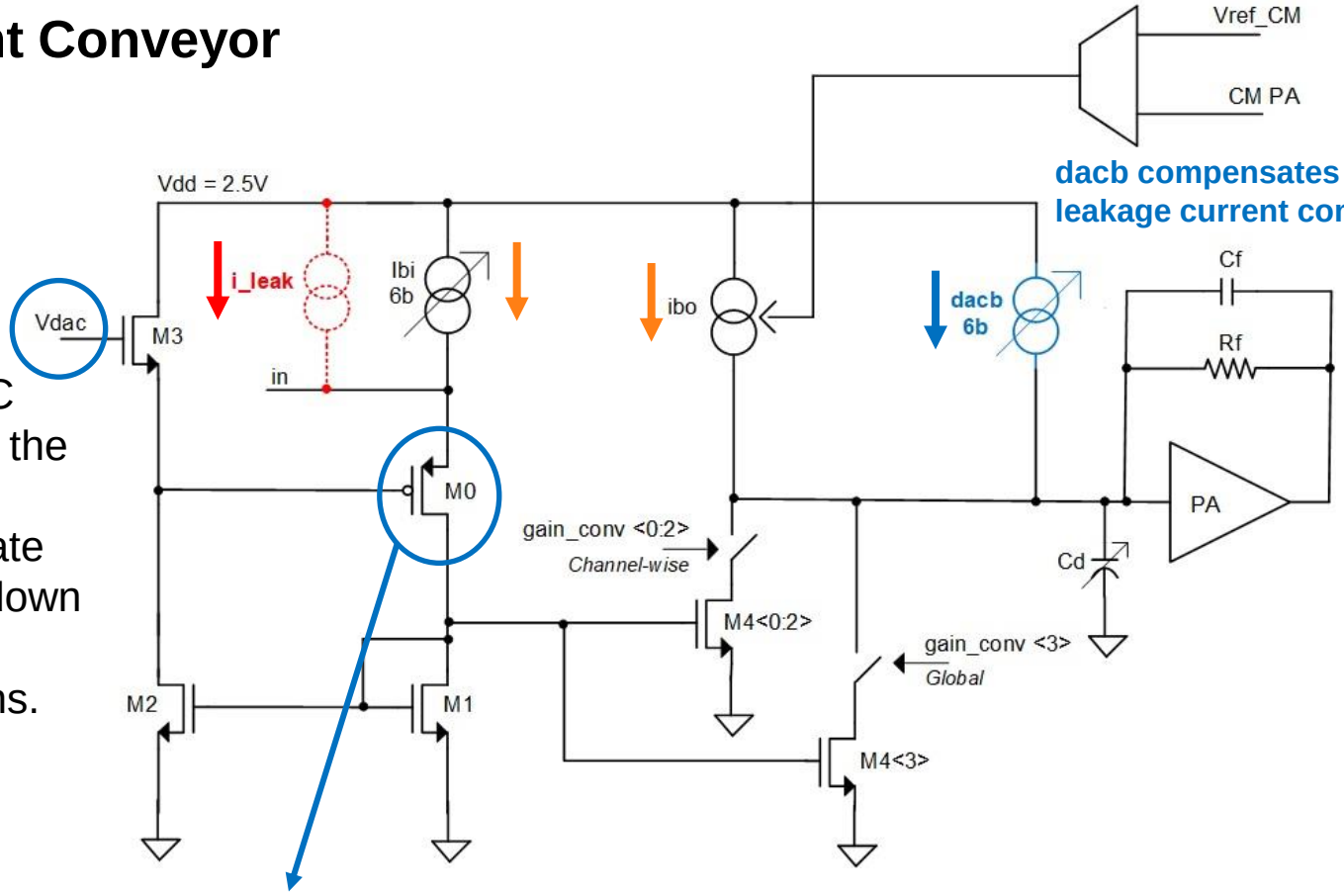
Current Conveyor
based on KLAUS chip from Heidelberg UNI. [6]

Attenuates the current at the input with 4 bits.
CC gain:
0.025 to 0.375
(step 0.025)



H2GCROC: Analog channel overview

Current Conveyor



dacb compensates up to ~1.2mA leakage current coming from the SiPM

Tuning DC voltage at the input to compensate for breakdown voltage fluctuations.

Current mode feedback to increase the gm

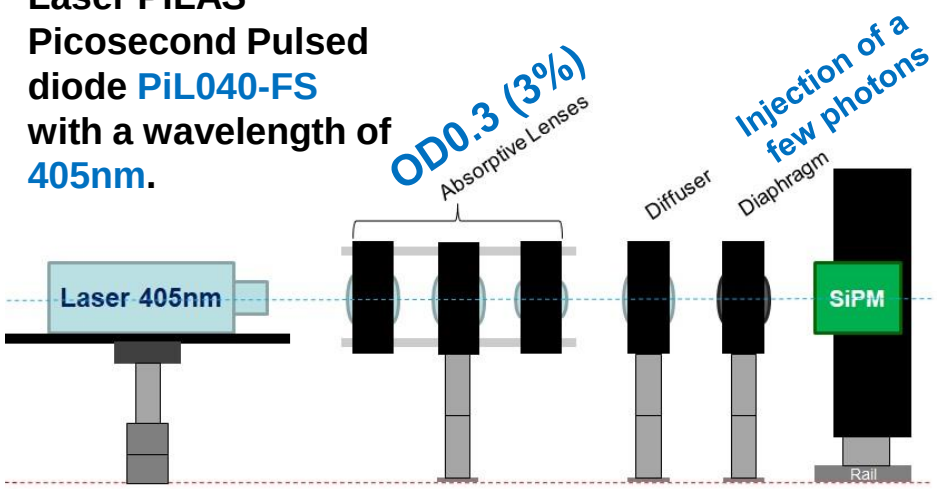
CC gain = 0.025 to 0.375 (step 0.025)

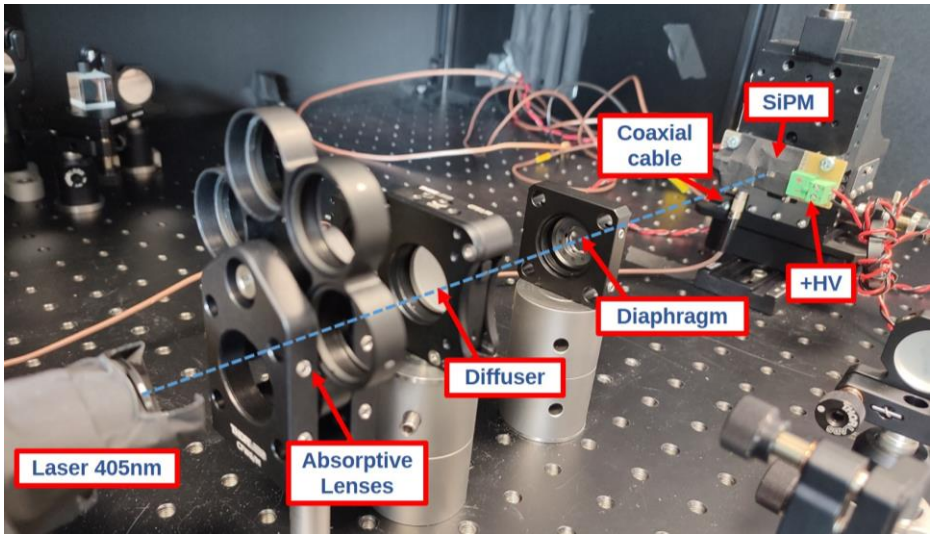
[4]

- **2 typical gains**
  - High gain (Calibration mode): **4-7 fC/ADC gain, 9-20 fC noise**
  - Low gain (Physics mode): **16-23 fC/ADC gain, 20-35 fC noise**

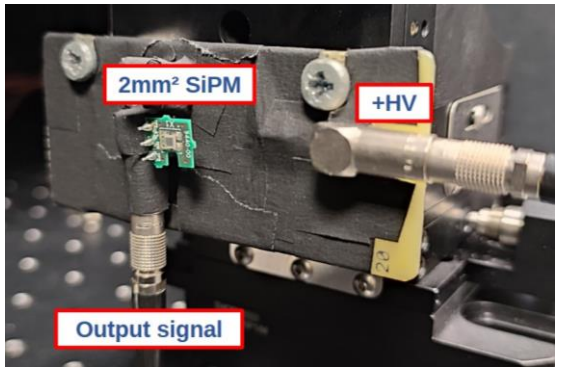
Calibration: Photon injection setup

Laser PILAS Picosecond Pulsed diode PiL040-FS with a wavelength of 405nm.

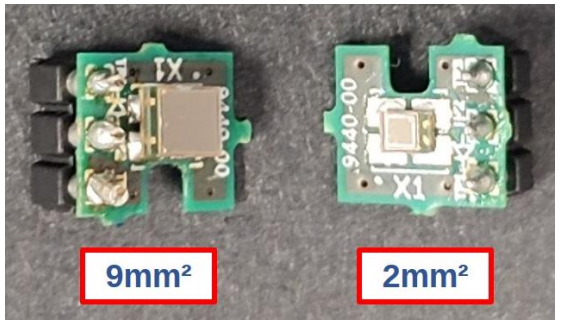




- **SiPM sizes in HGCAL** were considered to be **2mm²** and **4mm²**.
- Radiation damage to scintillators and increased noise in irradiated SiPMs have led to use **9mm²** SiPMs in certain regions.

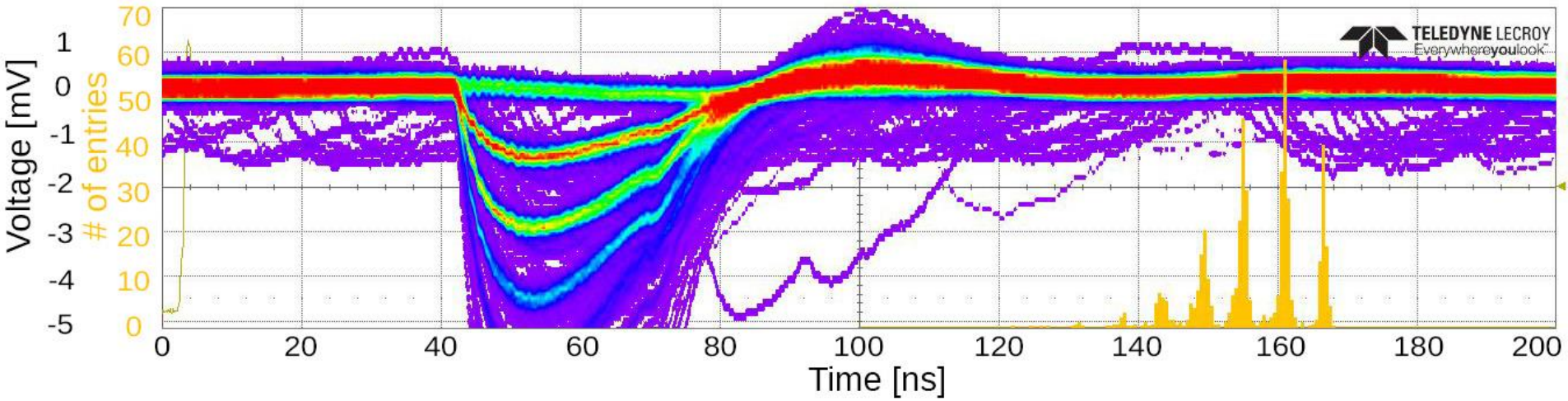


- **Two SiPMs tested:**
  - SiPM S14160-1315PS with an effective photosensitive area of **2mm²** and a pixel pitch of 15μ. [7]
  - S16713 Hamamatsu pre-series SiPM with an effective photosensitive area of **9mm²** and a pixel pitch of 15μ.



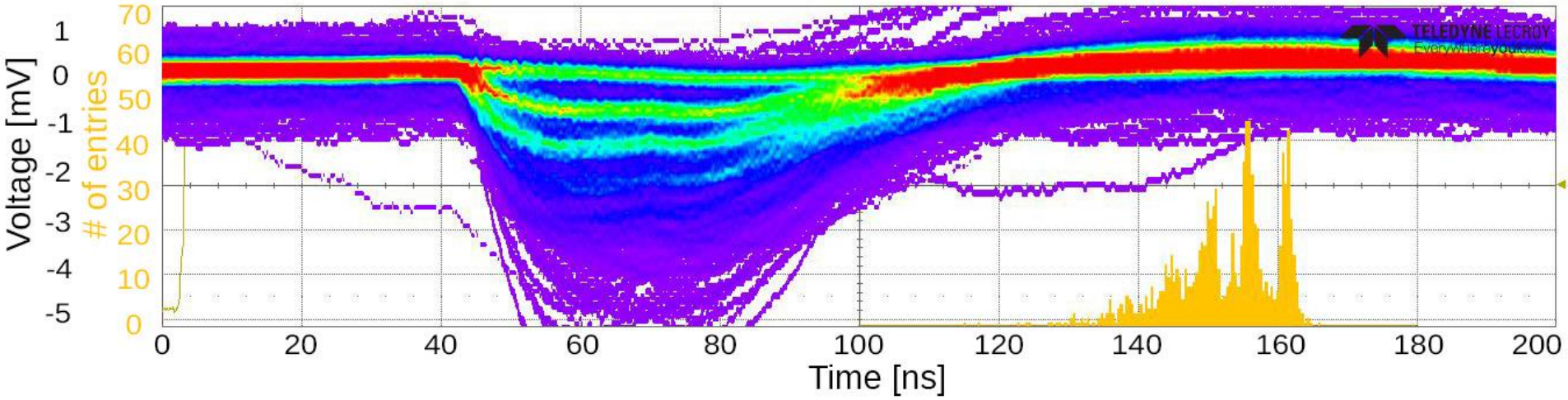
SiPM Oscilloscope measurements

SiPM 2mm²:



- Clear separation of all photon peaks after factor 5 amplification.

SiPM 9mm²:



- Larger noise after factor 5 amplification. Slower rising and falling times
- Hard to see photon separation after the third photon.

SiPM model

Large area SiPM have larger C_G capacitance and larger number of pixels that both increase the total capacitance of the detector (C_{det}).

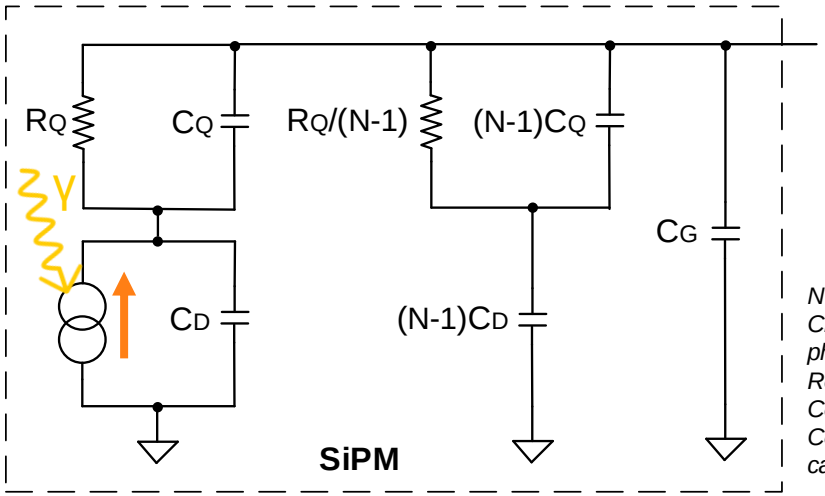
The SiPM capacitance is dominated by C_G value. However, to have an equivalent capacitance an extra margin need to be added to consider the capacitance of each pixel.

- Equivalent detector capacitance of SiPMs:

  2mm²: $C_{det} = 120pF$
  4mm²: $C_{det} = 270pF$
  9mm²: $C_{det} = 560pF$

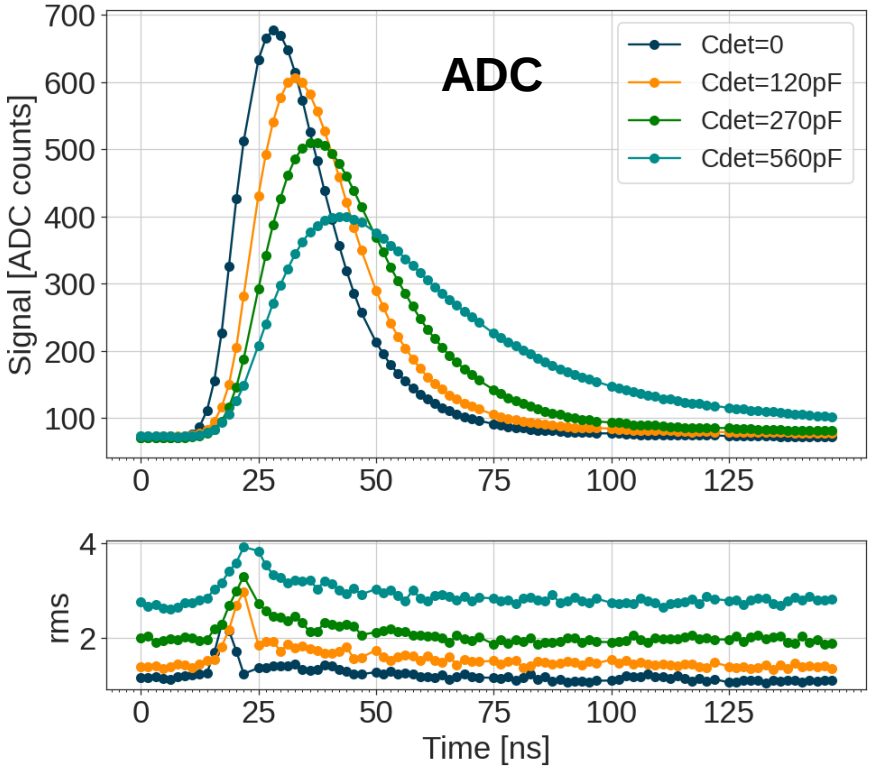
The internal injection of the ASIC can be configured to inject **2.47pC** using an internal DAC and a 3pF capacitor.

The impact of different external capacitors connected to 4 different channels are shown to simulate the detector response.



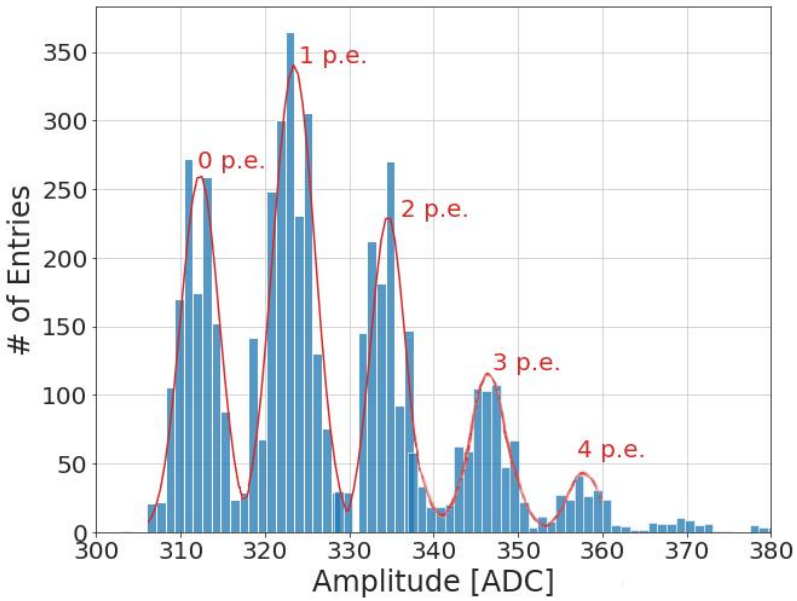
N = # of micro-cells
C_D = Capacitance of photodiode in the micro-cell
R_Q = Quenching resistance
C_Q = Parasitic capacitance
C_G = Total parasitic capacitance

[14]

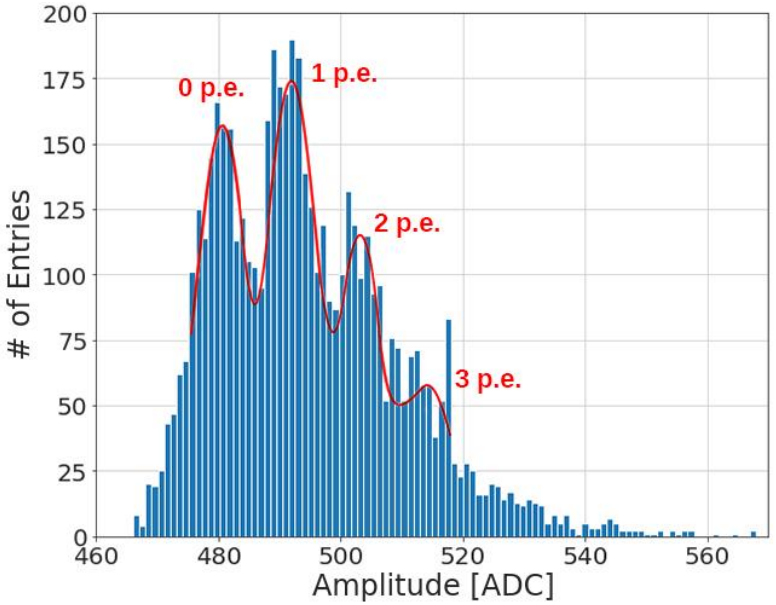


Calibration: Single-photon-spectrum

- **2mm²:**



- **9mm²:**

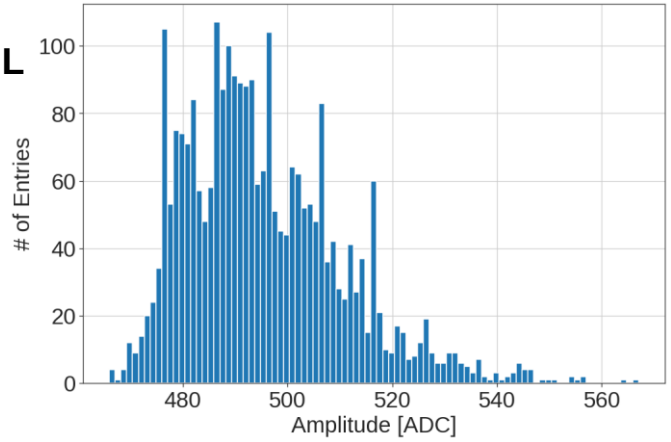


***Extra step for 9mm² SiPM calibration:**

The large C_{det} of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

Without DNL correction:



Calibration: Single-photon-spectrum

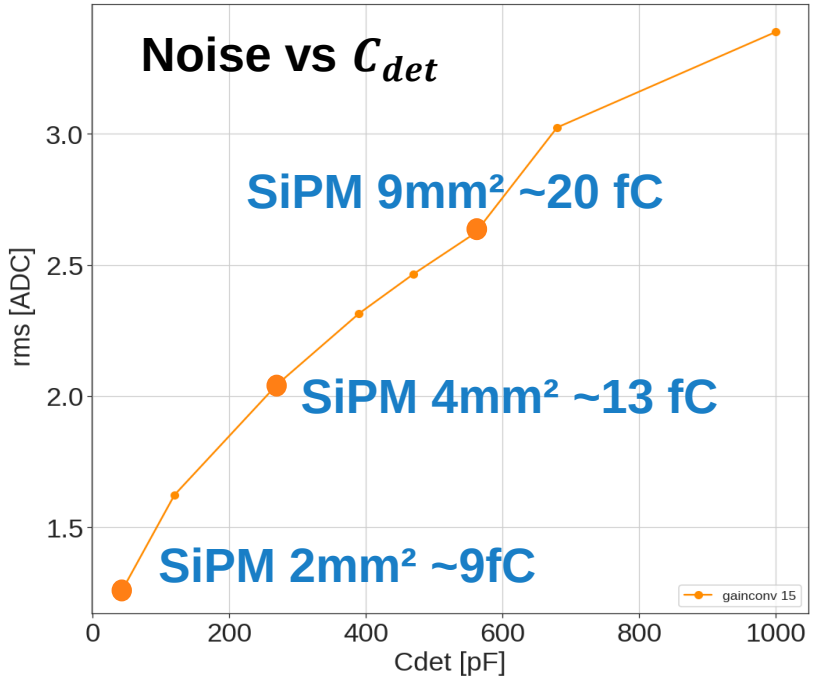
Also a different configuration of the ASIC is necessary to increase the SNR.

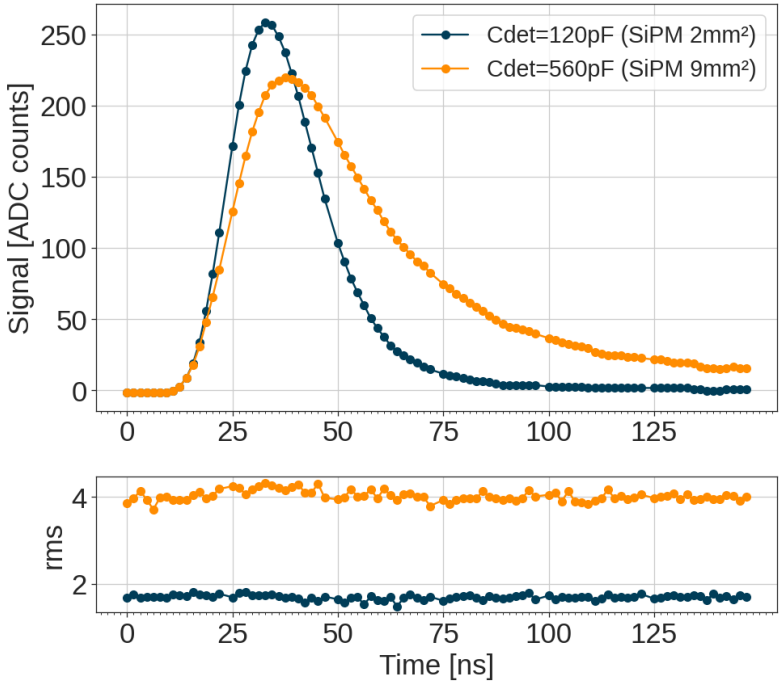
2mm²:

- CC gain attenuation = **0.3**
- $R_f = 16.6\ k\Omega$
- $C_{f\_total} = 600fF\ (C_f + C_{fcomp})$

9mm²:

- CC gain attenuation = **0.375**
- $R_f = 16.6\ k\Omega$
- $C_{f\_total} = \mathbf{300fF}$ (To make the pulse shorter)



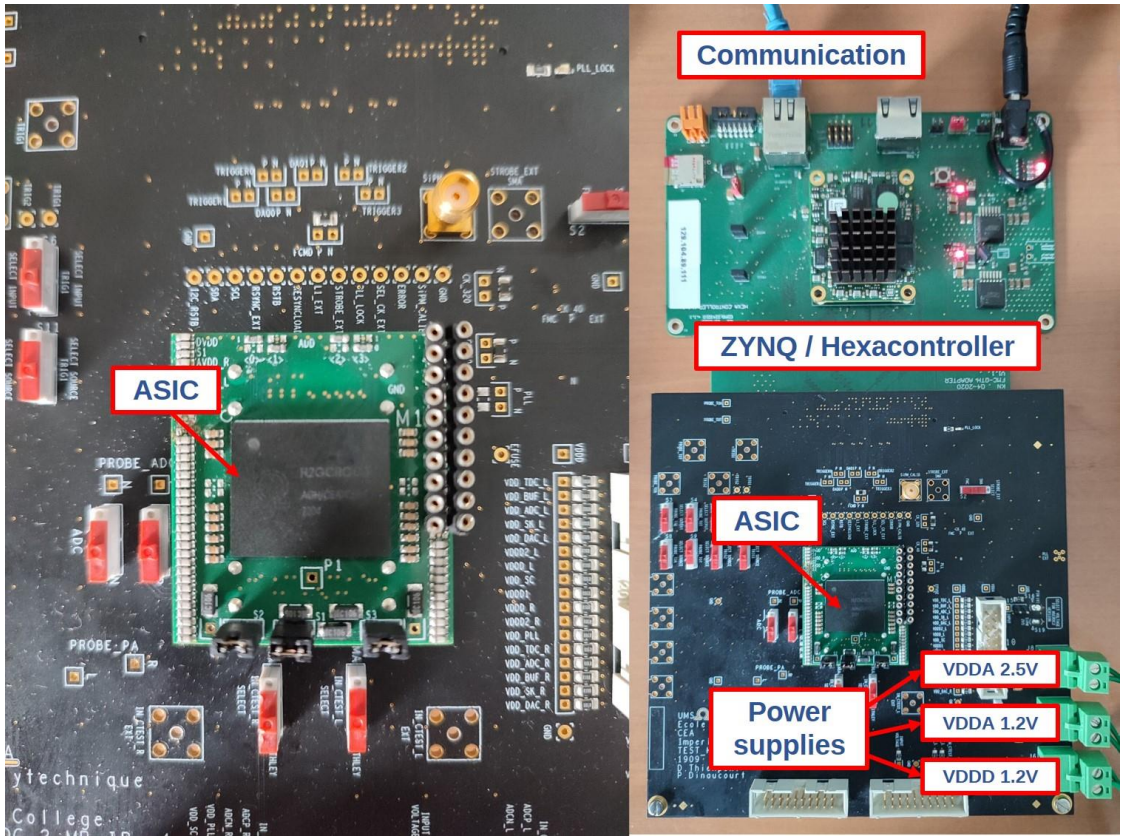


*Noise measured with the same configuration parameters for all C_{det}.

- The increment in noise is due to the detector capacitance of the SiPM.
- SNR can be improved with the gain configuration.

Physics mode: Injection setup

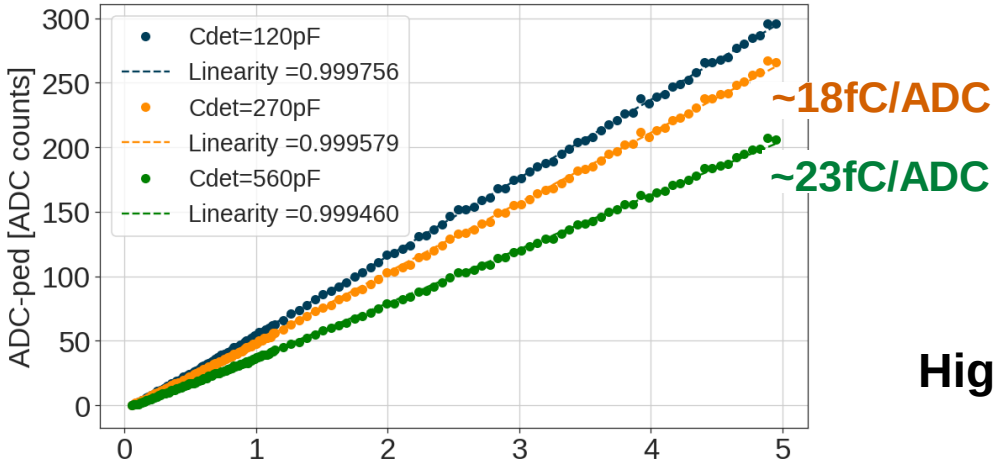
- **The ASIC has an internal 12 bit DAC that can inject up to 1.7V.**
  - Each channel has a 3pF capacitor available at the input.
  - **Low range injection:** Uses just one 3pF capacitor in the selected channel. Charge injection up to **~5pC**
  - **High range injection:** It uses every 3pF capacitor of each channel in parallel and uses the sum of all capacitances (117pF) to convert the DAC voltage to a charge. Charge injection up to **~195pC**



Physics mode

- ~ 60 fC minimum detectable charge efficiently, up to 320pC

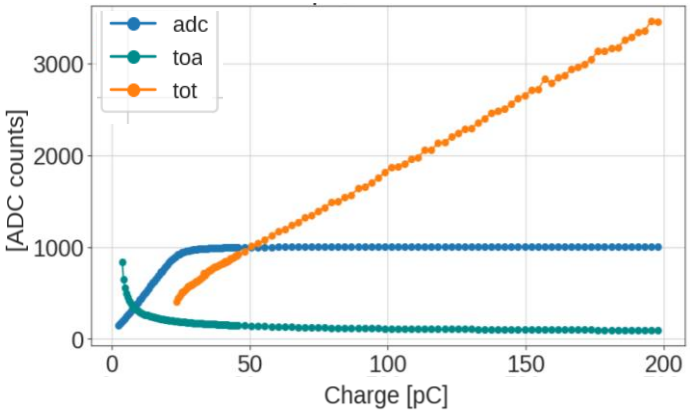
Low range injection (ADC):

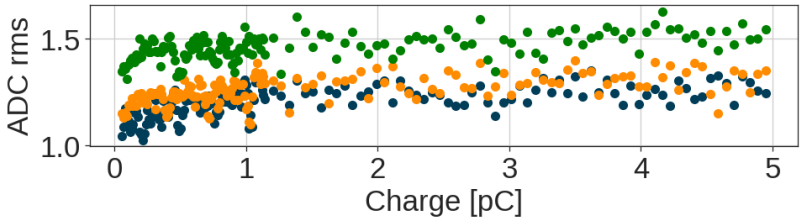


~16fC/ADC

~18fC/ADC

~23fC/ADC

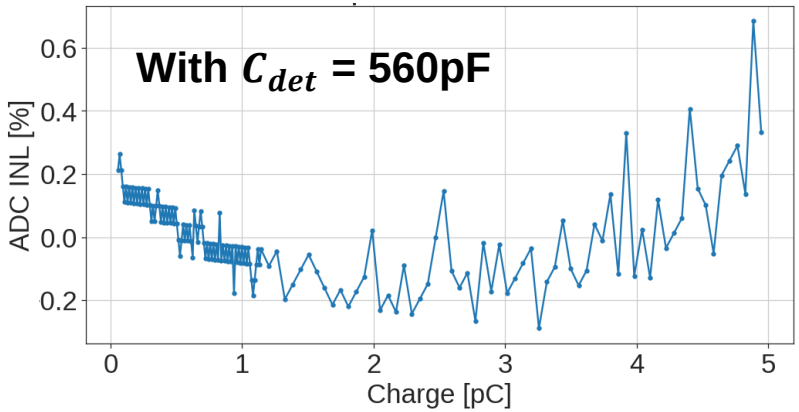




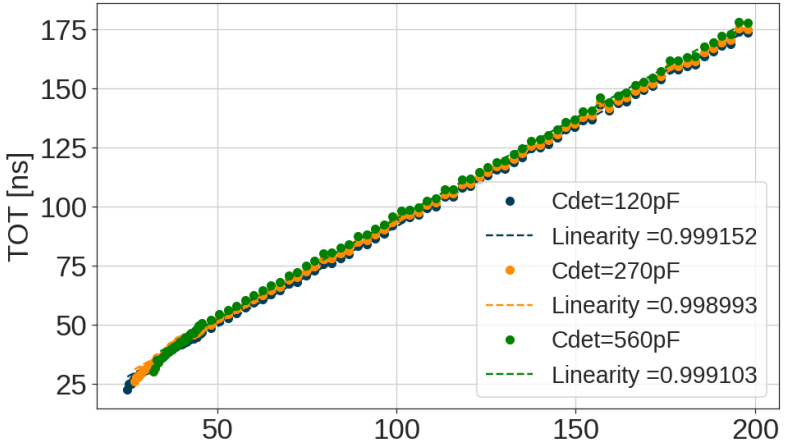
~35fC

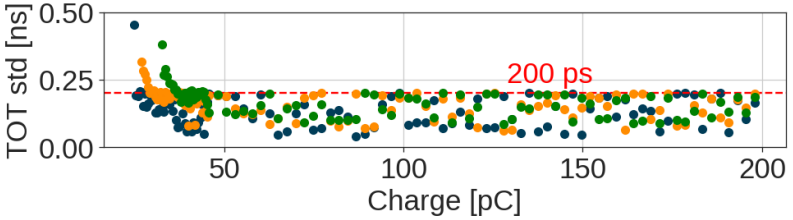
~26fC

~21fC



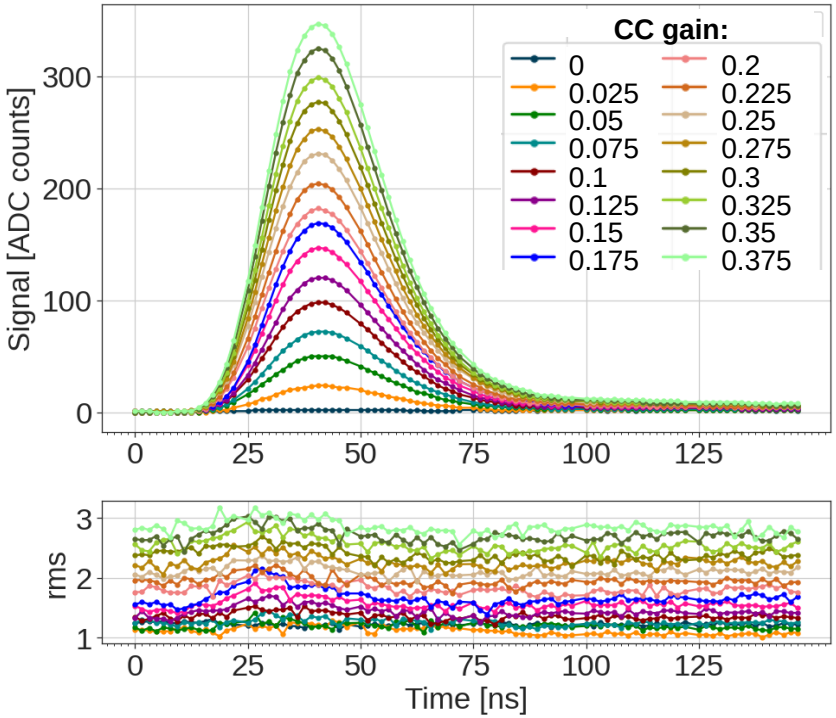
High range injection (TOT):



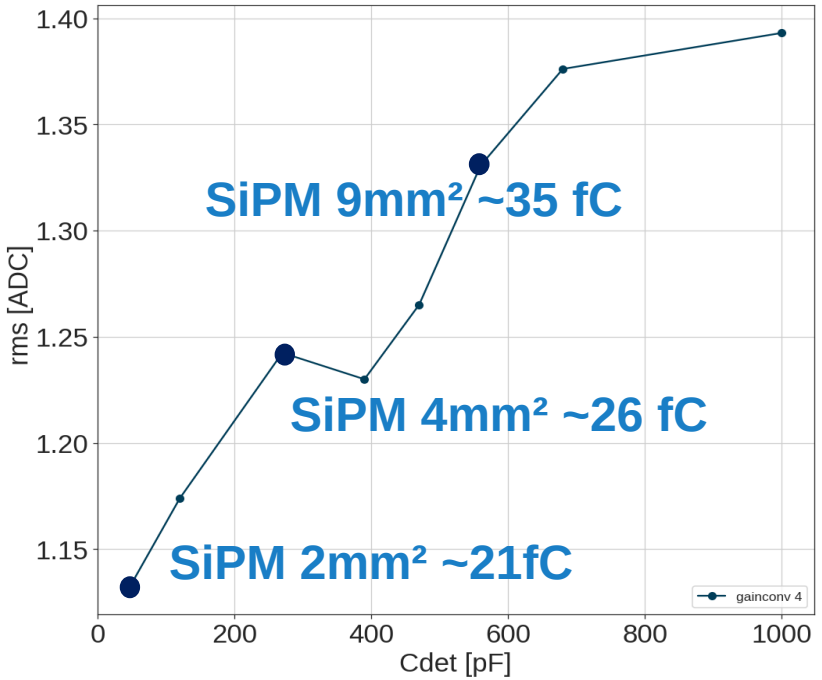


Physics mode

CC gain scan:



Noise vs C_{det}:

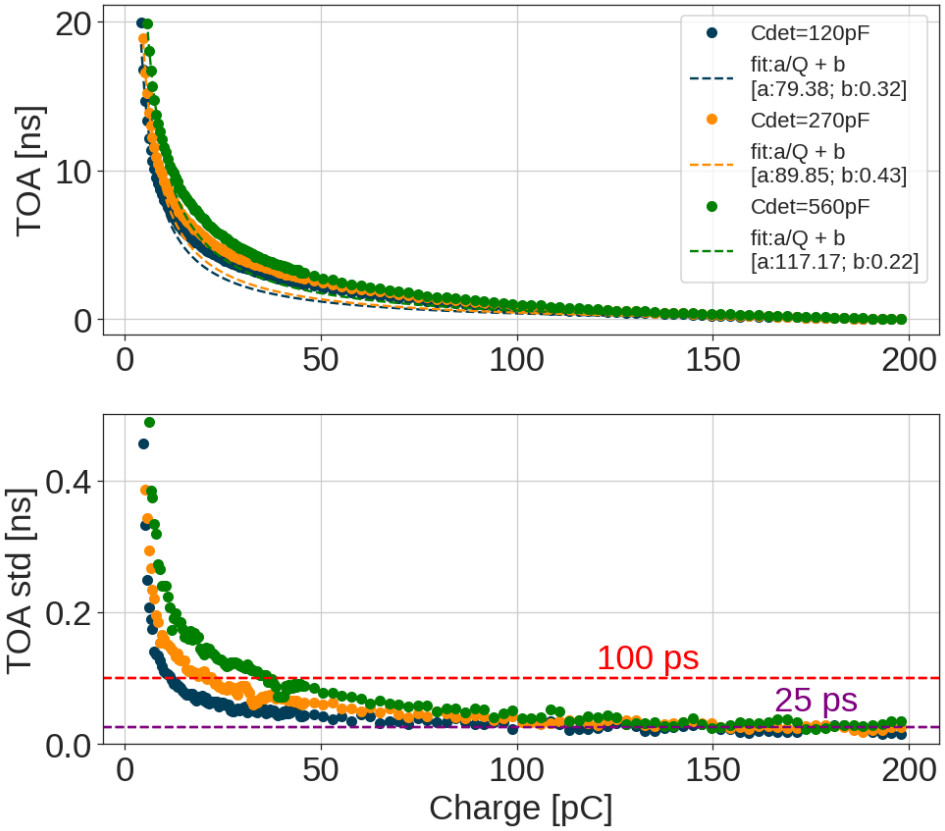


- The CC gain has good performance in linearity.
- The increment in noise is due to the gain configuration and the detector capacitance of the SiPM.

* May be necessary to have a configuration file for each SiPM. Both the calibration mode and physics modes.

Physics mode

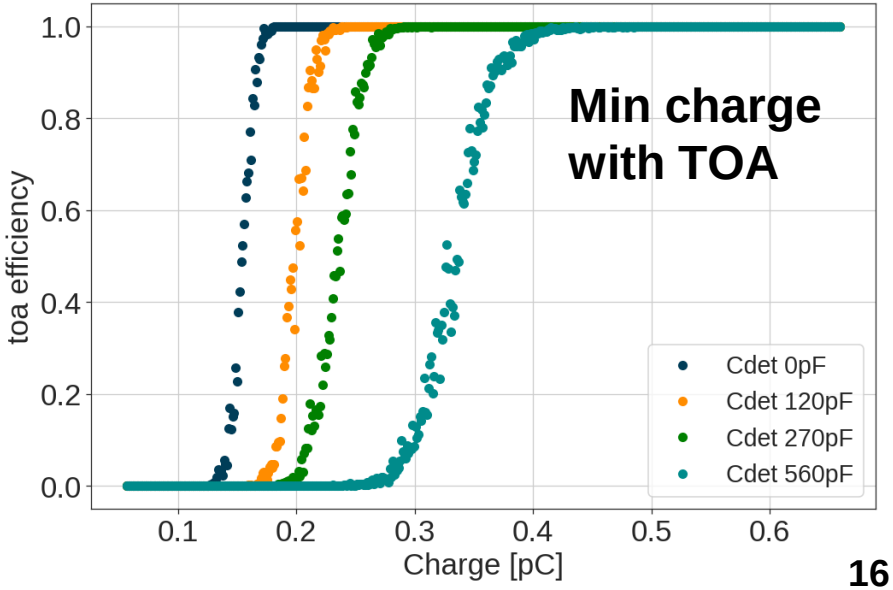
TOA:



- The increase in noise due to larger C_{det} shifts the minimum charge associated with TOA data.
- The thresholds can be adjusted channel-wise for a uniform performance.

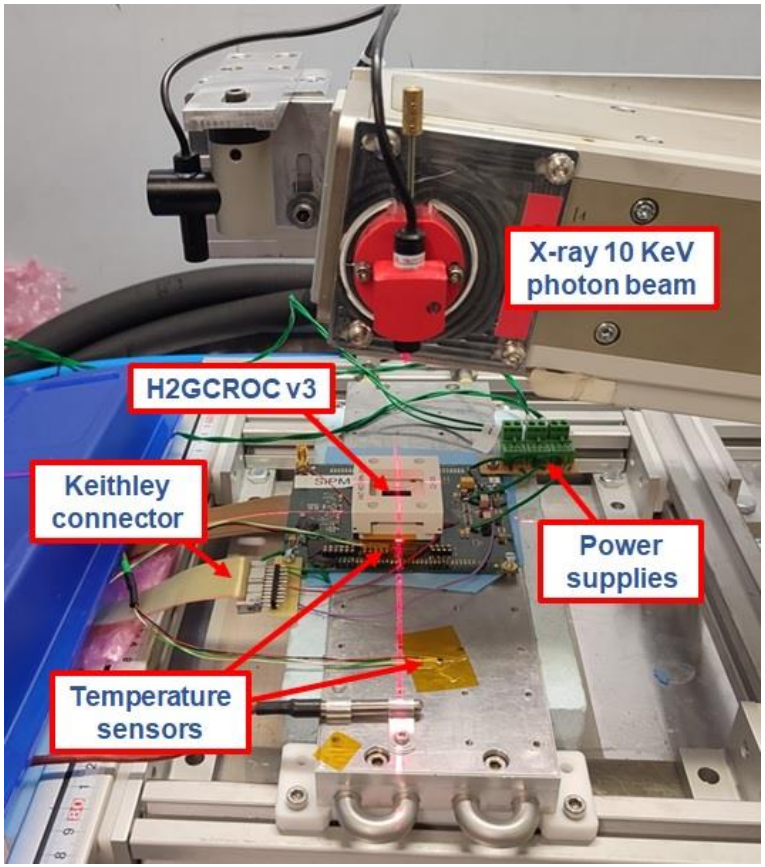
Effect of C_{det} on TOA:

- Larger C_{det} produce larger time walk due to the duration of the signal.
- Increasing C_{det} delayed the achievement of a 100ps resolution in charge injection.

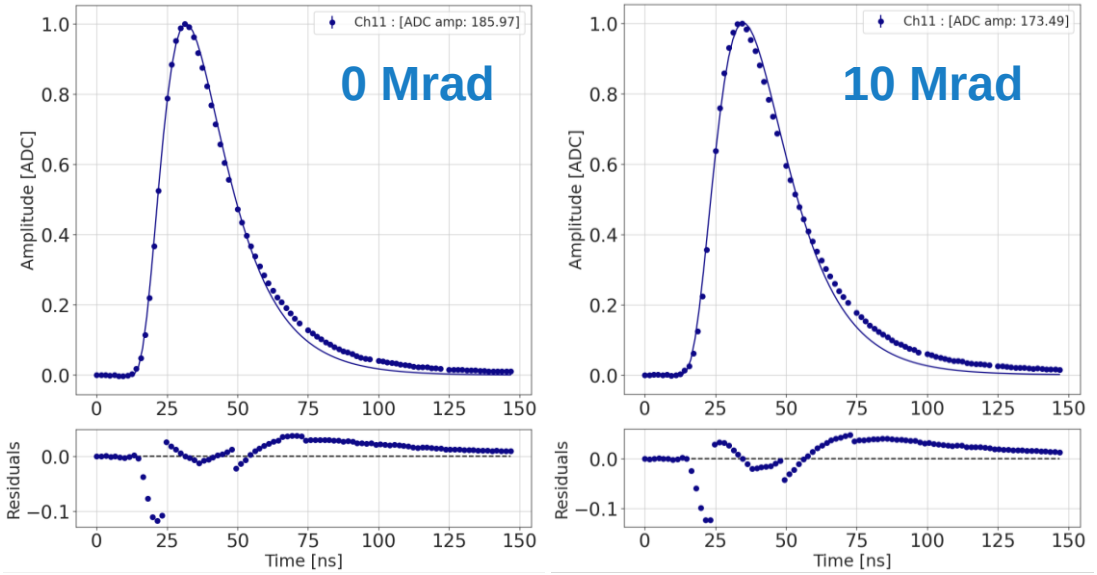


Irradiation campaigns

- Power consumption, ADC & TDC performance, noise, links stability, etc. tested during irradiation
- **TID irradiation tests in both ASIC versions.** [8,9,10,11]
- **Heavy ion and Proton irradiation in the Si version of the ASIC** [12,13]
  - Increase on triplicated parts for HGCROC3b



Stability of ADC measurements after 10Mrad:



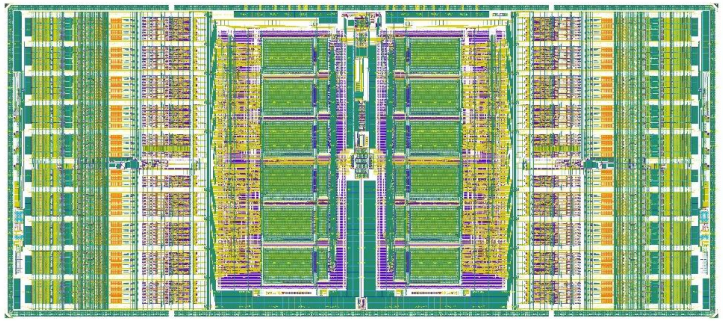
- **H2GCROCv3** has proven to be **radiation tolerant up to 10 Mrad** at -5°C with good ADC, TDC and PLL measurements.

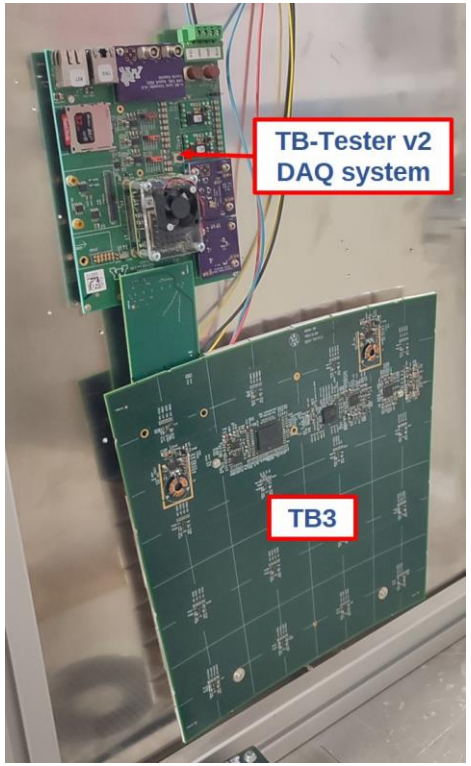
Conclusions

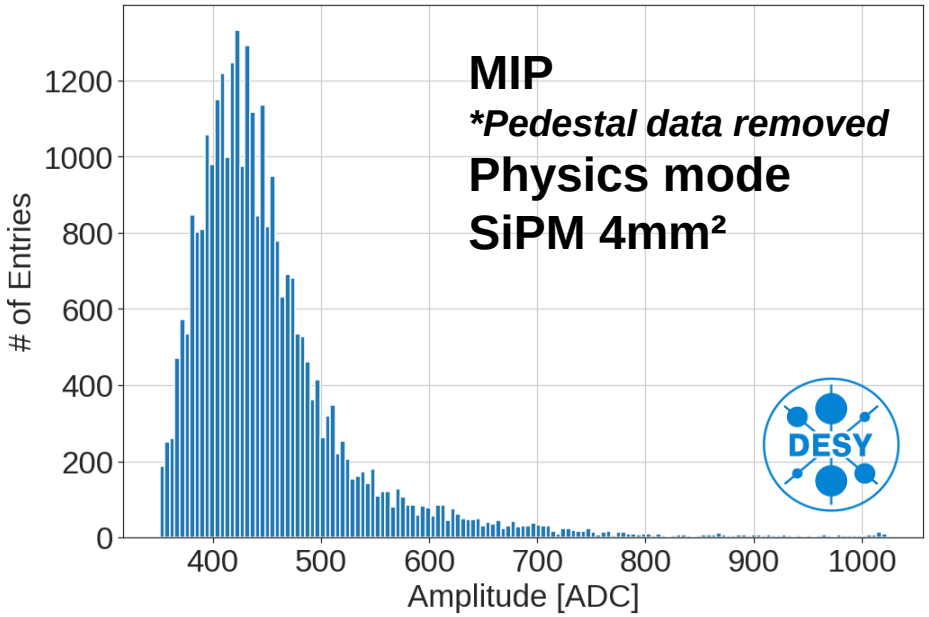
- H2GCROC3 is robust enough to be calibrated for the different SiPM of HGCAL
- The configuration of the ASIC needs to be carefully selected to adapt gain, linearity, time walk and charge range.
- ASIC tested at beam and TID campaigns.
- Minor corrections are expected for H2GCROC3b.
- **Beam data:**

**Energy: 3GeV*
64ch Tileboard
fully equipped
with 4mm² SiPM

H2GCROC3 Layout:







**The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).*

Thank you for your attention

Backup

HGCROC3: Architectural overview

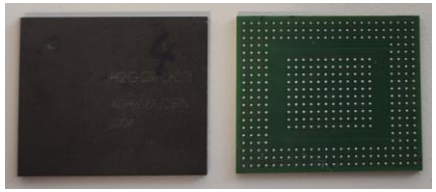
Overall chip divided in two symmetrical parts

- **1 half is made of:**
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

HGCROC3
High density

Two data flows

- **DAQ path**
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links
- **Trigger path**
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links

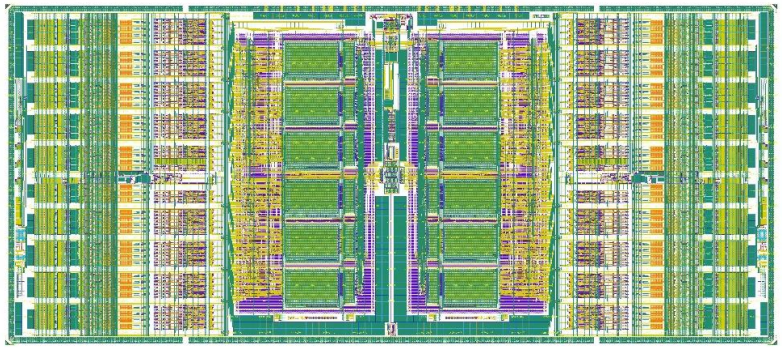


H2GCROC3
Low density

Control

- **Fast commands**
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- **I2C protocol for slow control**

HGCROC3 Layout:

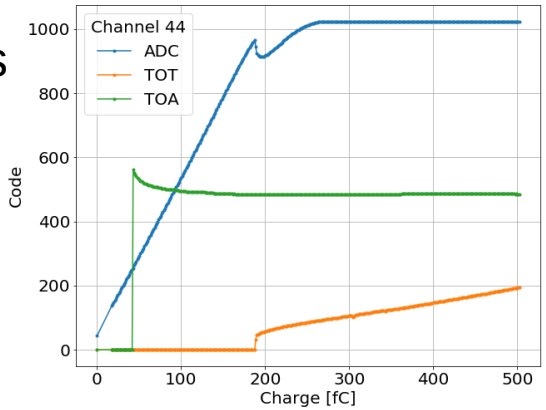


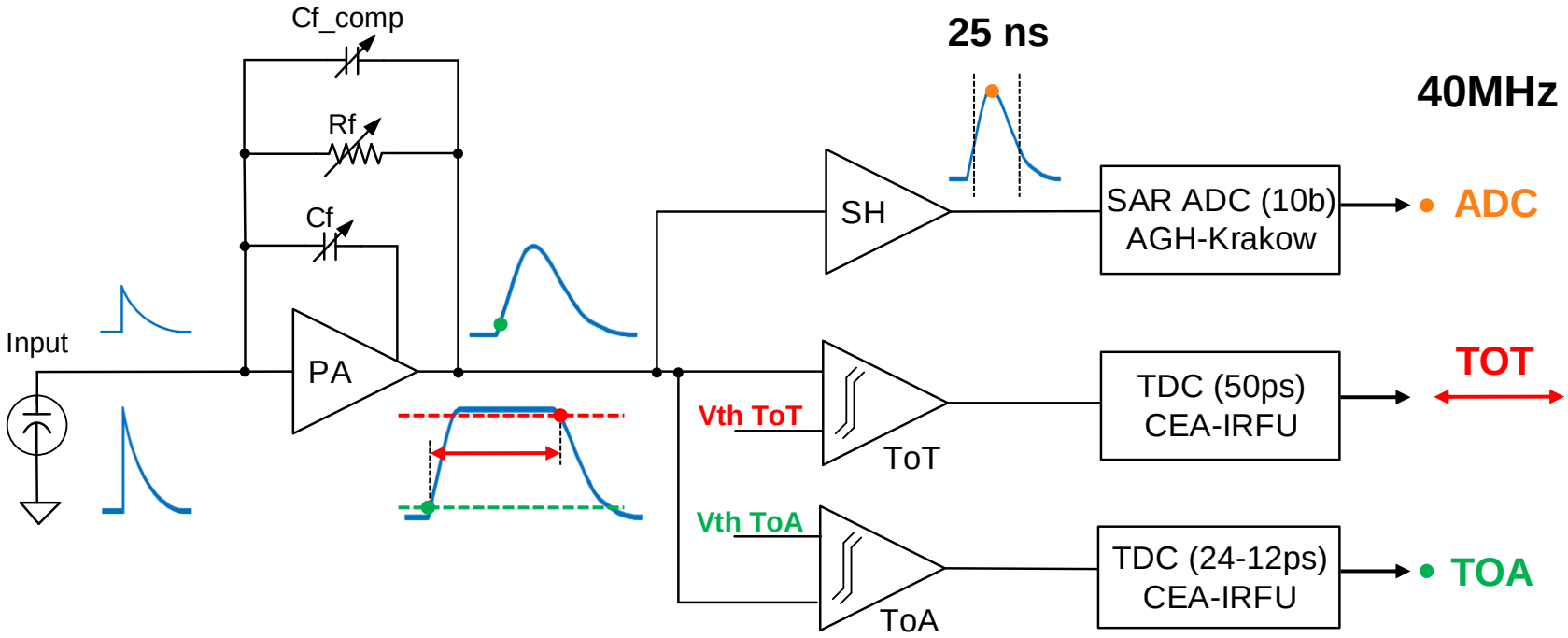
Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

HGCROC3: Analog channel overview

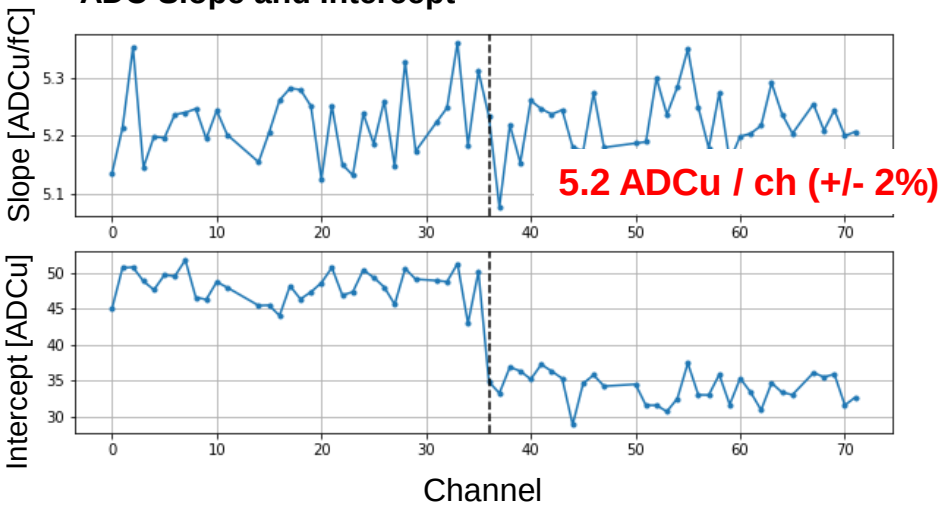
- **Calibration pulser**, 0.5pF and 10 pF calibration cap.
- **Preamp :** adjustable gains for 80, 160 and 320 fC ranges
- **Tunable TOT** over 5 bits
- **Sallen Key shaper RC4**, tp<25 ns, tunable (~20%) with 2 bits, BX+1/BX<0.2
- Temperature stabilization to < 0.5 mV/K
- **10 bit ADC from Krakow AGH**
- **TOT and TOA TDCs from CEA-IRFU**





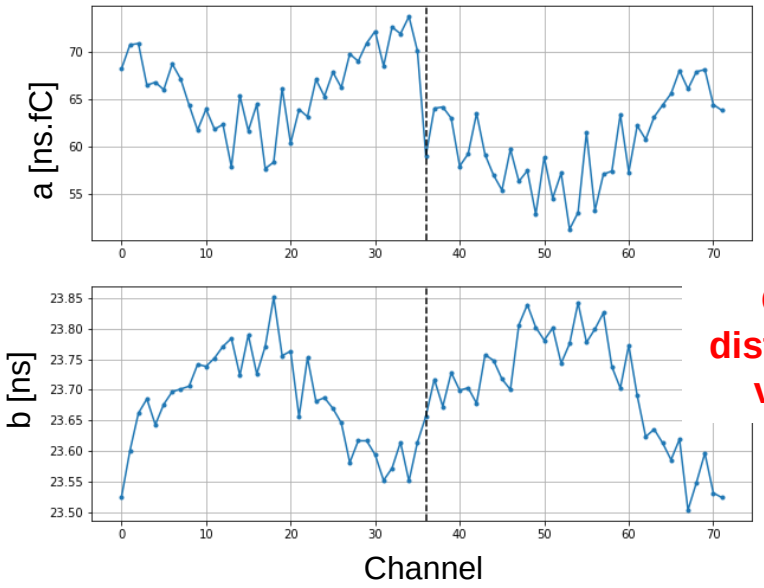
HGCROC3: Charge and time uniformity

ADC Slope and Intercept



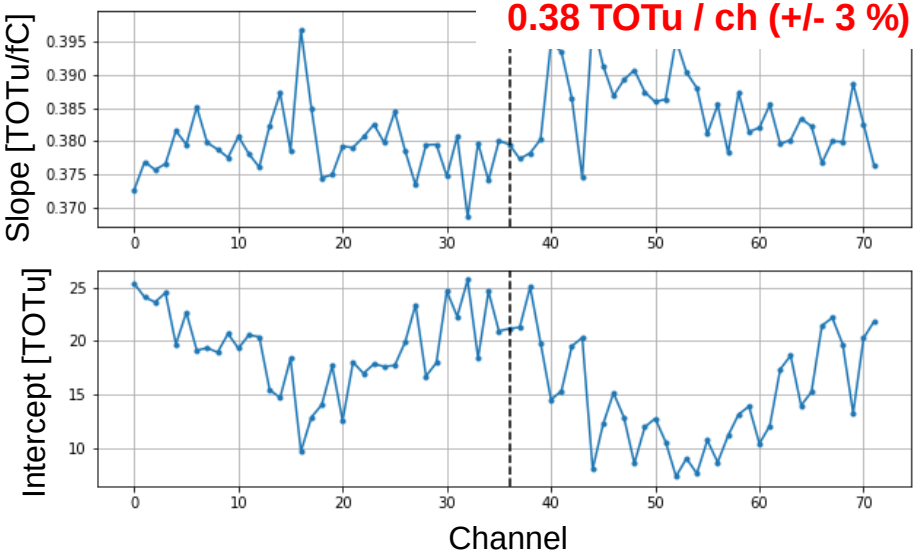
5.2 ADCu / ch (+/- 2%)

TOA Time Walk. a & b parameters of the $a/Q + b$ fit



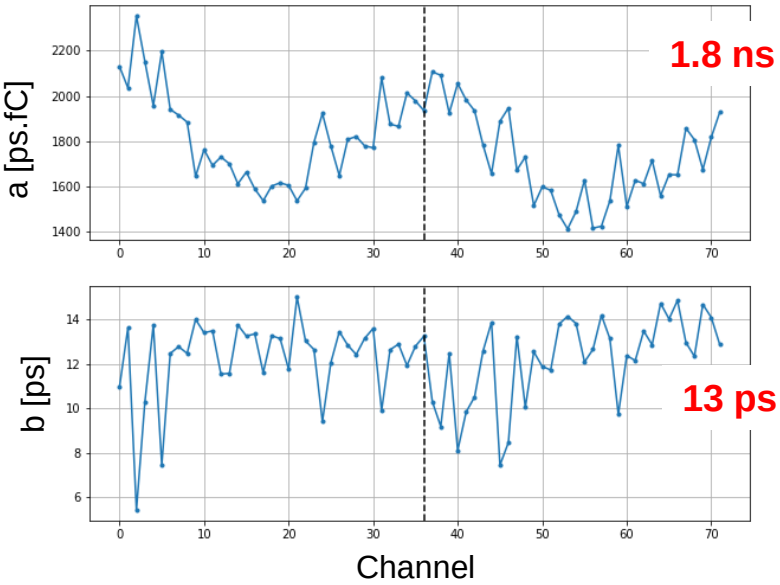
Clock distribution visible

TOT Slope and Intercept



0.38 TOTu / ch (+/- 3 %)

TOA Jitter. a & b parameters of the $\sqrt{(a/Q)^2+b^2}$ fit



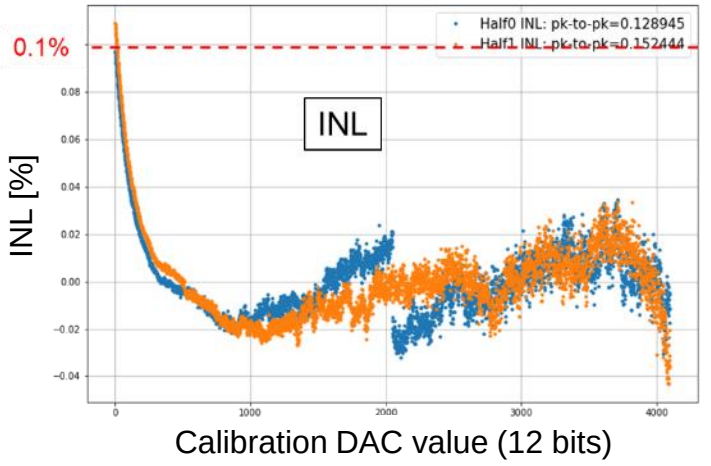
1.8 ns / Q(fC)

13 ps rms

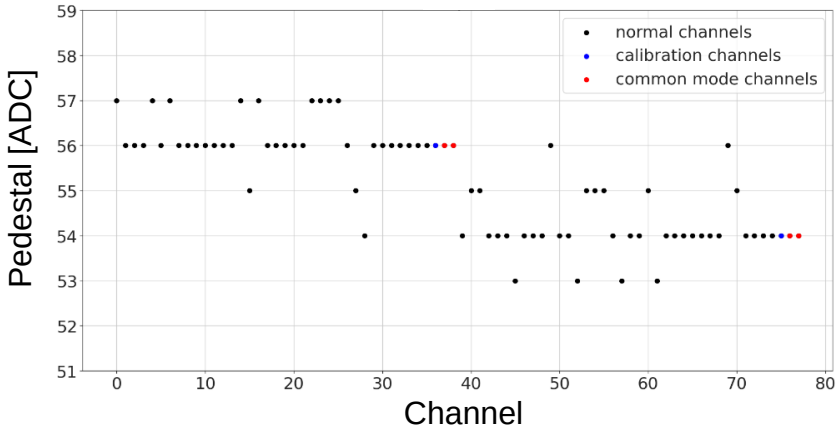
DACs & trimming

- **12 bits calibration DAC**
  - ~ 2-3 mV offset due to leakage current (1 – 1.5 fC)
  - < 0.1 % linearity, temperature sensitivity: 60 ppm/K, stable after 350 Mrad
- **Four 10-bit DACs** to set pedestals, TOA & TOT thresholds + **3 channel-wise 6-bit DACs** to reduce dispersion per channel
  - Pedestals: ~ 1 ADC counts dispersion after trimming
  - TOA & TOT thresholds: 1-2 DAC counts after trimming
- 8-bit input DAC to compensate for the **leakage current** up to **50 µA**
  - Additional noise as expected from simulation

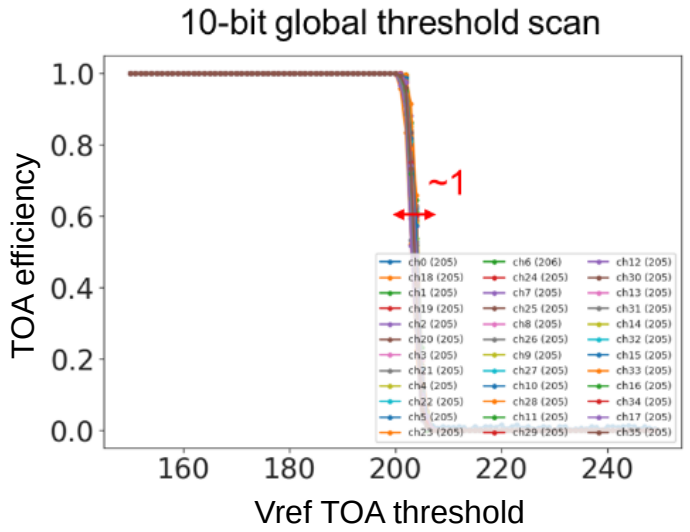
Calibration DAC:



Trimmed pedestals:

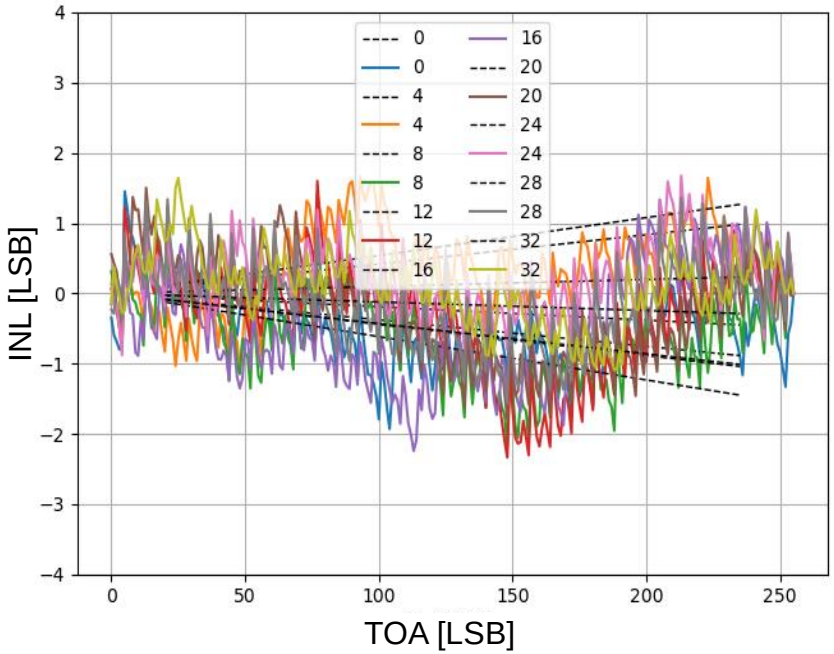


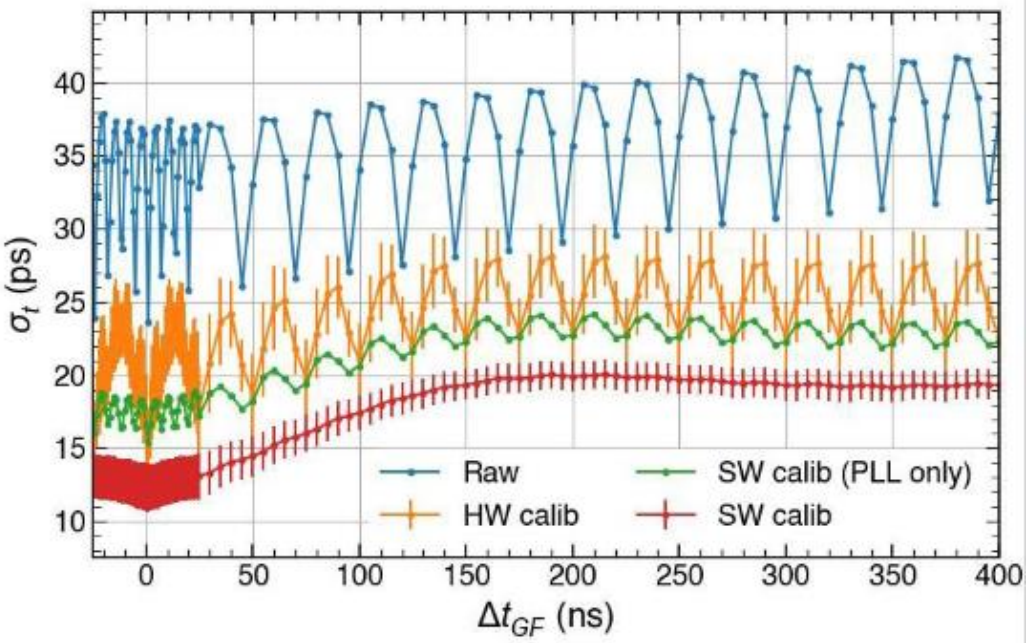
Trimmed TOA thresholds:



TDC V3 INL measurements

- I2C parameters to tune master and channel-wise DLLs
- Parameters can be optimized thank to the on-chip asynchronous clock generator (ACG) by minimizing the INL.





TDC calibration in 2 steps:

- Master DLL tuning
- Individual channel DLL tuning

After Calibration: INL < ± 2 LSBs, < 16 ps resolution

Resolution of 2 uncorrelated chips given by resolution at large T-delays

- Before calibration (blue): ~ 40 ps resolution
- After calibration (orange): < 30 ps resolution
- (After software correction (cancel FPGA clock jitter): **< 20 ps resolution**)

SEE (Single Event Effect) Irradiation Test

- Only tested in **HGCROC Si version** for both Protons and Heavy ions.
- Test the radiation damage induced by a single particle to electronic devices and non-cumulative. It can cause a failure at any moment since the beginning of operation.
- **Three types:**
  - Single Event Upset (**SEU**): bit flip (0 -> 1 or 1 -> 0).
  - Single Event Transient (**SET**): bit shift.
  - Single Event Latchup (**SEL**): permanent damage.

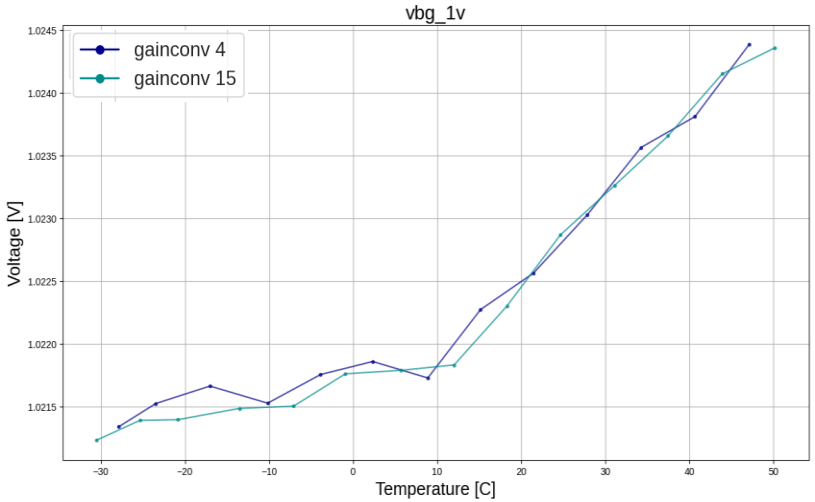
# errors	Counters	Trigger	CRC	Memory	Short SET	**Long SET**
Heavy ions [12]	0	1	2	3	24	**18**
Protons [13]	< 1	38	30	127	85	**190**

1 link loss / 2.5 years (for each chip on average)

- Very few errors in the not triplicated parts of Trigger and CRC.
- Very few errors in the memory, always detected by the hamming.
- Many errors in the not triplicated part (**PLL**).
  - **Increase in the triplication of the new version of PLL (Tested in EICROC).**

**Analysis by Elena Vernazza*

H2GCROC3: Temperature



Bandgap (Two slopes):

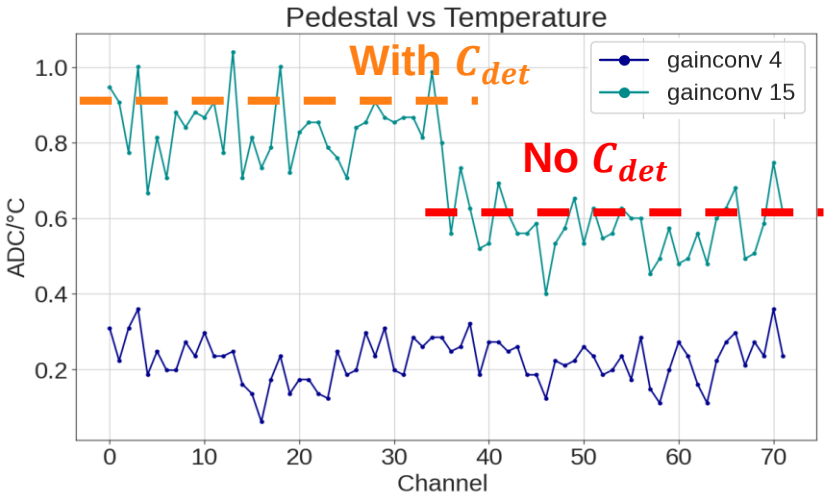
From -30°C to 10°C: ***12.5 µV / °C***

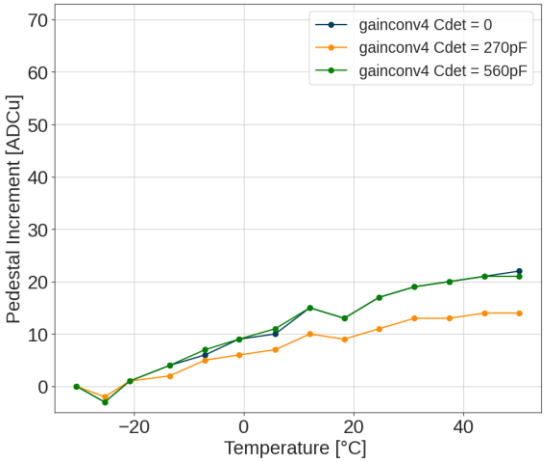
From 10°C to 50°C: ***65 µV / °C***

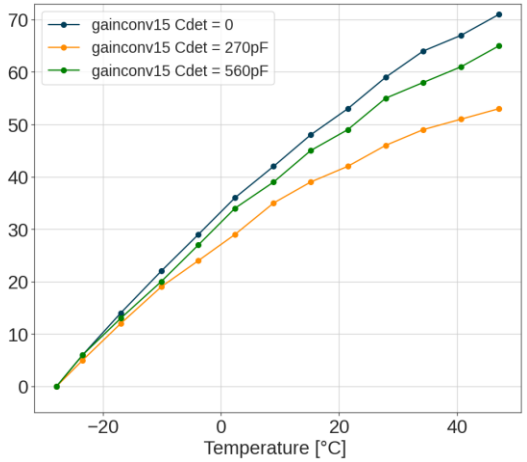
Pedestals:

Physics mode: ***+ 0.3 ADCu / °C***

Calibration mode: ***+ 0.9 ADCu / °C***







*Noise : almost flat

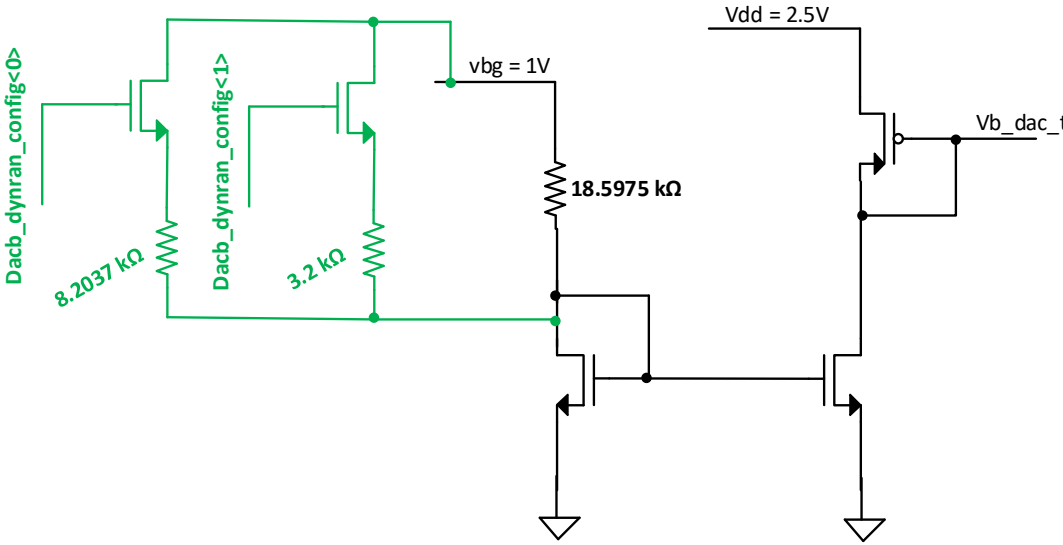
H2GCROC: Leakage compensation

Dacb_dynran_config (2 bits). Extra resistors added to modify the current that controls the dynamic range of dacb.

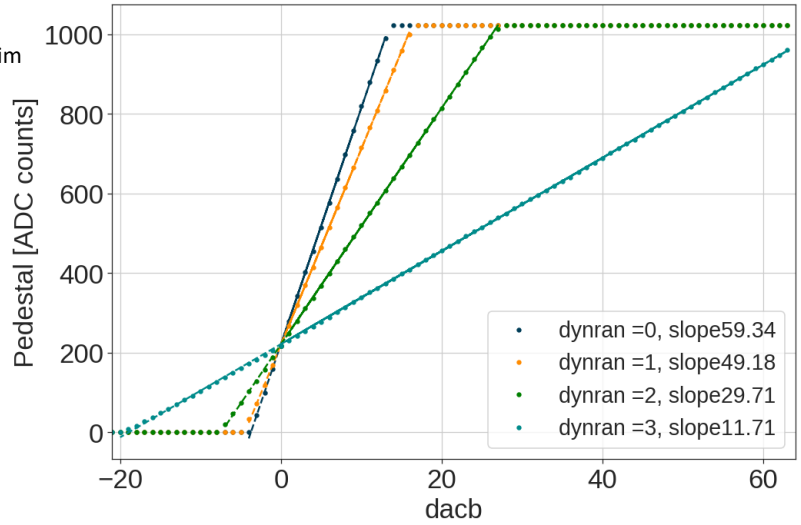
Dacb_dynran_ config	Leakage current Correction range	Max dacb current	OUTPA pedestal step
0	0 to ~270 µA	~21 µA	~6.45mV
1	0 to ~660 µA	~54 µA	~16.4mV
2	0 to ~1.09 mA	~90 µA	~27.2mV
3	0 to ~***1.31 mA***	~109 µA	~32.96mV

*Optimum for Ileak = 1mA compensation with gainconv = 4

*Extra correction for gainconv > 4



H2GCROC3 measurements:



Power consumption

- **HGCROC3:** extrapolation for LD & HD modules (w/o LDO contribution)

	Analog (half)		Digital		Low Density module Analog		Low Density module Digital		High Density module Analog		High Density module Digital		Comments
	(mA)	(mW)	(mA)	(mW)	(A)	(W)	(A)	(W)	(A)	(W)	(A)	(W)	
Low power mode	**63**	**76**	**83**	**100**	**0,378**	**0,456**	**0,249**	**0,3**	**0,756**	**0,912**	**0,498**	**0,6**	RUN = 0
Default config	260	312	127	153	1,56	1,872	0,381	0,459	3,12	3,744	0,762	0,918	Not trimmed parameters
trimmed	**260**	**312**	**127**	**153**	**1,56**	**1,872**	**0,381**	**0,459**	**3,12**	**3,744**	**0,762**	**0,918**	Adjusted pedestals, threshold, gain …
vbi11	300	360	127	153	1,8	2,16	0,381	0,459	3,6	4,32	0,762	0,918	trim_vbi_pa=11 (default is 7)
vbi15	330	396	127	153	1,98	2,376	0,381	0,459	3,96	4,752	0,762	0,918	trim_vbi_pa=15
50% 10ch	280	336	134	161	1,68	2,016	0,402	0,483	3,36	4,032	0,804	0,966	trimmed conf. + 50% TOA in 10 channels per half
50% all	325	390	154	185	1,95	2,34	0,462	0,555	3,9	4,68	0,924	1,11	trimmed conf. + 50% TOA in all channels
LowBuf	215	258	127	153	1,29	1,548	0,381	0,459	2,58	3,096	0,762	0,918	Low power ADC buffer
LowBuf + vbi11	255	306	127	153	1,53	1,836	0,381	0,459	3,06	3,672	0,762	0,918	
LowBuf + vbi15	290	348	127	153	1,74	2,088	0,381	0,459	3,48	4,176	0,762	0,918	

Spec < 15 mW / channel

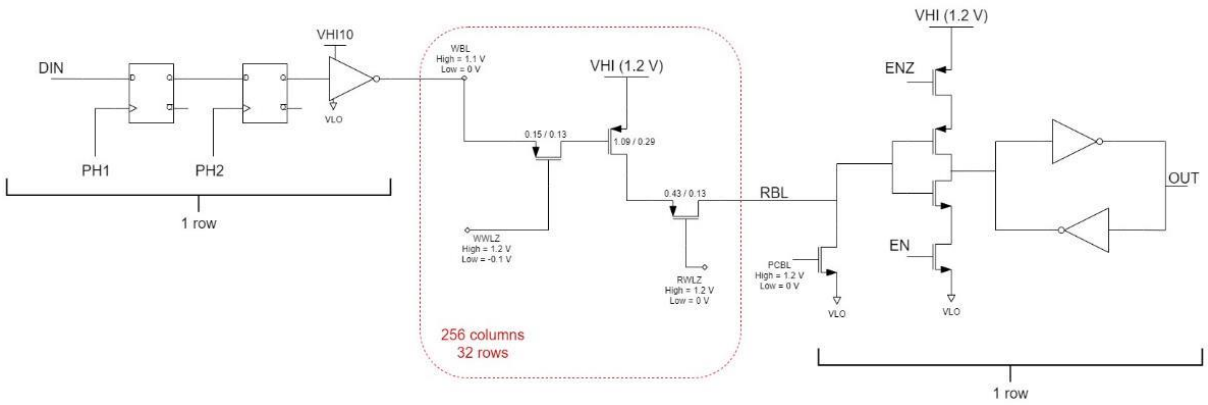
- Low power mode: 3,5 mW / channel
- Default config : ~10,8 mW /channel
- With 50 % toa events in 50 % channels: 11,5 mW / channel
- With maximum preamp. current : **11,8 mW / channel**

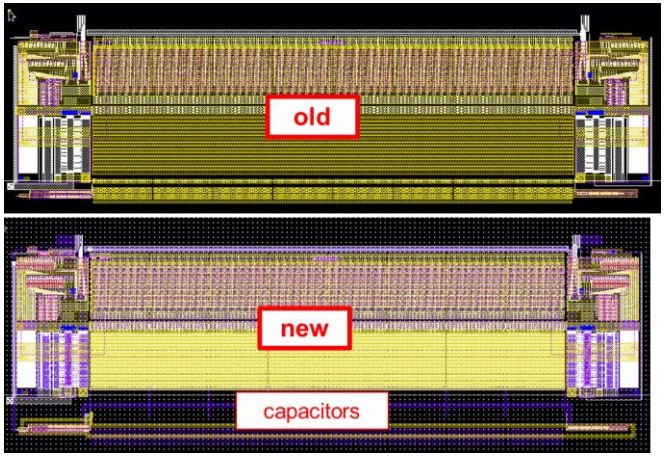
- **H2GCROC3:**

		Analog 1.2		Analog 2.5 (2.41)		Digital 1.2		Comments
	Gain_conv	mA	mW	mA	mW	mA	mW	
Low power mode	15	104.30	125.16	27.90	67.24	112.70	135.24	
Default config		353.20	423.84	136.80	329.69	123.00	147.60	
vbi_pa 48		356.30	427.56	116.80	281.49	125.90	151.08	dacb_vbi_pa = 48
vbi_pa 63		356.50	427.80	94.80	228.47	127.00	152.40	dacb_vbi_pa = 63
10 ch TOA		357.00	428.40	136.60	329.21	124.80	149.76	toath = 65, 10 channel per half unmasked
all ch TOA		359.00	430.80	136.50	328.97	126.30	151.56	toath = 65, all channels unmasked
Default config	2	376.00	451.20	128.60	309.93	135.30	162.36	
vbi_pa 48		374.00	448.80	108.90	262.45	134.50	161.40	dacb_vbi_pa = 48
vbi_pa 63		366.50	439.80	87.30	210.39	135.40	162.48	dacb_vbi_pa = 63
10 ch TOA		375.20	450.24	128.60	309.93	135.30	162.36	toath = 65, 10 channel per half unmasked
all ch TOA		376.20	451.44	128.80	310.41	131.10	157.32	toath = 65, all channels unmasked

Issue 1: bitflips in the Rams

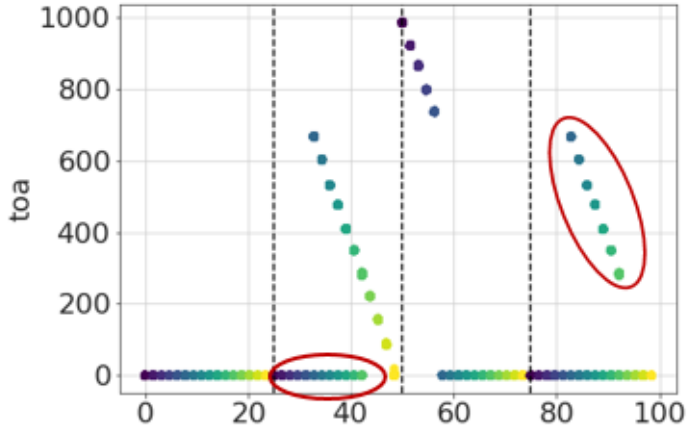
- **Large majority of 1 > 0 bitflips**
  - Not a classical leakage effect
  - Better (almost perfect) at low temperature and/or low digital power supply
- **RBL node has been identified as culprit**
  - Lower capacitance on RAM2 (due to the shrink from 512 to 32)
  - Reproduced in simulation
  - Force VHI10_0 to VDDD corrects the misbehaviour
    - No bitflips at all whatever the temperature and power supply value
    - No problem with multi consecutive L1A
- **Corrected for next version**, **ROC3b**, add capacitance on this node and possibility to force VHI10_0 to VDDD
- Has been implemented in HKROC1, first measurements show the fix works

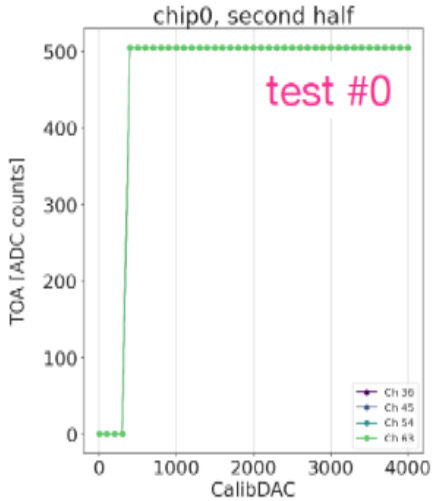


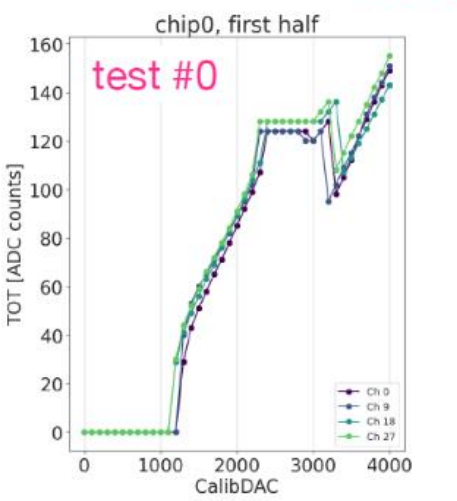


Issue 2: TDC

- **Issue 2.1: TOA data in the wrong BXs**
  - Error localization in the start of the latency buffer of the TDC FiFo. A double clock gating causes a glitch in the zone where the 40MHz clock is at 0
  - This effect is reproduced in simulation and **will be corrected in HGCROC3b**
- **Issue 2.2: TOA data for all channels from the same half are stuck to 504 (0b 01 11111 000)**
  - Infrequent effect, impossible to make reproducible
  - Resetting the chip resolves the issue
  - Reproduced in simulation: the Master DLL is not properly locked
  - **Has been fixed by changing the startup sequence**
- **Issue 2.3: Strange (faster) TDC measurement**
  - Happens more often than issue 2.2
  - Completely removed after tuning DLL parameters (Charge pump current)
  - Has been fixed by changing the startup sequence



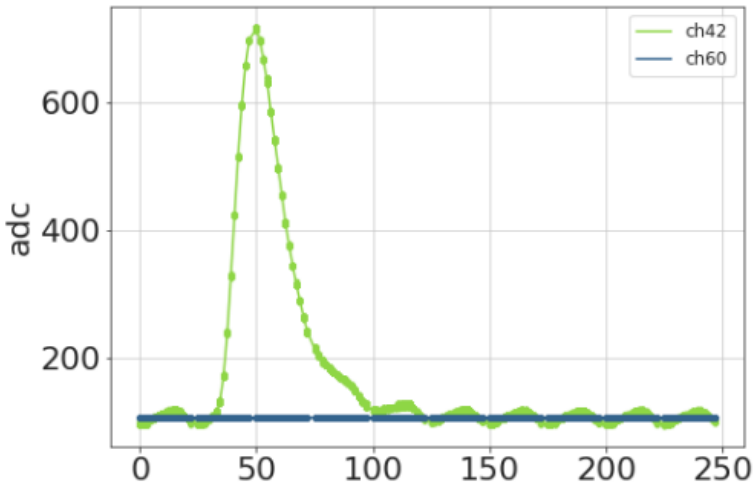


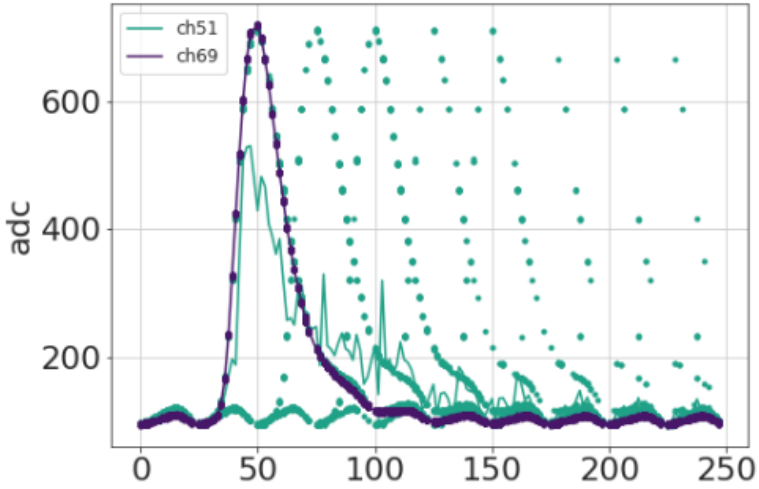


Issue 3: ADC

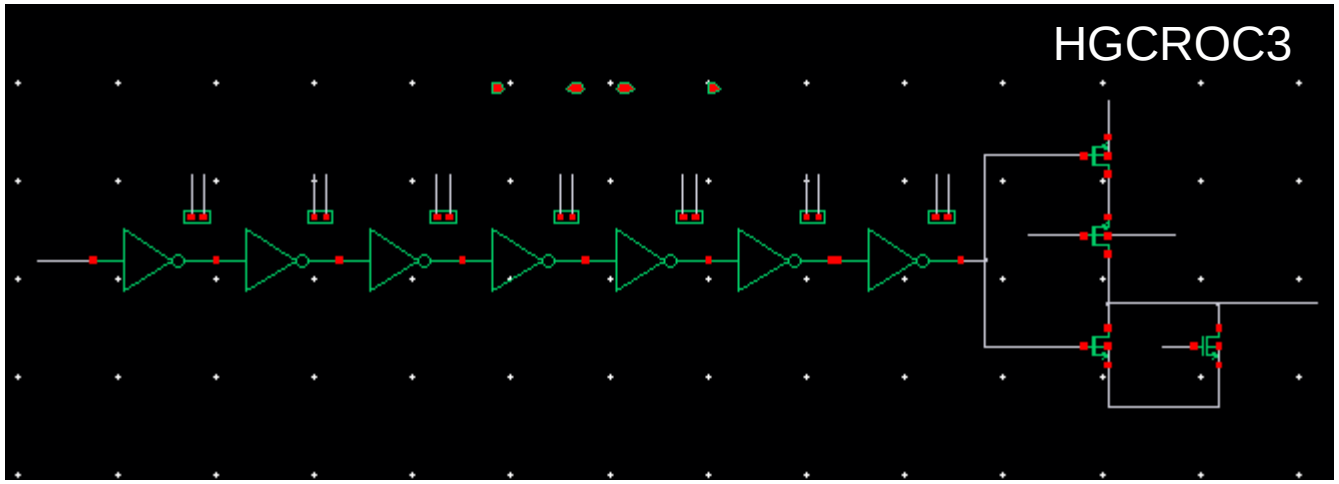
- **Flat ADC or Multiple ADC**
  - Already in HGCROC2, although less often
    - More easily resolved by tuning conversion time
    - HGCROC2 run faster than HGCROC3 which seems more in the typical region
  - The ADC does not convert at 40 MHz
  - Sensitive to ADC settings (conversion time), temperature, digital power supply
  - ~ 5 % of the channels at room temperature, but not Gaussian distribution at all
  - RC-extracted view reproduces both flat ADC and Multiple ADC effect (6% bad channels against ~ 5% in measurement)

  - **Will be corrected in HGCROC3b (Next slide)**
  - **Correction proved to work in HKROC1**

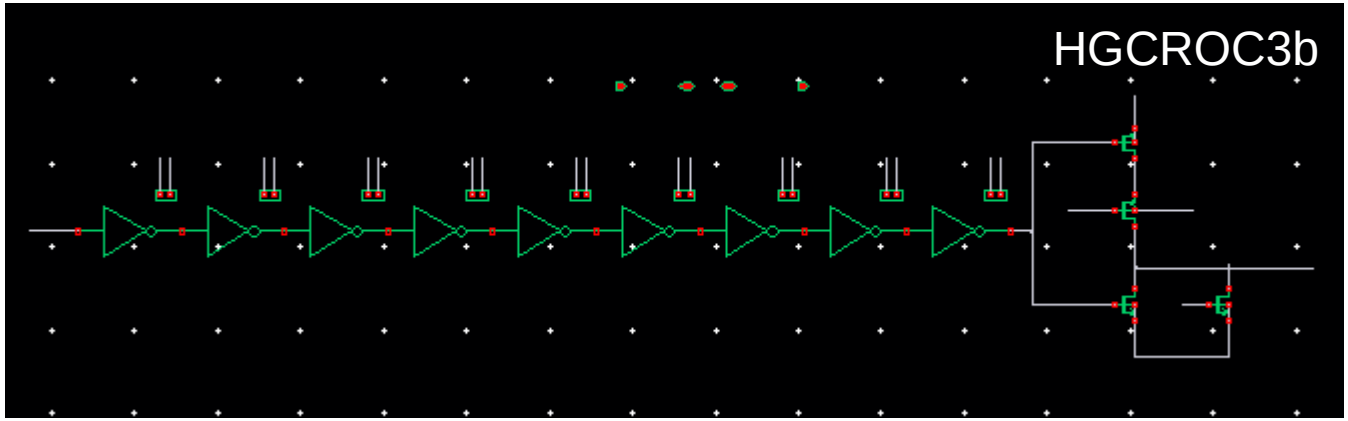




Issue 3: ADC



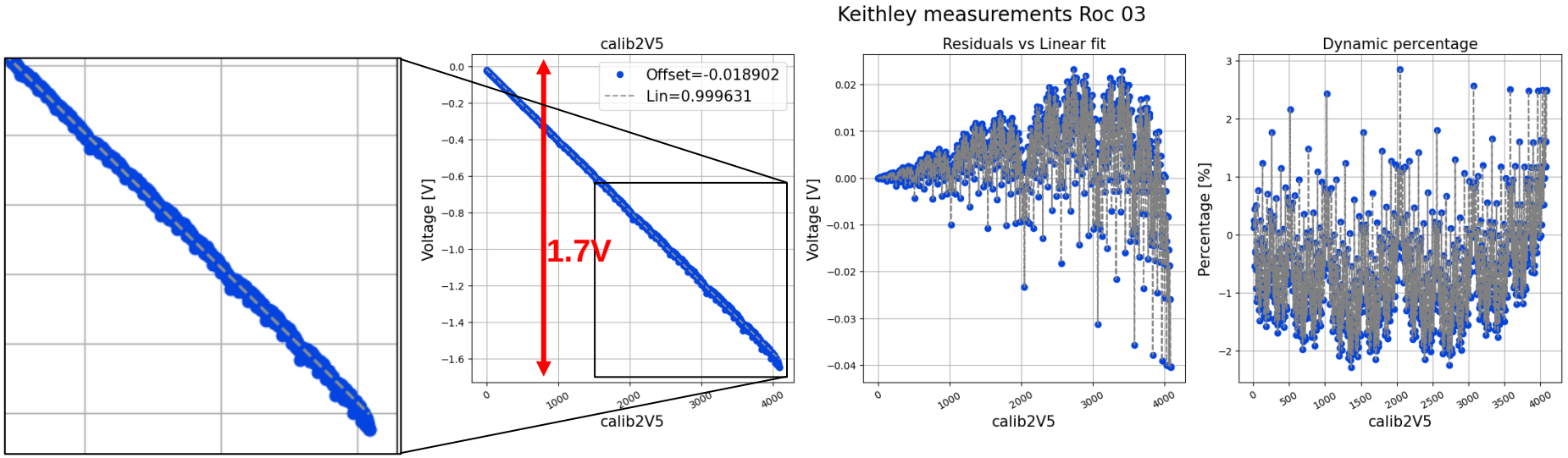
Simulations Monte-Carlo + process corners done



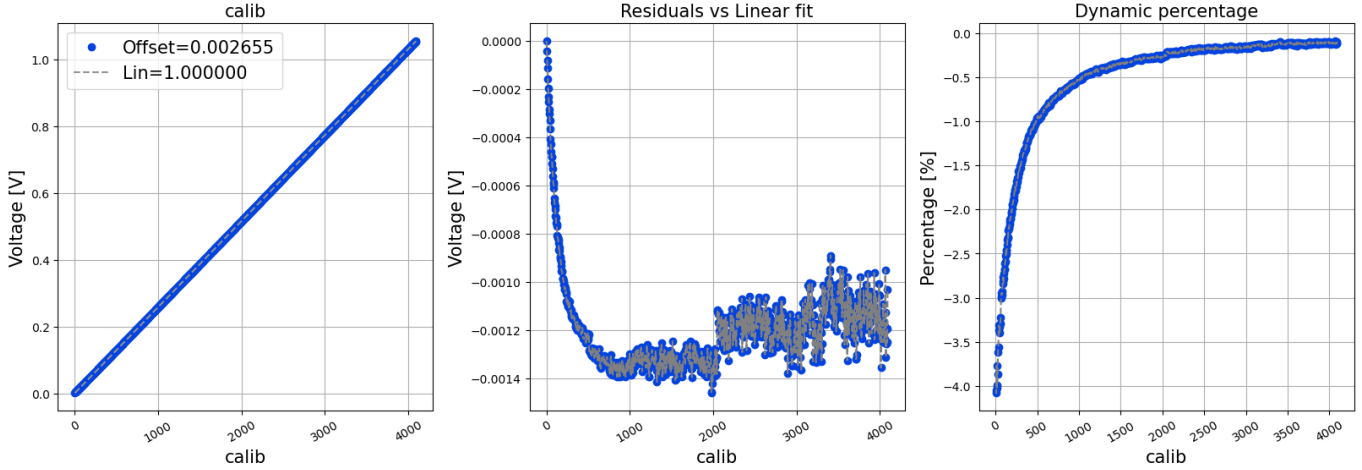
Effects disappear in all corner and MC simulation with this change

Issue 4: SiPM Calibration DAC

Nonlinearities calibdac2V5 especially for larger values.
Dynamic range up to 1.7 V that corresponds to 0 to 200pC injection.

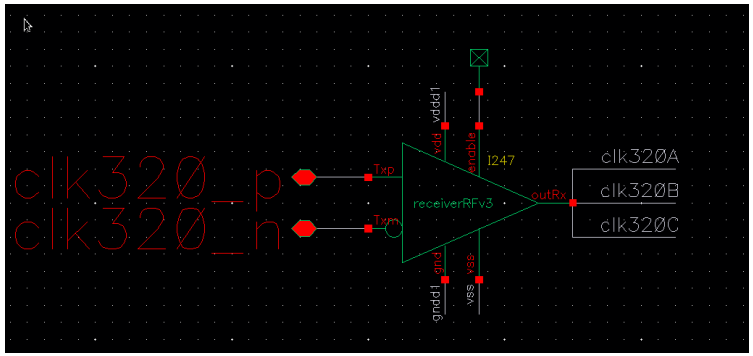


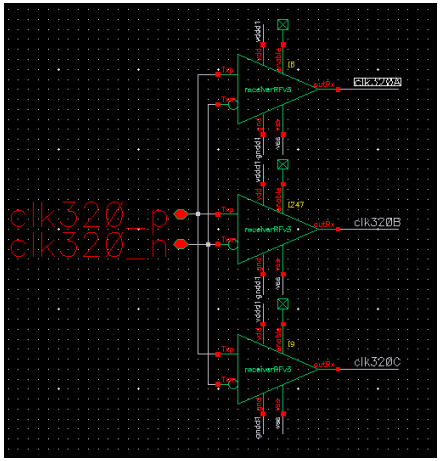
1.2V Calib DAC for injection into the PA doesn't present nonlinearities:



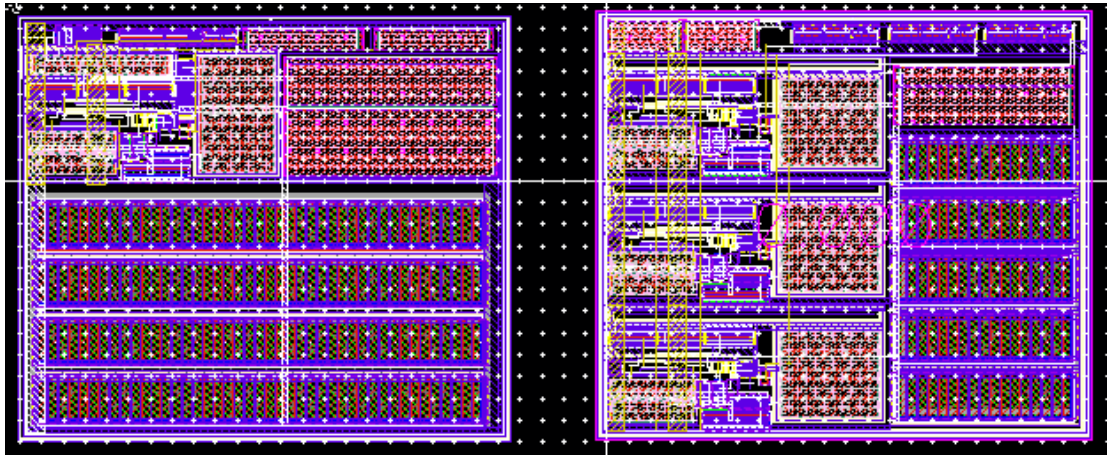
HGCROC3b: Improvements

- **SEU mitigation**
  - Triplication of CLPS receivers for CK320 and FCMD
  - Enable pin removed…





Old



New

  - Capacitance added on sensitive ENABLE/startup nodes (bandgap….). Look/simulate all these nodes in schematic !
  - M7 shielding of ctest line to avoid crosstalk from internal injection

References

[1] CERN (2021).*CMS Detector.* [Online]. Available: https://portail.polytechnique.edu/omega/fr/omega/recherche/cms-hgcal

[2] CMS Collaboration (2018). *The Phase-2 Upgrade of the CMS endcap calorimeter*. CERN-LHCC-207-023, Vols. CMS-TDR-019, pp. 1-364.

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[4] D. Thienpont (2020). *H2GCROC2/2A: architectural overview*. OMEGA Microelectronics. [Online]. Available: https://edms.cern.ch/ui/file/2133536/1/ASIC_parameters_HGCROC_for_SiPM.pdf

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