Characterization of the ATLAS Liquid Argon Front-End ASIC ALFE2 for the HL-LHC upgrade

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Geremeas, Sardinia, Italy

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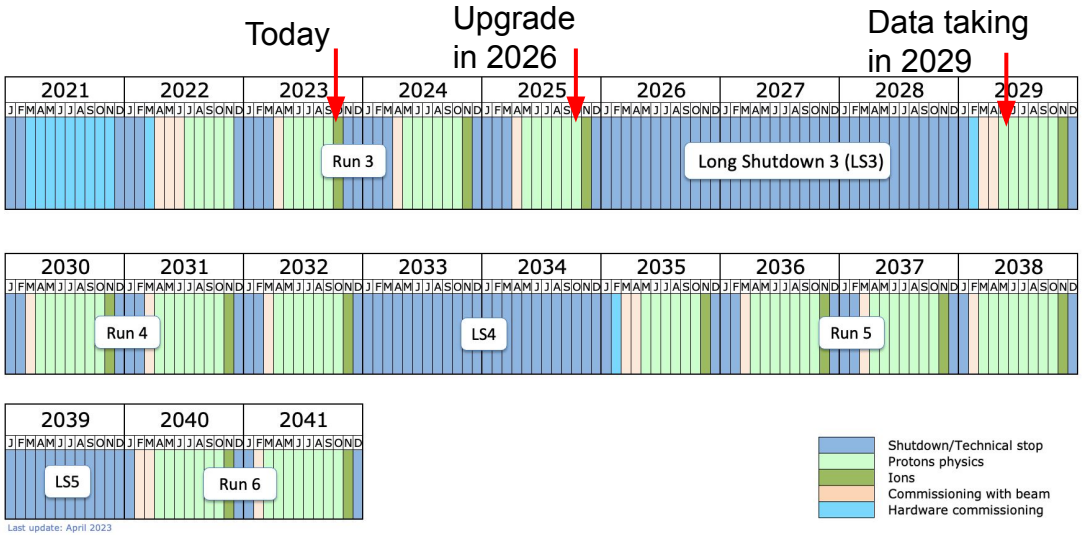
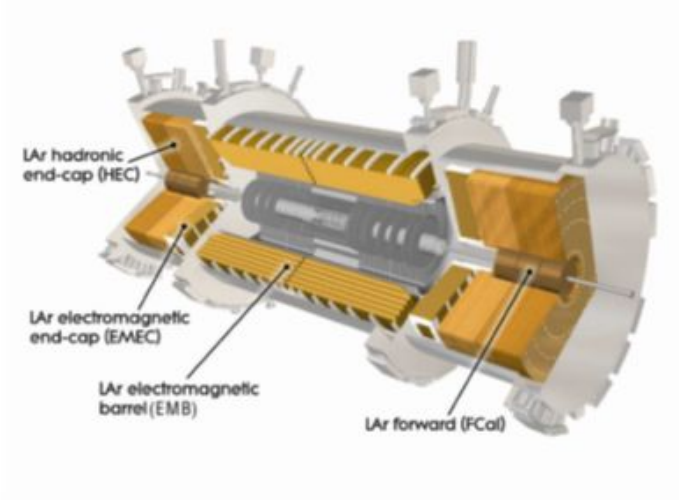
High Luminosity-Large Hadron Collider upgrade

- HL-LHC upgrade with an increased 7x instantaneous luminosity is scheduled to begin operation in 2029.
- ATLAS **Liquid Argon calorimeter** electronics will be upgraded for higher data rates (220 Gbps/FEB2 vs 1.6 Gbps/FEB) and increased radiation hardness



LHC and HL-LHC plan



ATLAS Liquid Argon Calorimeter

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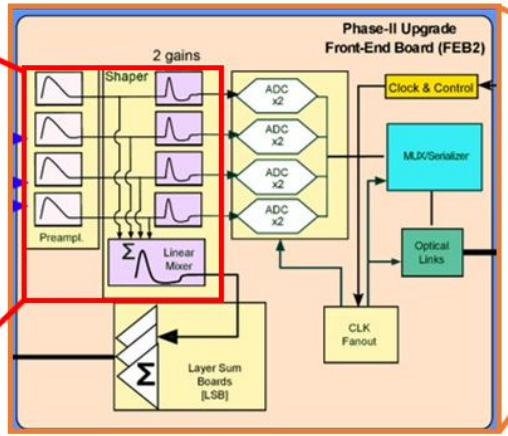
ATLAS Liquid Argon Front-End ASIC

The **ATLAS LAr (Liquid Argon Calorimeter) Front-End (ALFE2)** is an ASIC for the ATLAS LAr Calorimeter

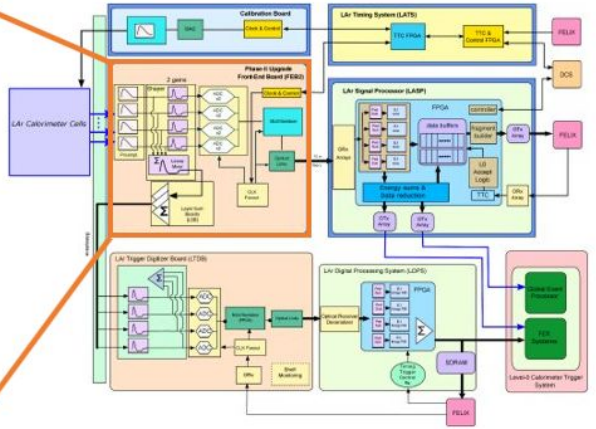
- 4-channel pre-amplifiers (PA) and CR-$(RC)^2$ shapers
- Trigger sum output
- BGA package 196-pin, 0.8 mm pitch, 12 mm x 12 mm

- ~80k chips will be produced
- 1,524 Front-End Boards, 32 chips and 128 channels per board
- Higher trigger rates (1 MHz vs 100 kHz)
- Higher radiation tolerance

ALFE2



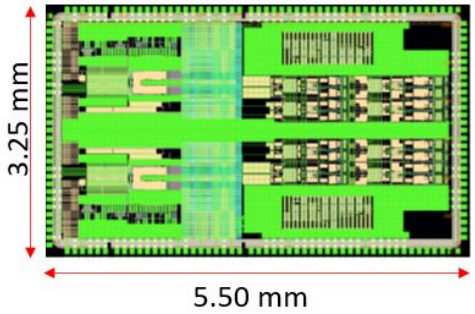
Front-End Board



ATLAS LAr readout electronics

ALFE2 overview

ALFE0

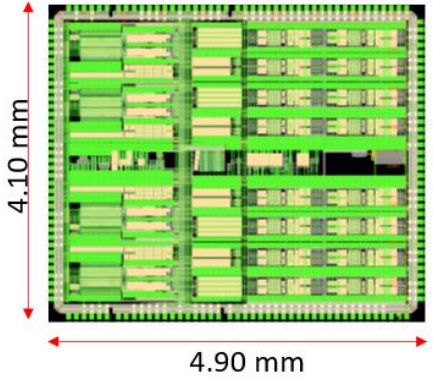


Dual-ch with *Zin* = 25 Ω

- Low noise (ENI ~ 150 nA)
- Low non-linearity (< 0.1%)
- Fully differential preamp architecture

Nov 2018

ALFE1

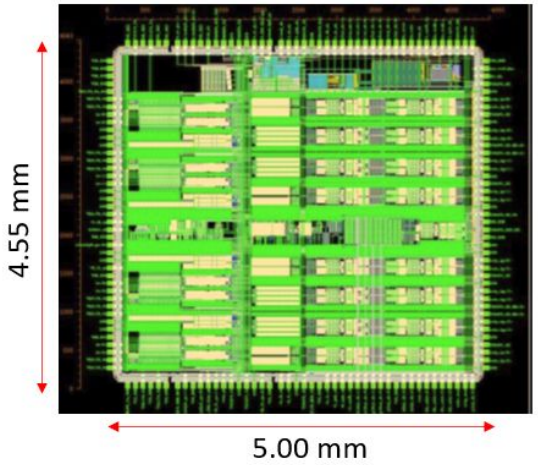


Quad-ch with *Zin* = 25 & 50 Ω

- Zin, peaking time, and baseline configuration
- Channel power-down capability

Nov 2019

ALFE2



Final and production version

- Trigger sum
- SEU-tolerant I2C interface
- DACs
- BGR

March 2021

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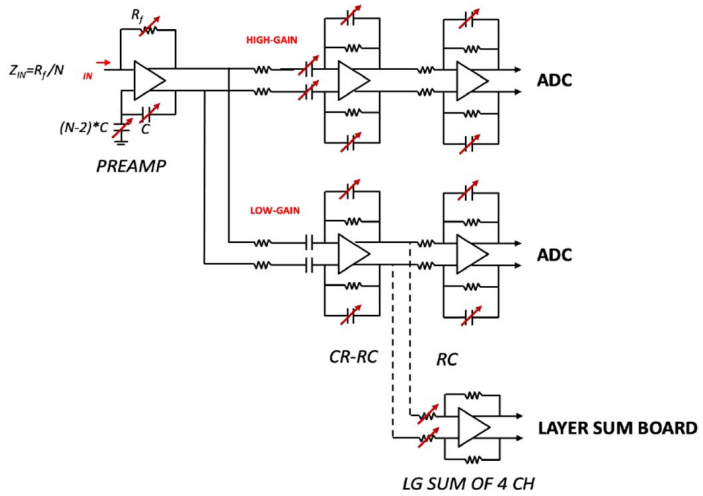
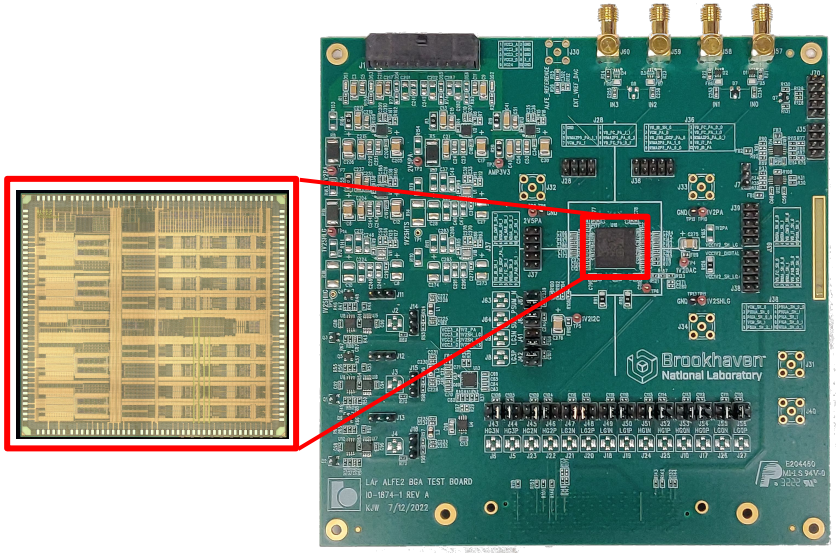
ALFE2 features

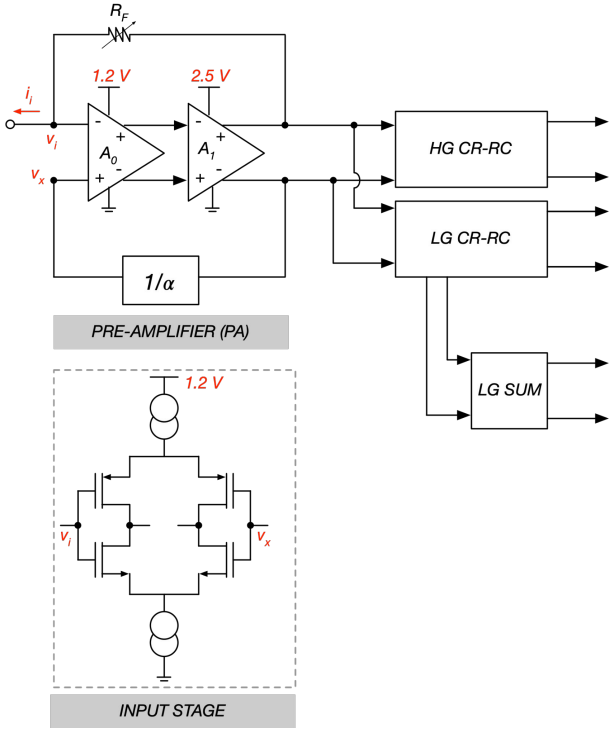
- 16-bit dynamic range (DR) on signal reconstruction and energy resolution requirements
- Each channel has a High-Gain (HG) output and a Low-Gain (LG) output simultaneously
- Reconfigurable (I2C slow control interface)
- Radiation tolerance:
  - Triple modular redundancy - TMR
  - Auto-refresh to correct errors by single event effects



Specifications	
Zin	25 Ω or 50 Ω configurable
Noise	ENI < 350 nA at $\tau_{p\ (5\%-100\%)}$ = 46 ns (25 Ω HG) ENI < 120 nA at $\tau_{p\ (5\%-100\%)}$ = 38 ns (50 Ω HG)
Gain	High Gain / Low Gain ratio: 22 ± 5
INL	± 0.2% on High Gain output ± 0.5% on 80% of Low-Gain dynamic range ± 5% on 100% LG full dynamic range
PSRR	10 dB up to 1 MHz
Power	650 mW
Radiation	TID 140 krad, SEE h/cm2 1.0 x 10^{13}



ALFE2 Channel | Architecture Advantages



- Key block enabling very low-noise performance & high linearity is the Pre-amplifier, which is implemented by means of a Fully-Differential Amplifier (FDA) enclosed in an asymmetric differential feedback [1].
  - FDA is implemented with inverter-based input pair [2], which gives √2 noise improvement vs traditional FDA (implemented e.g. in [1])
  - FDA is multi-power-domain with input pair biased at 1.2 V and output stage at 2.5 V. This allows (1) minimization of power consumption and (2) increase of transimpedance gain (R_F), which reduces noise contribution from the shaper.

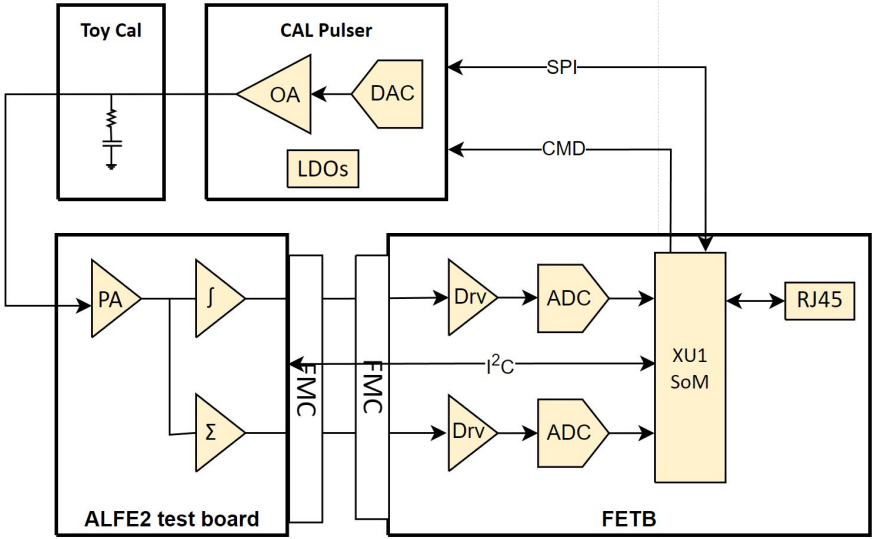
Key PA & Channel Architecture advantages:

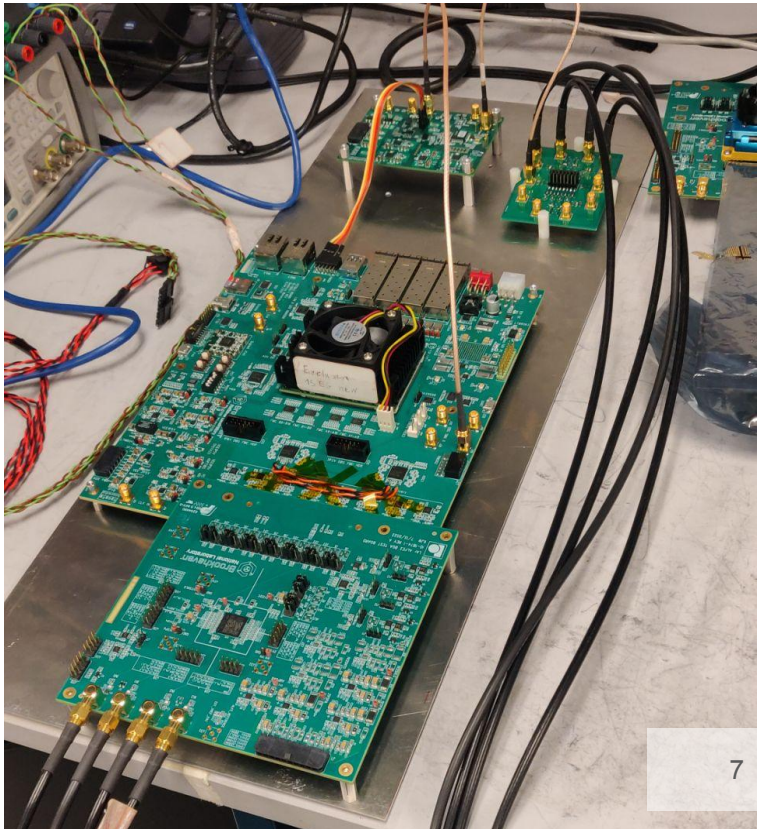
- Signal flows only through passive components
  - Very linear & very stable termination
- Fully-differential architecture
  - Doubles the voltage swing (reduction of noise from the shaper)
  - FE much less sensitive to common mode noise e.g. from input pair current sources, power supply or coupling on the PCB

[1] G. De Geronimo et al, "HLCI: A Front-End ASIC for Liquid Argon Calorimeters," *2017 IEEE NSS/MIC,* Atlanta, GA, USA, 2017, pp. 1-3, doi: 10.1109/NSSMIC.2017.8532699.
[2] M. Dabrowski, "Fully Differential Rail-To-Rail Output Amplifier with Inverter-Based Input Pair", US Patent US11336244B2, May, 2022

Test Setup

- A **Front-End Test Board (FETB)** was designed, based on Enclustra Mercury XU1 (Xilinx's Zynq Ultrascale+™ MPSoC)
- Integrates 2x 8ch, 16-bit ADCs with 13-bit ENOB, 125 MSPS (TI ADS52J65)
- Runs Petalinux for data taking and analysis
- Has an Ethernet interface for radiation testing
- Used for both characterization, QC tests and irradiation tests

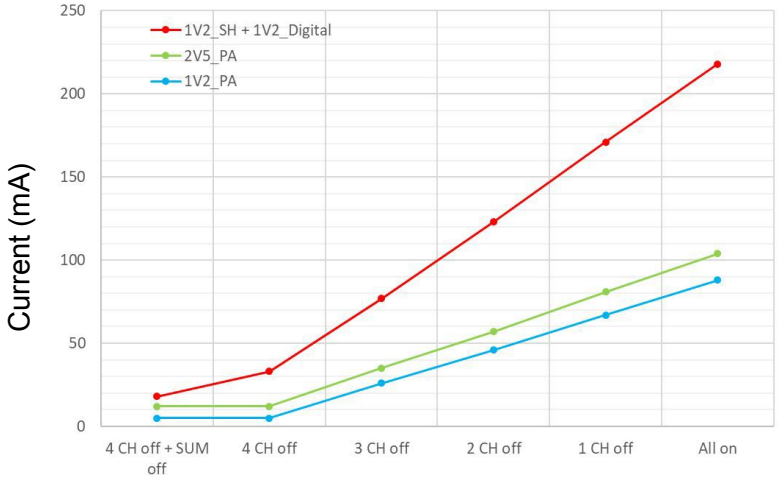




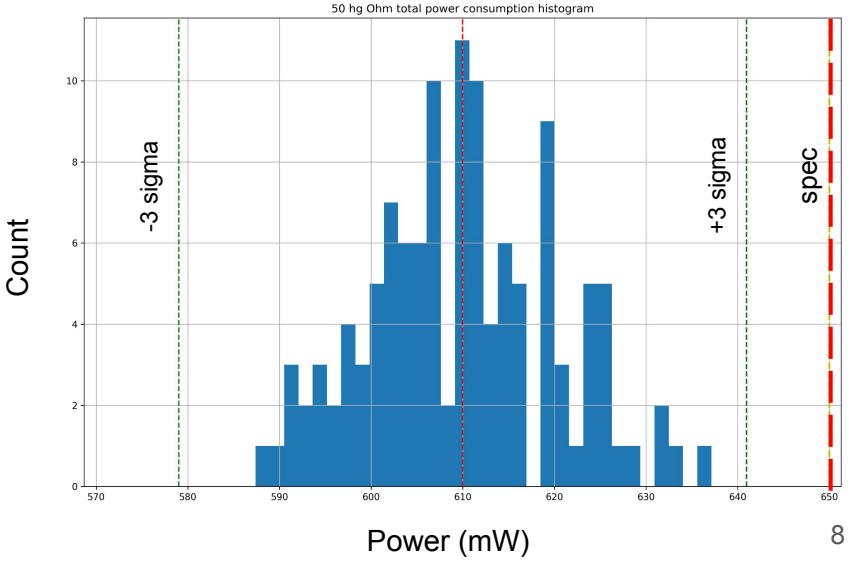
Test results - power consumption

- Average power consumption is ~610 mW, matches simulation results.
- Analog channels can be powered off individually.
- **All chips measured meet the specification.**

	Specifications	Measurement
Power (mW)	650	610 ± 11 (mean ± σ)



Histogram of the total power consumption of ALFE2 (120 chips)



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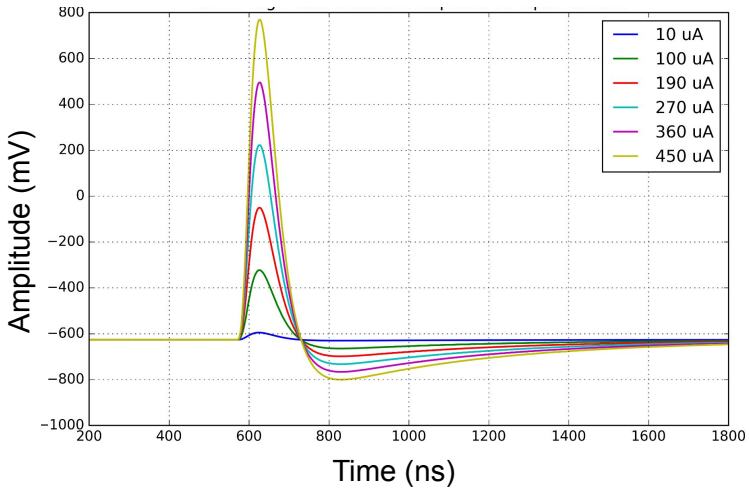
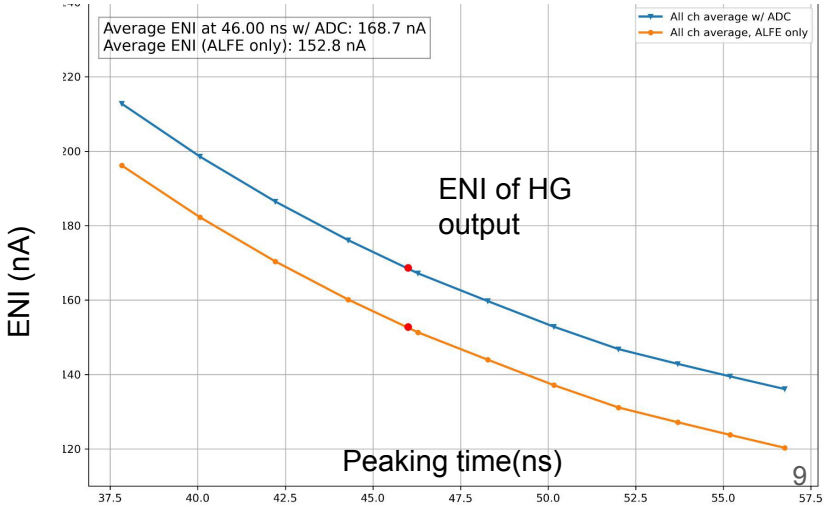
ALFE2 test results - Noise, gain

- Measured equivalent noise input (ENI) at reference conditions, with input protection network installed, including ADC contribution:
  - **~170 nA**, 25 Ω mode
  - **~50 nA**, 50 Ω mode
- **The measured performance greatly exceeds specification requirements.**



ALFE2 high gain output at different input signals. Phase has been interpolated 18 times.

	Specifications	Measurement
Noise	ENI < 350 nA at $T_p^{5\text{-}100}$ = 46 ns (10 mA) ENI < 120 nA at $T_p^{5\text{-}100}$ = 38 ns (2 mA)	~170 nA ~50 nA
Gain	High Gain / Low Gain ratio: 22 ± 5	~22.5



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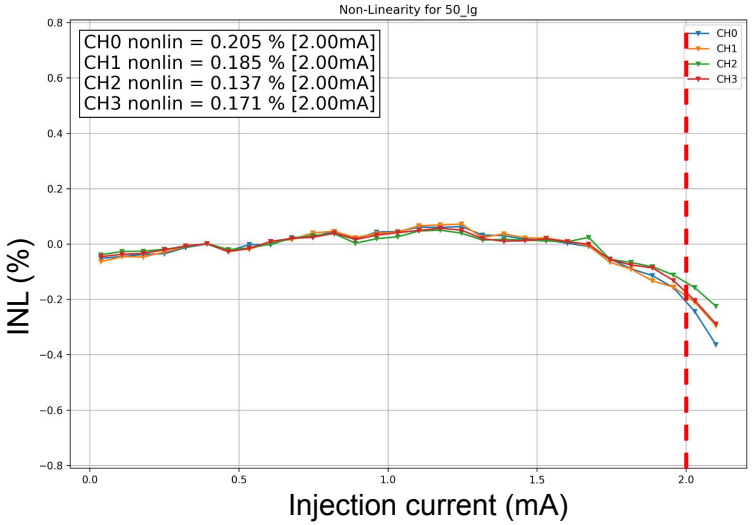
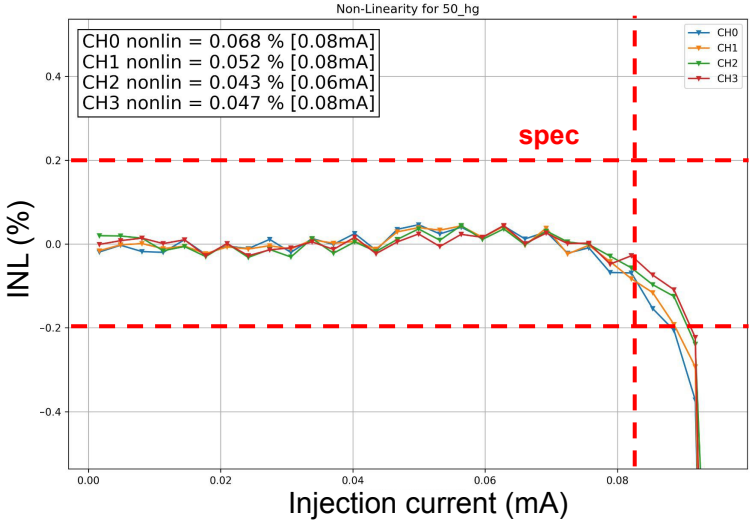
ENI definition: $\frac{\text{RMS of pedestal run}}{\text{Gain}}$

ALFE2 test results - Linearity

- Measured using the IN2P3/OMEGA calibration pulser and a 16-bit TI DAC8830
- **The measured performance meets specifications**

	Specifications	Measurement
Linearity (INL)	< ± 0.2% on HG < ± 0.5% on 80% of LG dynamic range < ± 3% on the full dynamic range	< 0.15% (HG) < 0.25% 80% of LG Dyn Range < 0.6% of LG





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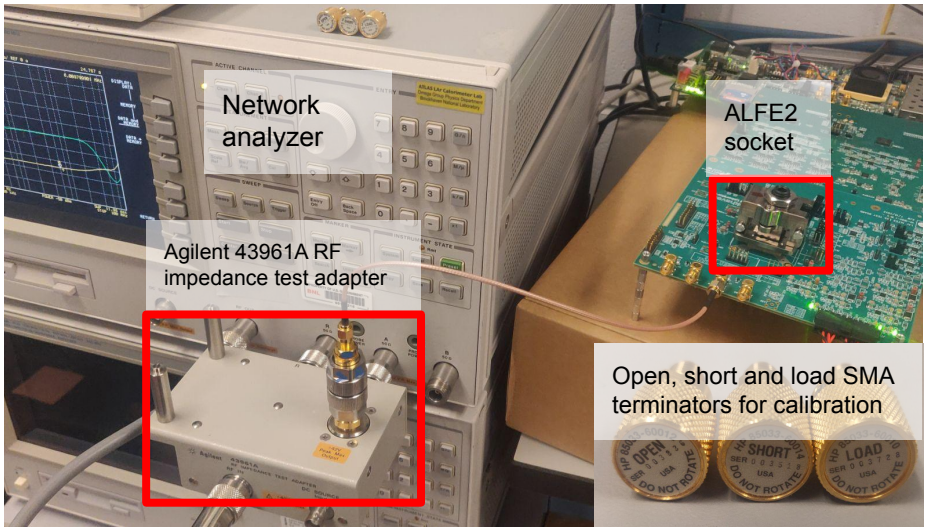
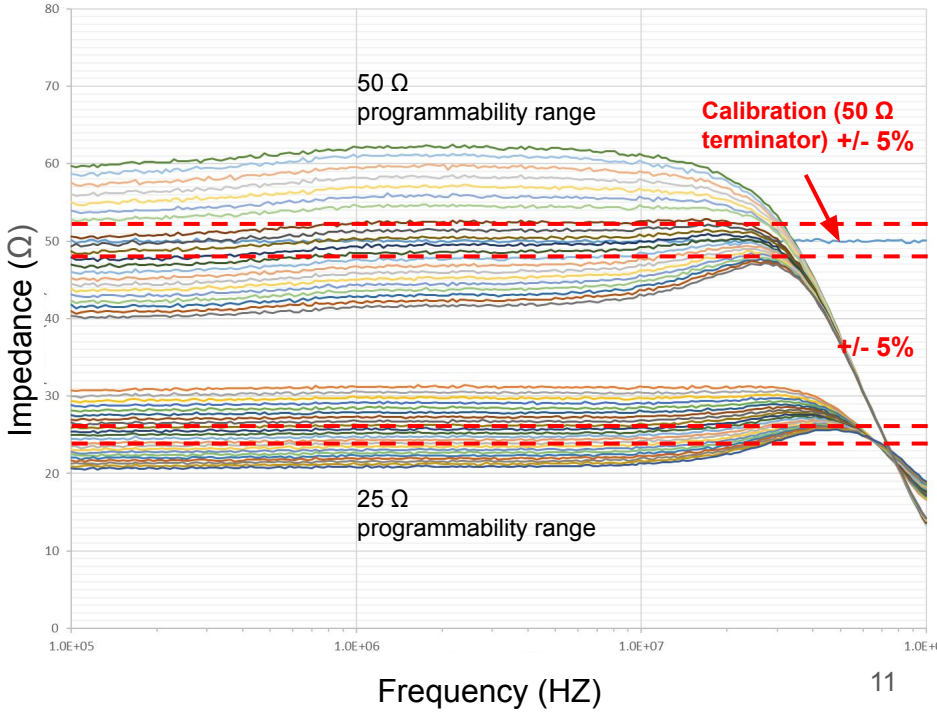
Test results - input impedance

- The input impedance was measured with a network analyzer (HP 4395A).
- The measured performance meets the specifications.

	Specifications
Zin	25/50 Ω configurable Adjustable (step 1 Ω) Stable 5% up to 20 MHz





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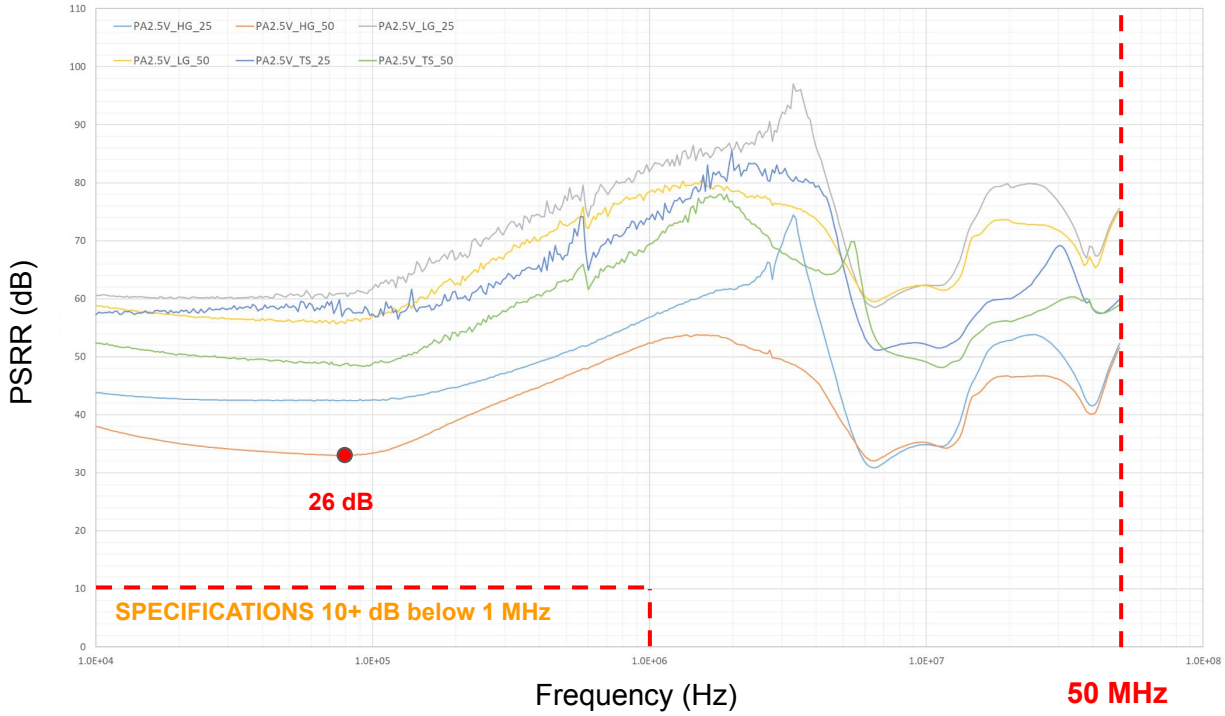
Test results - Power Supply Rejection Ratio

- The power supply rejection ratio (PSRR) was measured with a network analyzer (HP 4395A).
- The measured PSRR is higher than 26 dB up to 1 MHz for all power rails.
- The measured performance meets the specifications.



Power supply rejection ratio measurement for 2.5V power rail

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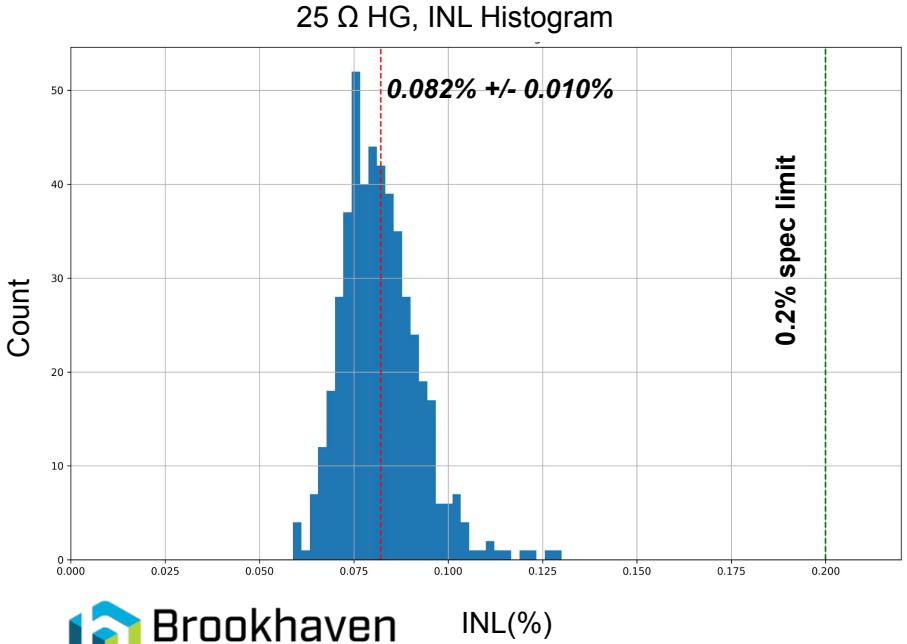
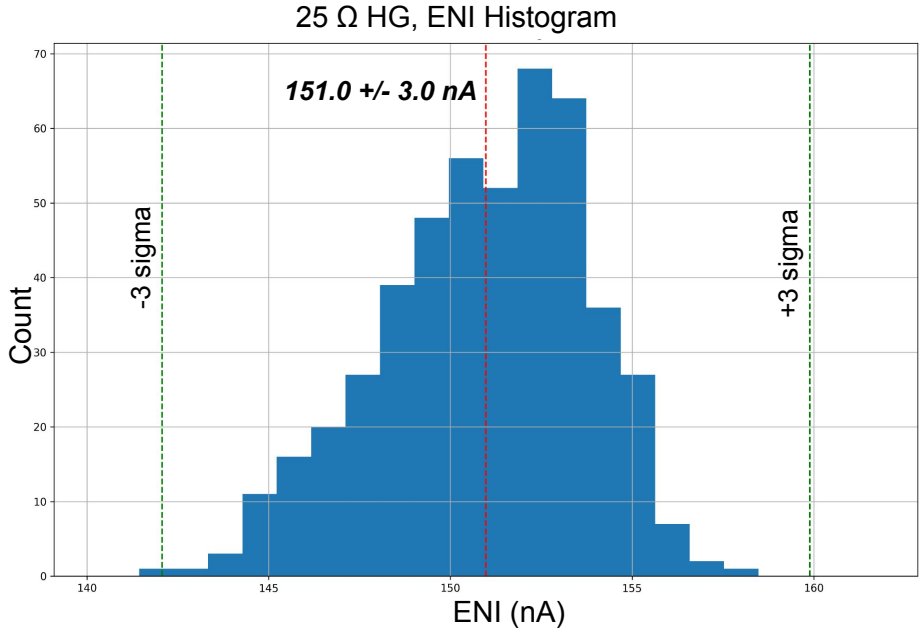
Test results - uniformity and yield

- 120 pre-production chips were tested, no errors on slow control interface observed
- 5 chips rejected with 3 sigma stringent rules. ~96% yield
- **All 120 chips meet the specifications**





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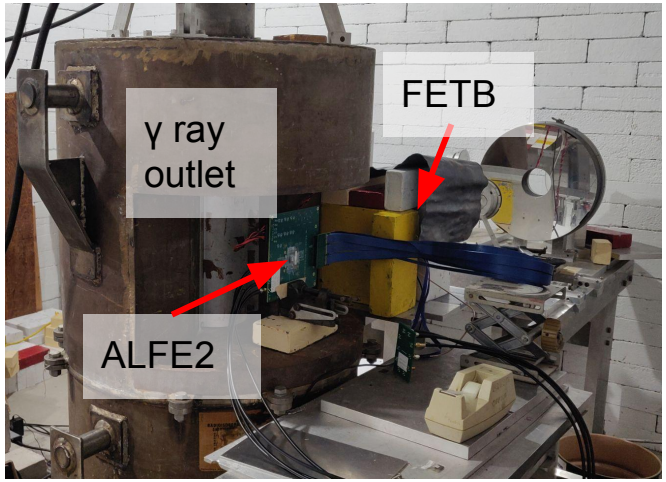
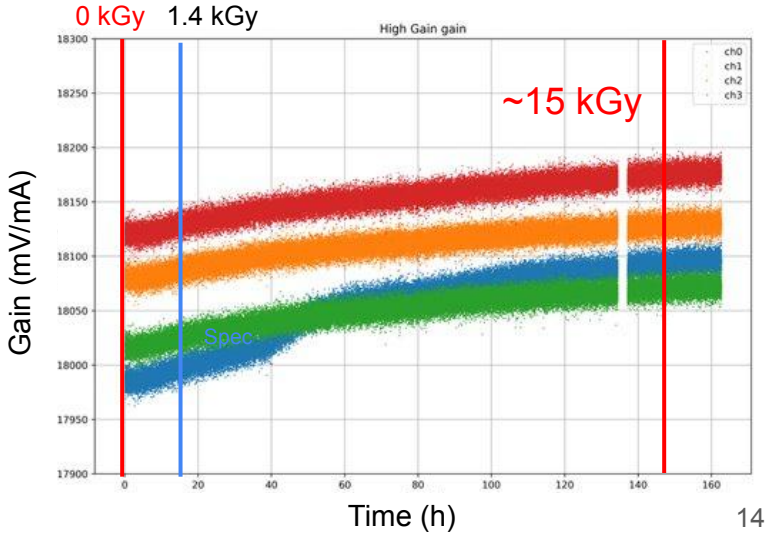
ALFE2 Radiation testing

- ^{60}Co gamma ray source, at Brookhaven National Lab
- Real time monitoring of temp, voltages, chip performance and slow control interface
- 10 kRad/h
- 10x of the target dose
- < 1% performance change observed

Radiation tolerance with safety factors		
	TID [kGy]	NIEL [n_{eq}/cm^2]
ASIC Barrel	1.4	4.1×10^{13}
ASIC Endcaps	0.21	6.0×10^{13}





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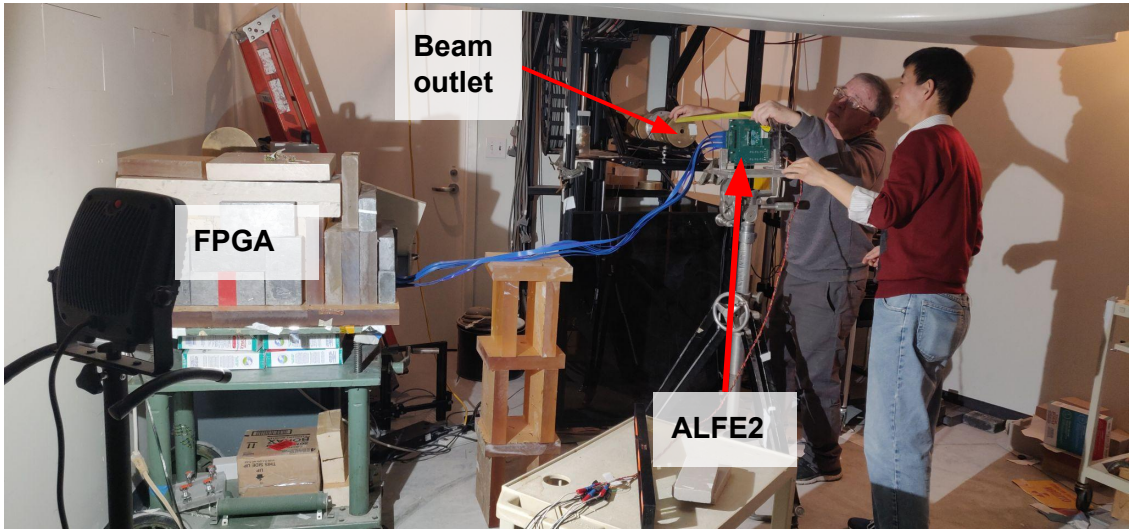
Test results - Single Event Effect (SEE) Test

- An SEE test was conducted in Massachusetts General Hospital in Boston in April 2023.
- Internal registers of ALFE2 were continuously written/read in the 226 MeV proton beam.
- Seven chips were tested (4 with auto-refresh on, the other 3 auto-refresh off).
- **No errors observed** with auto-refresh on. The estimated cross-section:
  $< 1.35 \times 10^{-16}$ cm^2/bit (combined, 95% confidence level)
  Extrapolated error rate for the entire ATLAS LAr calorimeter: **< 5 errors per day** (95% CL)

Radiation tolerance with safety factors

	NIEL [n_{eq}/cm^2]	SEE[h/cm^2]
ASIC Barrel	4.1×10^{13}	1.0×10^{13}
ASIC Endcaps	6.0×10^{13}	1.2×10^{12}



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Summary

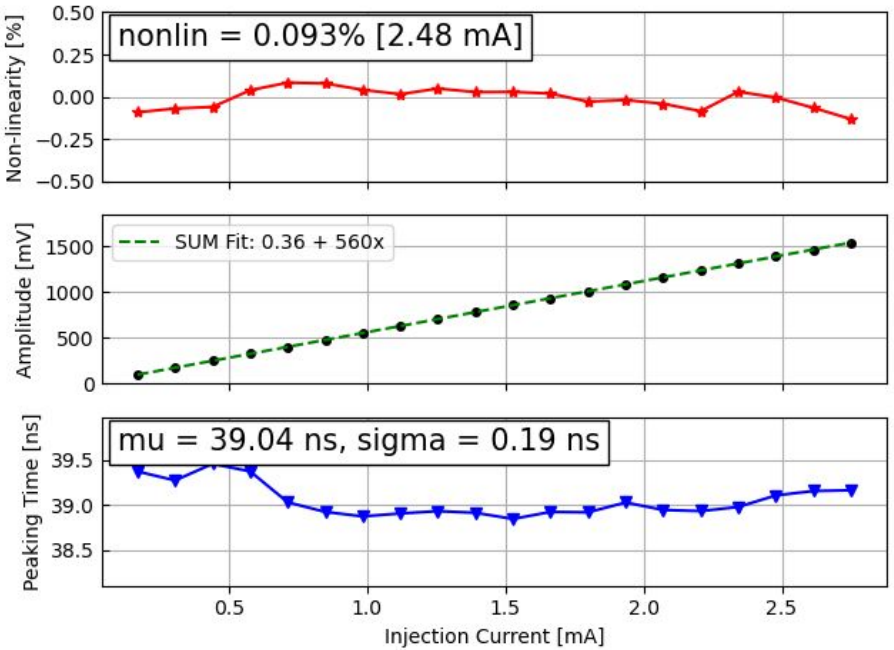
- ALFE2 is developed for ATLAS LAr Phase-2 upgrade and characterized with the Front-End Test board
- ALFE2 design meets and exceeds all requirements for the ATLAS LAr Calorimeter in the HL-LHC upgrade
  - Measured ENI ~170 nA for 25 Ω mode, ~50 nA for 50 Ω mode (Spec: 350 nA / 120 nA)
  - Measured INL < 0.6% for Low Gain, < 0.15% for High Gain
  - Trigger summing output working as expected and meets all specifications
  - Power consumption is 610 mW (spec 650 mW)
- TID tests were completed with ^{60}Co gamma ray source. <1% performance change observed with doses exceeding 1.5 MRad (10x times the spec)
- SEE test was completed with no errors observed when the auto-refresh feature was on. The extrapolated error rate for the entire ATLAS LAr calorimeter is < 5 errors per day (95% CL)
- The evaluation of pre-production chips is completed. Production is expected to start in the coming month.

Backup slides

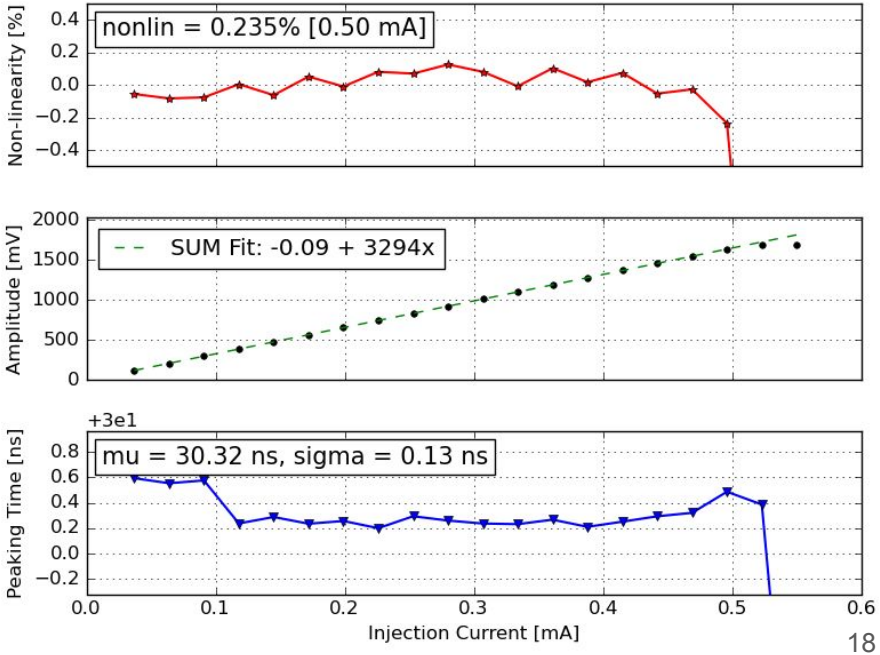
Test results - Trigger sum - INL

- INL requirement for trigger sum: ± 2%
- The measured performance meets specifications

25 Ω, 270 Ω injection resistance

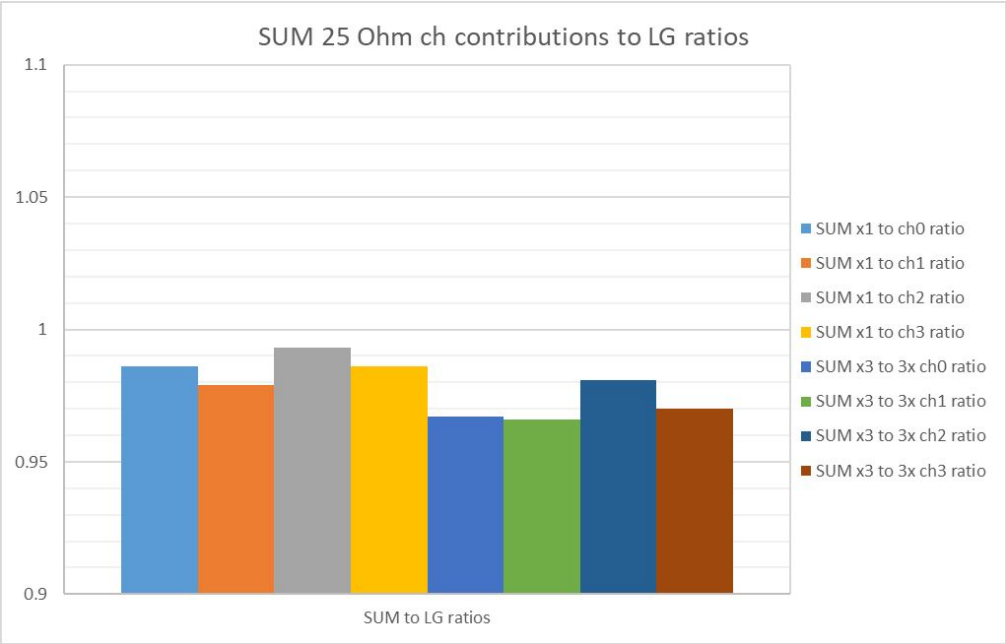


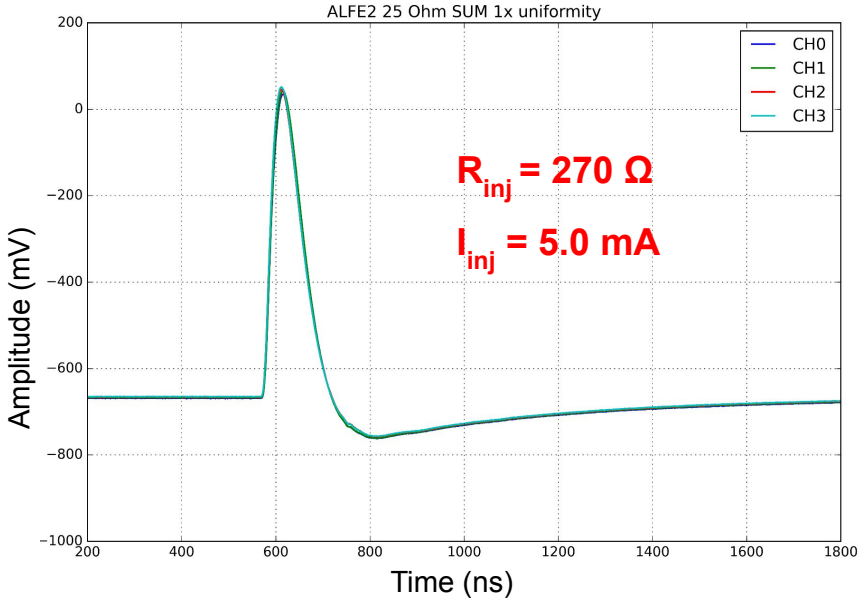
50 Ω, 1300 Ω injection resistance



Test results - Trigger sum - Channel uniformity

- Requirement for gain uniformity of the channels summed: < 5%
- The measured performance meets specifications





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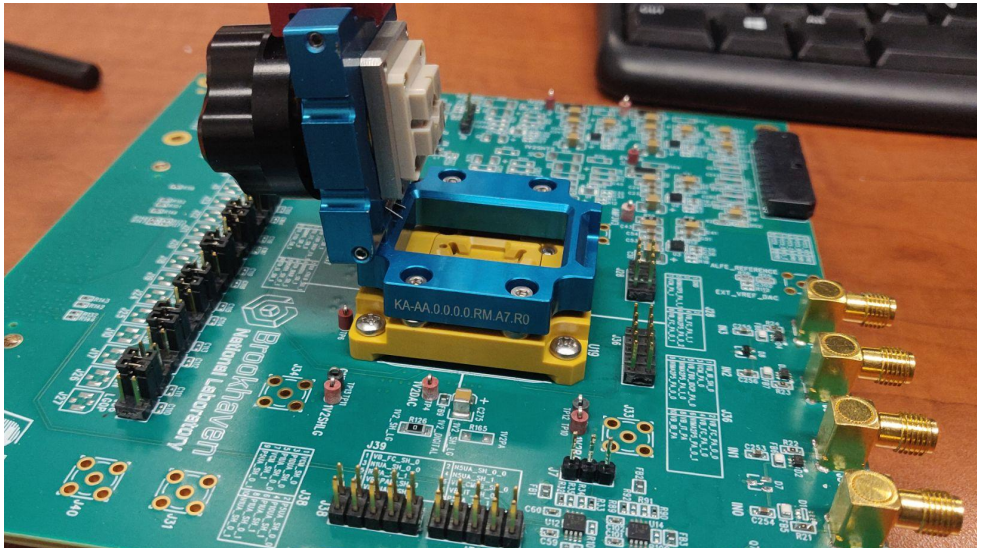
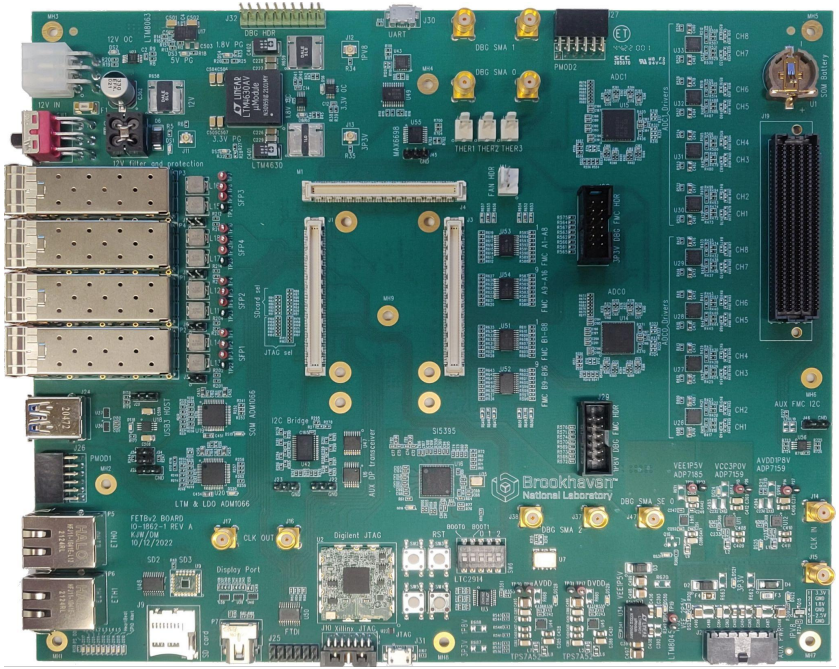
Front-End Test Board and ALFE2 socket





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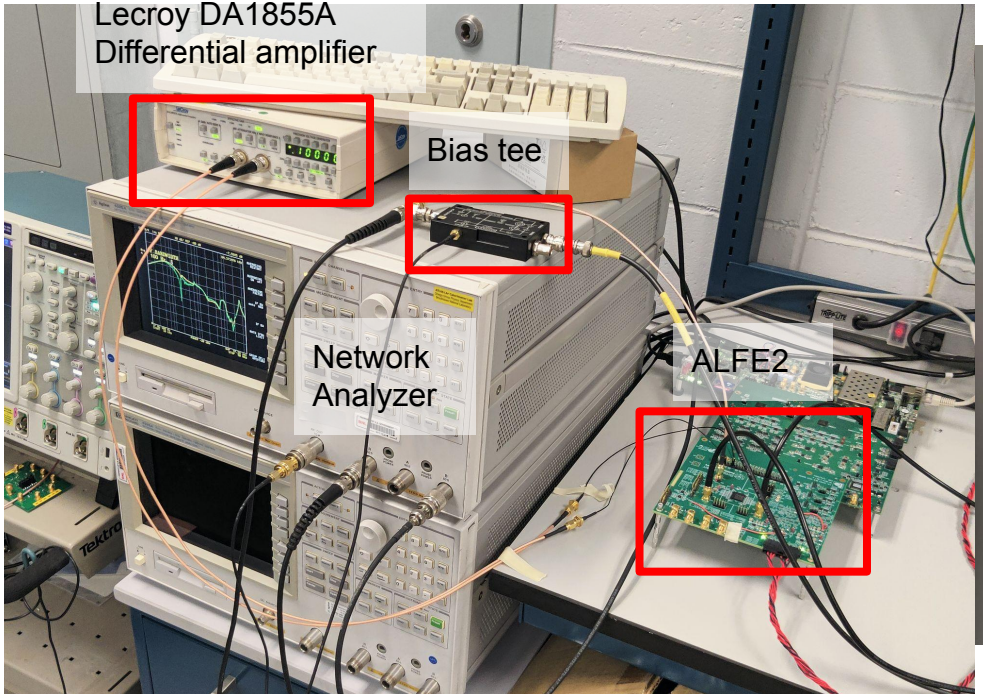
PSRR measurement test setup



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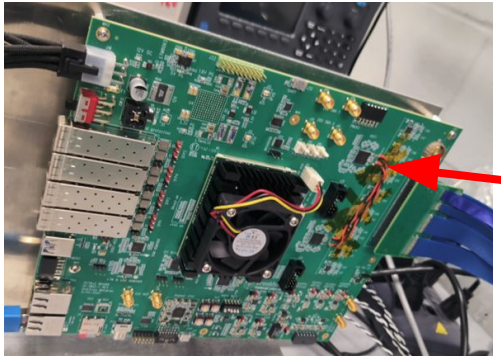
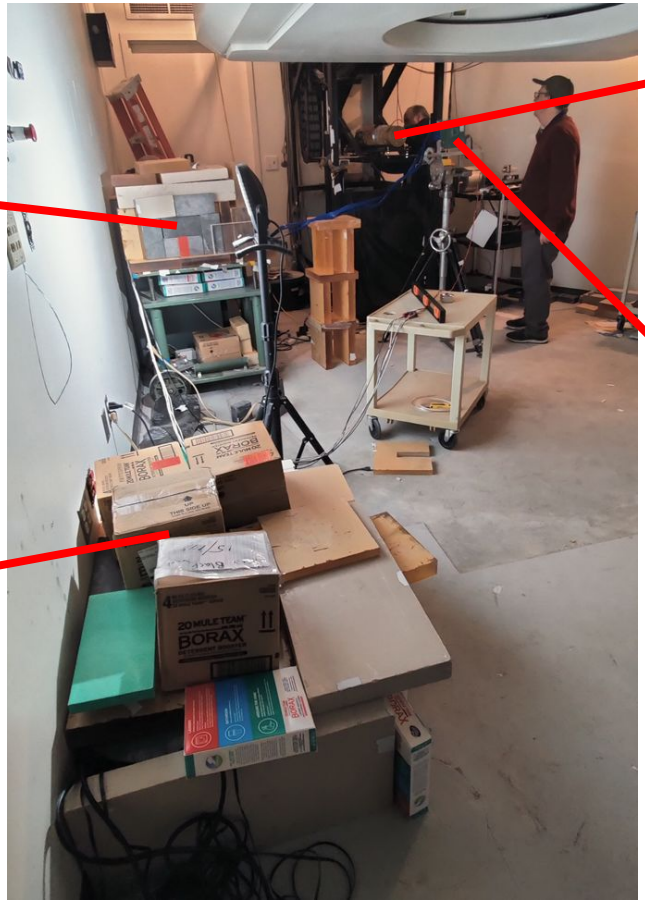
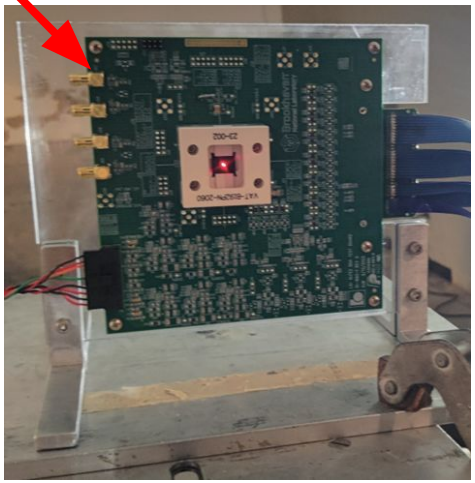
SEE test setup







Beam outlet

- Particle : 226 MeV proton
- Beam diameter: 1.5 cm
- Flux: 7E9 - 3.5E10 p/cm^2/s

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Power: PSRR measurement on ALL RAILS, outputs 25 Ω and 50 Ω

This plot shows all PSRR measurements for:

- VDD1P2_PA
- VDD2P5_PA
- VDD1P2_SH

Both 25 Ω and 50 Ω configurations, high gain, low gain and trigger sum outputs were tested.