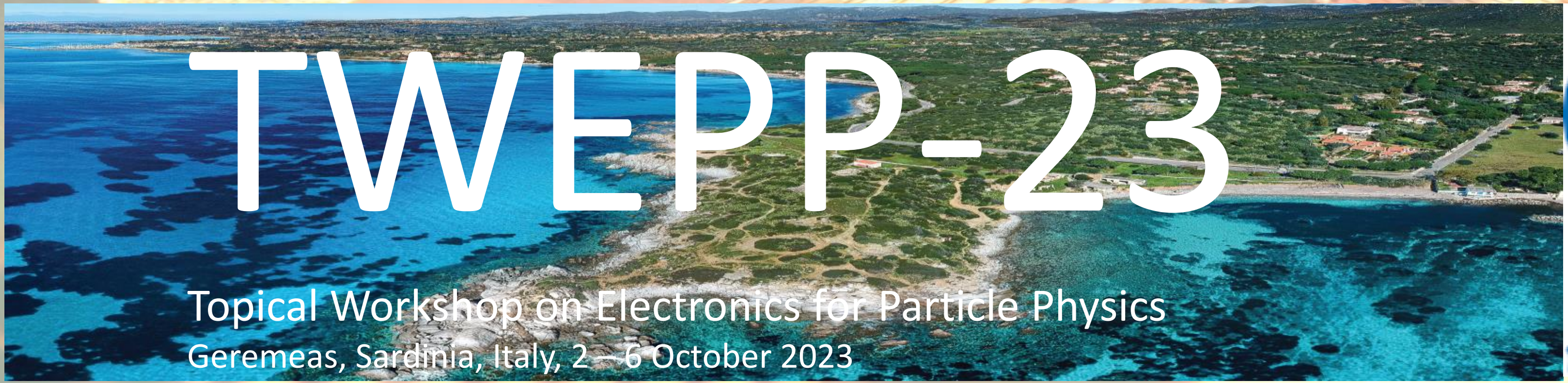
Chips dedicated to the upgrade of ATLAS LAr calorimeter Calibration

Ludovic Raux

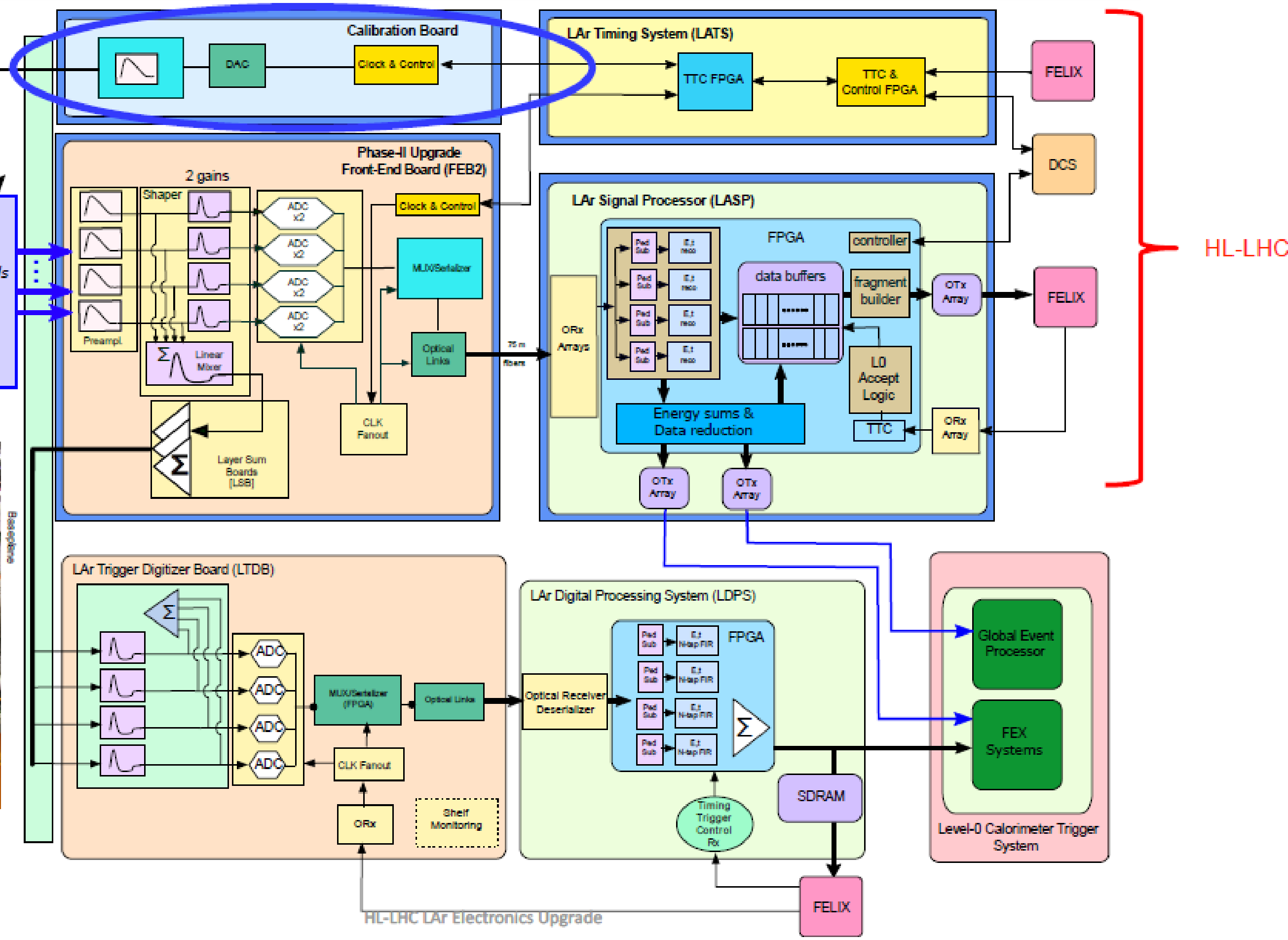
on behalf of Lar Calibration team



HL-LHC Readout - Calibration System

Calibration system :

- Send precise pulses to the 200 000 channels of the Lar calorimeters
- The upgrade to HL implies to redo electronics
- Will be placed in the existing crates
- Integrated in new control system (LpGBT)

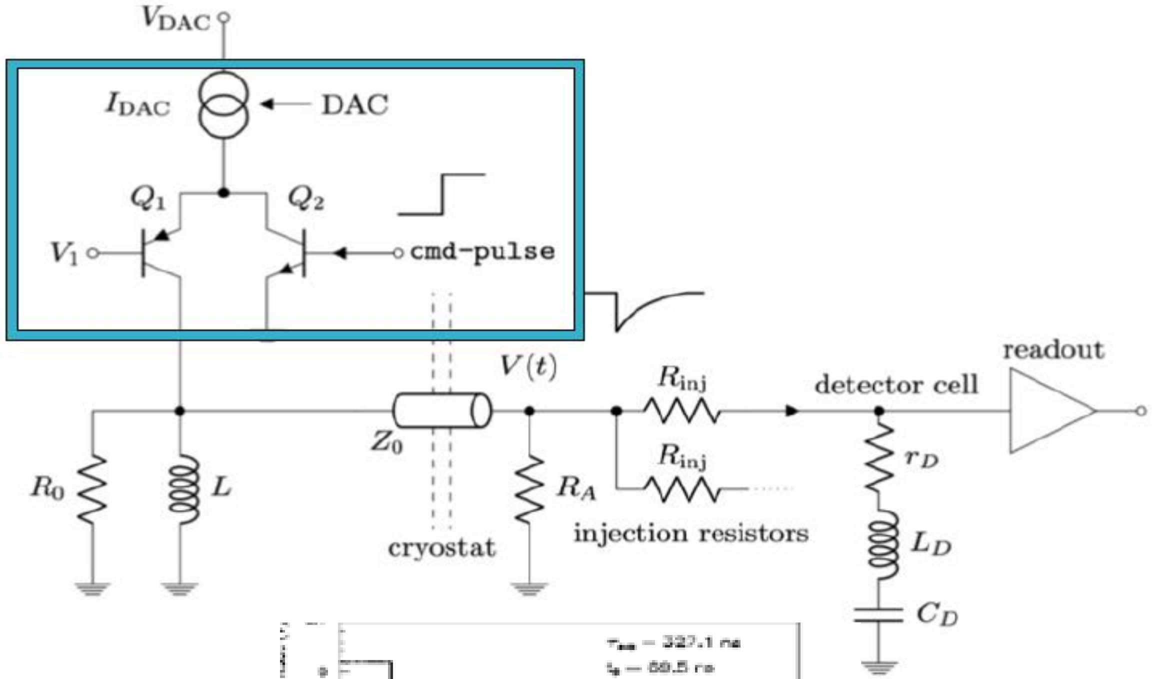


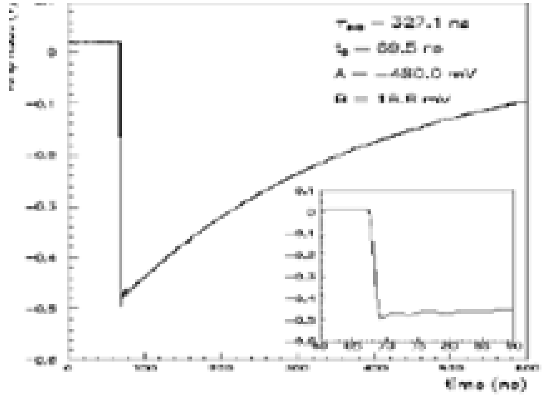
Calibration principle and specifications

The calibration system must provide a high precision test pulse in each channel of the electromagnetic LArg calorimeter.

Pulse specifications:

- **High dynamic range : 16 bits (from 5µA to 320mA)** =>(-8V on 25 Ohms)
- INL : **+/-1LSB** until 10 bits and **1‰** from 10 to 16bits
- Non uniformity between channels < 2.5‰
- Pulse rise time < 1ns
- **Rad hard** until 1.4 kGy (140Krad) (TID) and $4.1\text{x}10^{13}$ neq/cm^2 (NIEL)





Developments for calibration upgrade: ASICs evolution in 4 steps

CLAROC and LADOC timeline

2017 — STEP 0

CLAROC1

XFAB 180 nm
HF switch

Commercial DAC

Test Vehicule:
to evaluate the XFAB technology

2019 — STEP 1

CLAROC2

XFAB 180 nm

HF switch | **13-bit DAC**

1st complete prototype
with HF switches and DAC
Both XFAB 180 nm

2021 — STEP 2

CLAROC3

XFAB 180 nm
HF switch

LADOC1

TSMC 130 nm
13-bit DAC

2^{nd} **prototype** with **HF switches and DAC** functions **in 2 different chips** and **in different technology**
HF switches in XFAB 180 nm
13-bit DAC in TSMC 130 nm

2022 — STEP 3

CLAROC4

XFAB 180 nm
HF switch

LADOC2

TSMC 130 nm
16-bit DAC

3^{rd} **prototype** with two separated chips, still with different techno.
HF switches in XFAB 180 nm
16-bit DAC in TSMC 130 nm

Developments for calibration upgrade: ASICs evolution in 4 steps

CLAROC and LADOC timeline

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HF switch

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XFAB 180 nm
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2[nd] **prototype** with **HF switches and DAC** functions **in 2 different chips** and **in different technology**
HF switches in XFAB 180 nm
13-bit DAC in TSMC 130 nm

2022
STEP 3

CLAROC4

XFAB 180 nm
HF switch

LADOC2

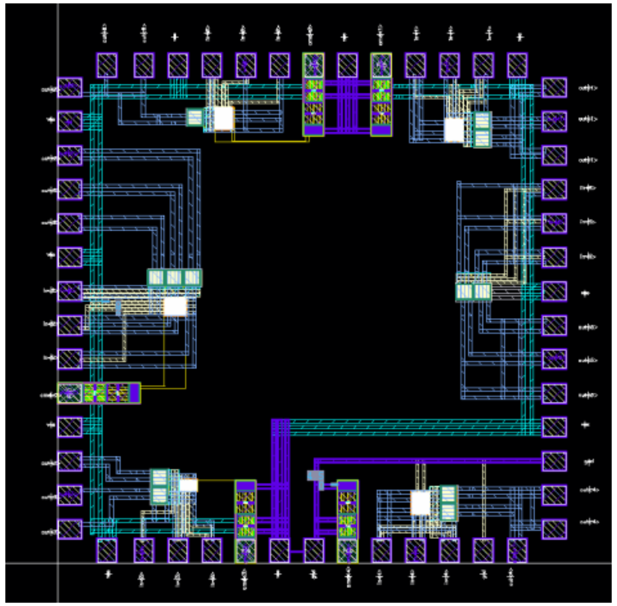
TSMC 130 nm
16-bit DAC

3[rd] **prototype** with two separated chips, still with different techno.
HF switches in XFAB 180 nm
16-bit DAC in TSMC 130 nm

CLAROC1 design and results

Chosen technology : **XFAB XT018** (180nm CMOS HV SOI)

- SOI to enable - 8V pulses
- HV for 5 and 10V MOS
- 6 metal layers to drive more than 320mA

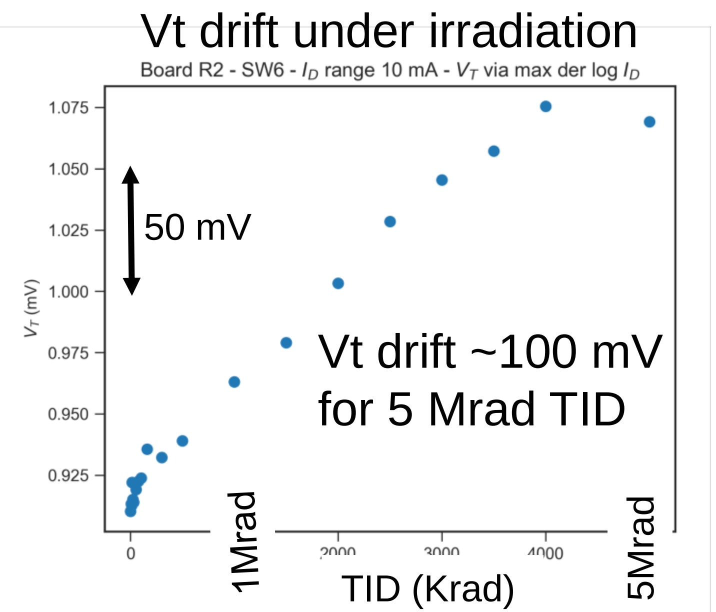


CLAROC1 (2017) : **C**alibration of **L**iquid **Ar**gon **O**utput **C**hip

- **Test vehicle** to explore this unfamiliar technology
- Evaluate its radiation hardness
- 6 different HF switches (size, type, grounding) to choose the best one

→ **Good behavior in irradiation test :**

Irradiation up to 5 Mrad does not degrade switch performance.



- 5V NMOS as command transistor (W/L=3mm/500nm)
- 10V PMOS as switch (W/L=3mm/500nm)

Developments for calibration upgrade: ASICs evolution in 4 steps

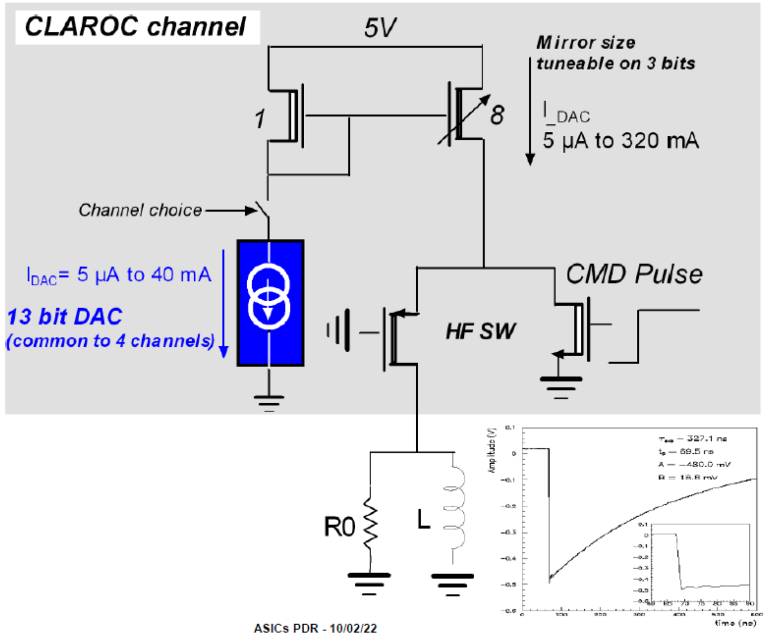
CLAROC and LADOC timeline

2017 STEP 0	2019 STEP 1	2021 STEP 2	2022 STEP 3
CLAROC1	CLAROC2	CLAROC3	CLAROC4
XFAB 180 nm HF switch	XFAB 180 nm HF switch / 13-bit DAC	XFAB 180 nm HF switch	XFAB 180 nm HF switch
Commercial DAC		LADOC1 TSMC 130 nm 13-bit DAC	LADOC2 TSMC 130 nm 16-bit DAC
Test Vehicule: to evaluate the XFAB technology	**1st complete prototype** with HF switches and DAC **Both XFAB 180 nm**	2nd **prototype** with **HF switches and DAC** functions **in 2 different chips** and **in different technology** HF switches in XFAB 180 nm 13-bit DAC in TSMC 130 nm	3rd **prototype** with two separated chips, still with different techno. HF switches in XFAB 180 nm **16-bit DAC** in TSMC 130 nm

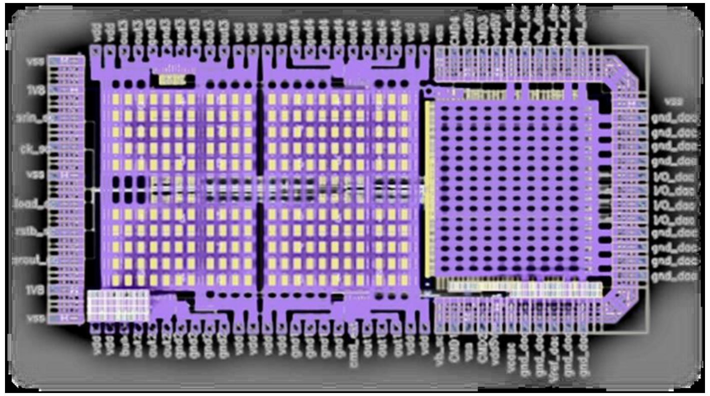
CLAROC2 principle

CLAROC2 complete chip in XFAB :

- **4 channels with HF switches**
- **16-bit DAC current :**
  - **A 13-bit DAC =** 10-bit DAC made by scaled current mirrors for the 10 LSB (5µA to 5mA) for precision + 7 current mirror thermometers for the 3 MSB (5mA to 40mA)
  - **3-bit tuneable gain (1 to 8) current mirror** in each channel to choose the dynamic range (0 to 40mA, to 80mA, …to 320mA)
- **shift register** for chip configuration (1.2V MOS transistors)
  - 17 bits for 13-bit DAC
  - 8 bits for current mirror (common for the 4 channels)
  - 4 bits to validate the 4 channels

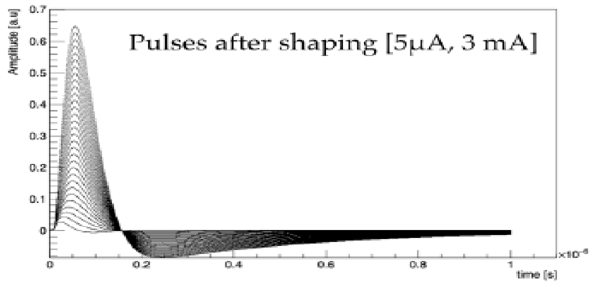


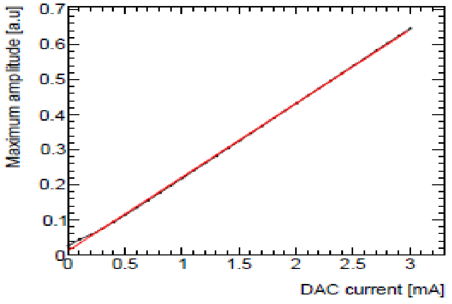
CLAROC layout
- 6,2mm x 2,3mm
- XFAB180nm
- Submitted in June 2019
- Received in Decembrer 2019

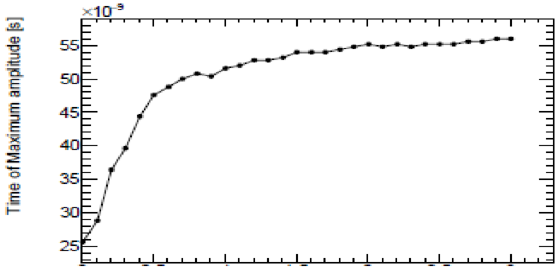


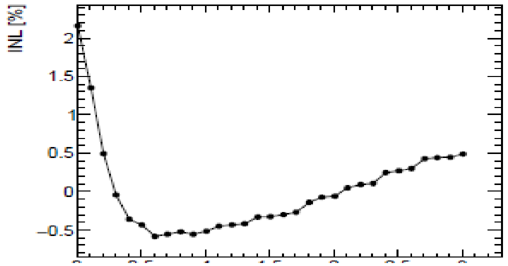
CLAROC 2 Switches measurements

Small current range [0-3mA]





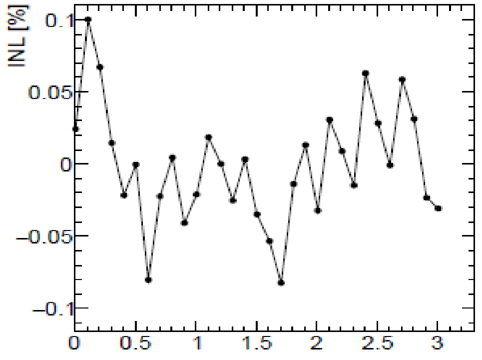


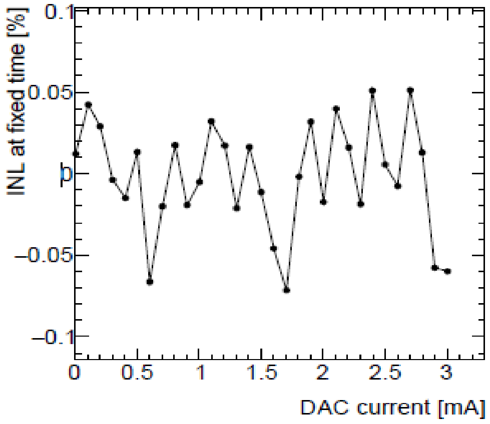


By substraction of the injected charge

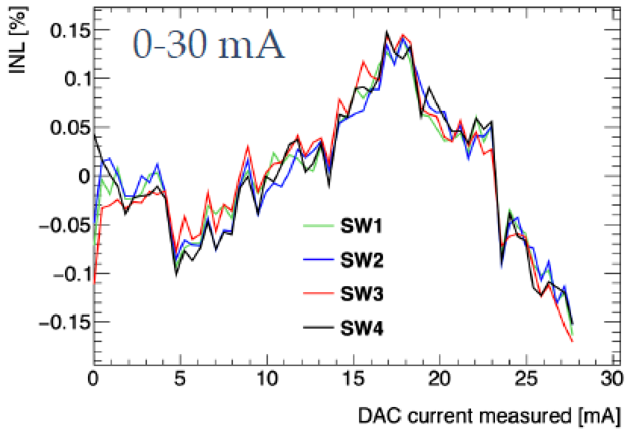
After correction

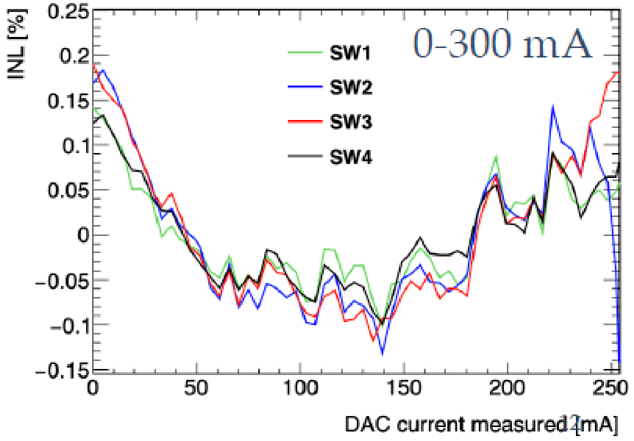
By using the fixed-time method (55ns)





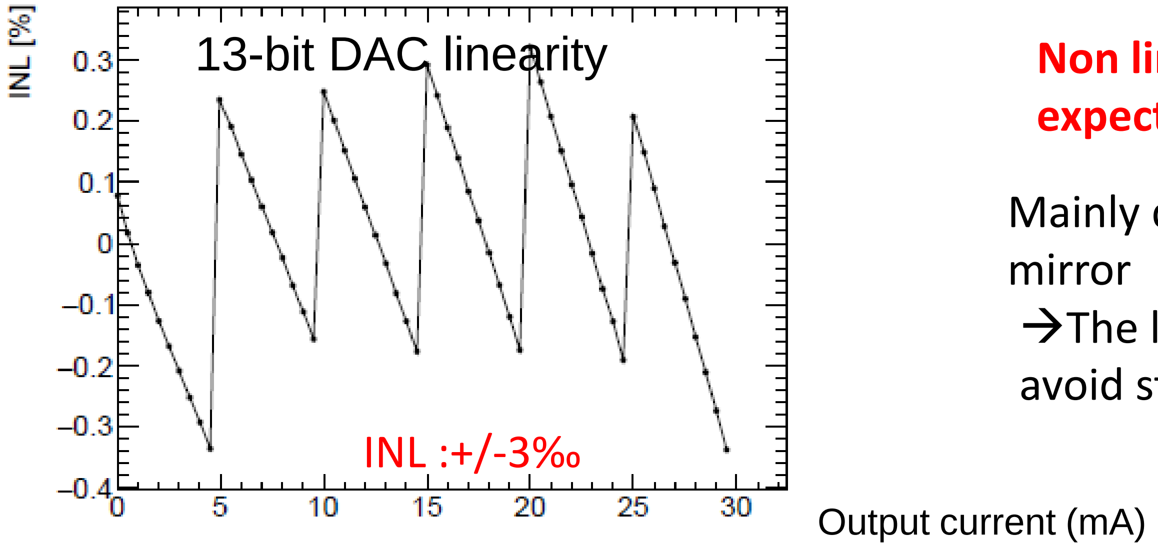
At low current, **injected charge (pulse measured at DAC~0) has non-negligible effect on linearity**





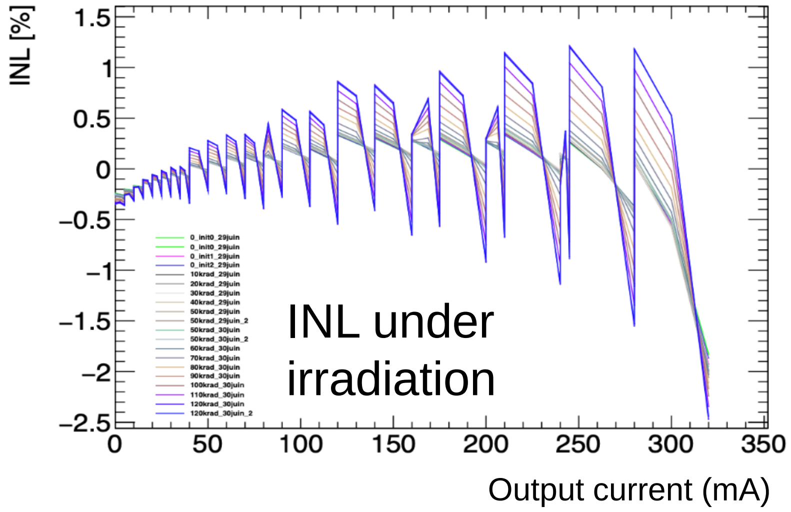
- **HF switches linearity is OK**
- **Injected charge issue under control**

CLAROC 2 measurements



Non linearity on the 13-bit DAC is larger than expected : +/-1‰

Mainly due to steps between each thermometer and each mirror
→The layouts of DACs and mirrors could be improved to avoid steps

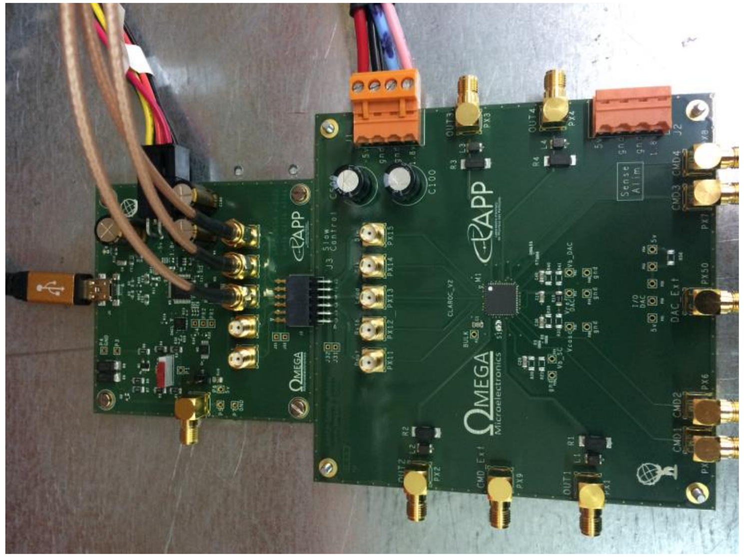


Under irradiation (X-ray and protons)

- the HF switches are still OK.
- DAC is degraded after only 50krad
- the slow control becomes non operational after 20krad

CLAROC2

→ Proposed solution: separate the 2 functions in 2 different chips



Test board CASA1

- The HF switches and mirrors remain in XFAB
  - we need SOI and the 5V and 10V MOS

  ➡ CLAROC3

- The 13-bit DAC is done in a well-known technology : TSMC 130nm

  ➡ LADOC

Developments for calibration upgrade: ASICs evolution in 4 steps

CLAROC and LADOC timeline

2017 STEP 0	2019 STEP 1	**2021 STEP 2**	2022 STEP 3
CLAROC1: **XFAB 180 nm** HF switch; Commercial DAC	CLAROC2: XFAB 180 nm — HF switch, 13-bit DAC	**CLAROC3**: **XFAB 180 nm** HF switch; **LADOC1**: **TSMC 130 nm** **13-bit** DAC	CLAROC4: **XFAB 180 nm** HF switch; LADOC2: **TSMC 130 nm** **16-bit** DAC
Test Vehicule: to evaluate the XFAB technology	**1st complete prototype** with HF switches and DAC **Both XFAB 180 nm**	2[nd] **prototype** with **HF switches and DAC** functions **in 2 different chips** and **in different technology** HF switches in XFAB 180 nm 13-bit DAC in TSMC 130 nm	3[rd] **prototype** with two separated chips, still with different techno. HF switches in XFAB 180 nm **16-bit DAC** in TSMC 130 nm

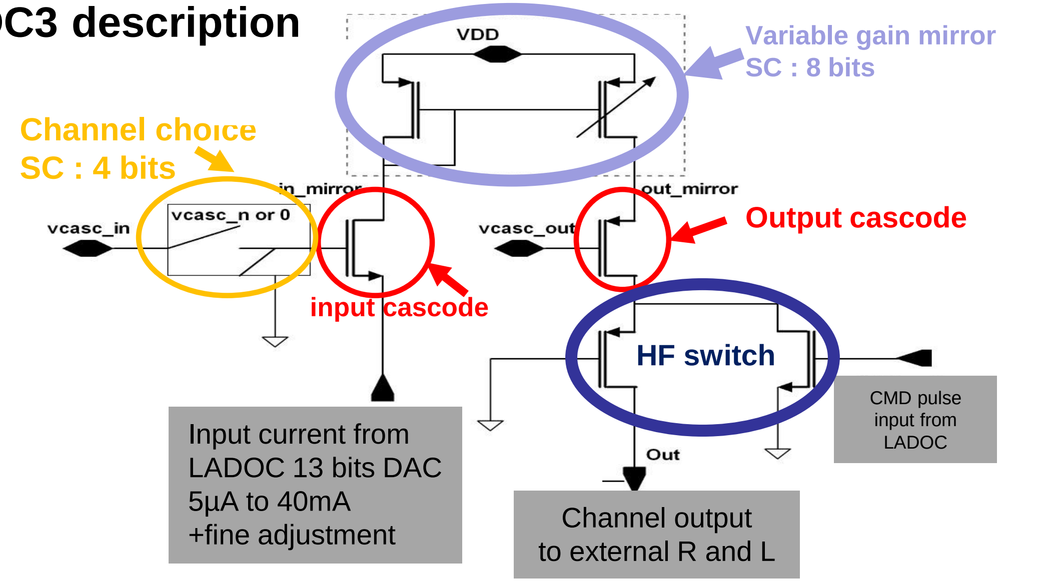
CLAROC3 and LADOC1

- **CLAROC3 in XFAB 180nm**
  - **4 identical channels** with HF switch and 3-bit DAC (mirror gain 1 to 8)
  - All slow control (12 bits) and fast signals are provided externally and need level translators (1.2V to 5V)

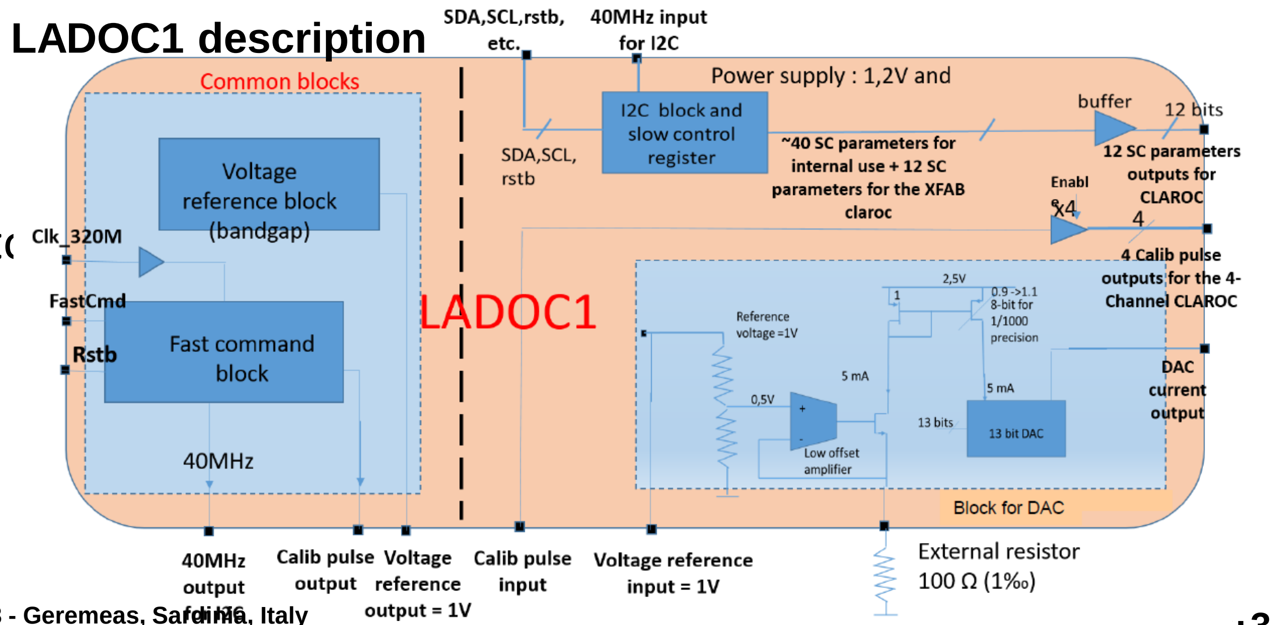
- **LADOC (Link And DAC Of Claroc) in TSMC 130nm**
  - **13-bit current DAC** from 5uA to 40mA with

  8-bit to adjust the current reference.
  - **Reference voltage** (CERN Bandgap)
  - **A fast command module** (re-used from HGCROC) to provide the command pulses,
  - **I2C Slow control** for both chips (LADOC itself and CLAROC) (re-used from HGCROC)

CLAROC3 description



LADOC1 description

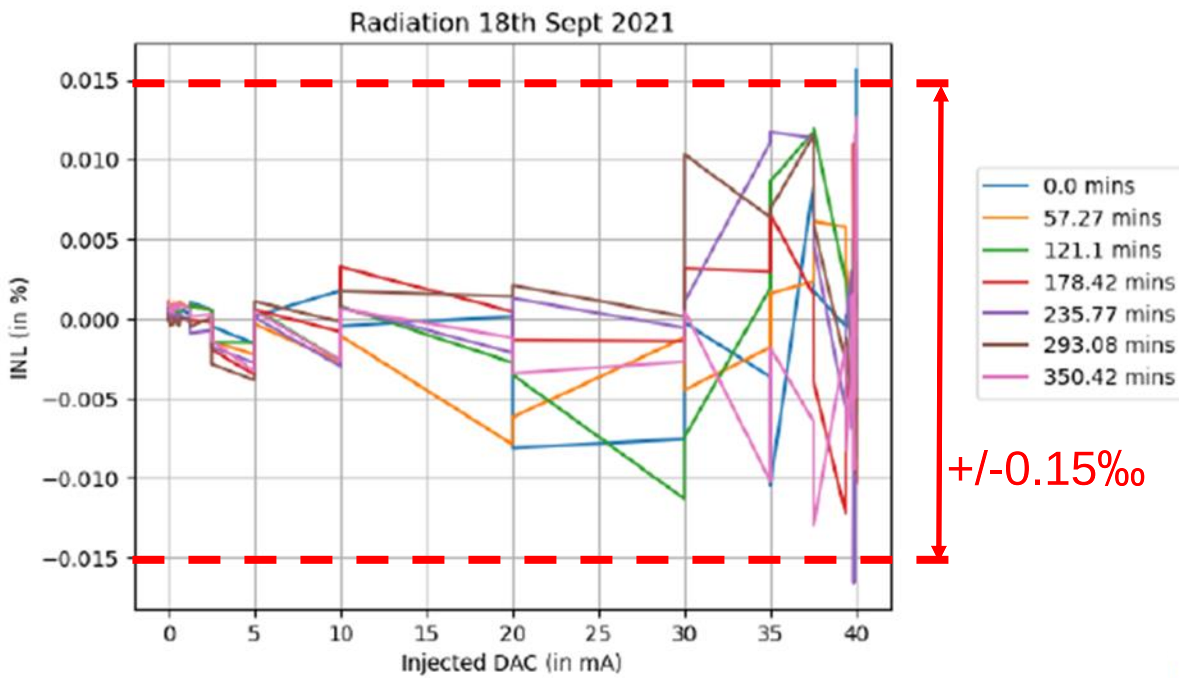


LADOC1 13-bits DAC measurement

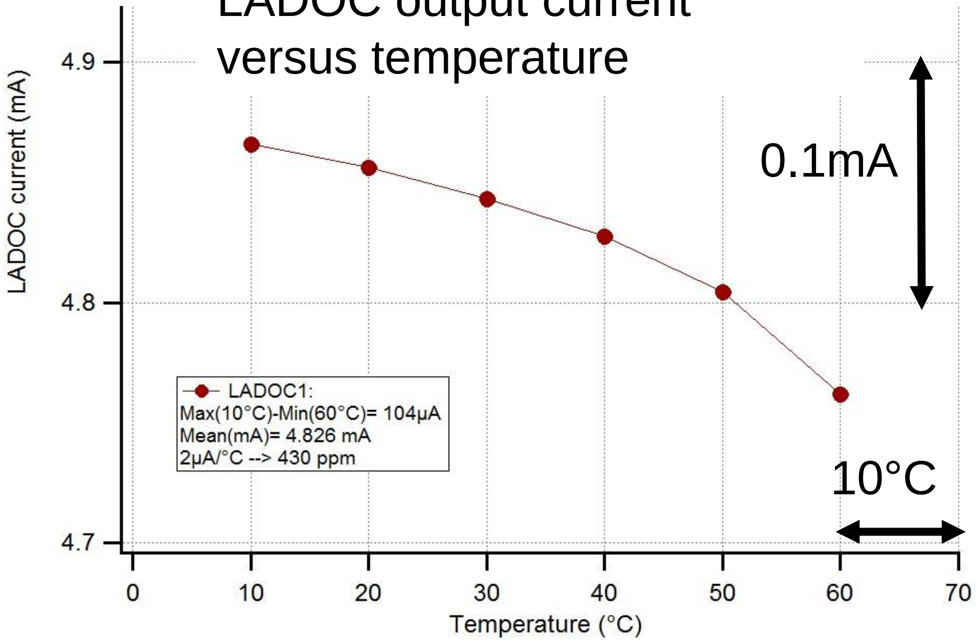
Linearity DAC measurements :

- INL on dynamic range < 0.3‰
- INL very stable under irradiation up to 20 times the requirements

LADOC1 INL measurements

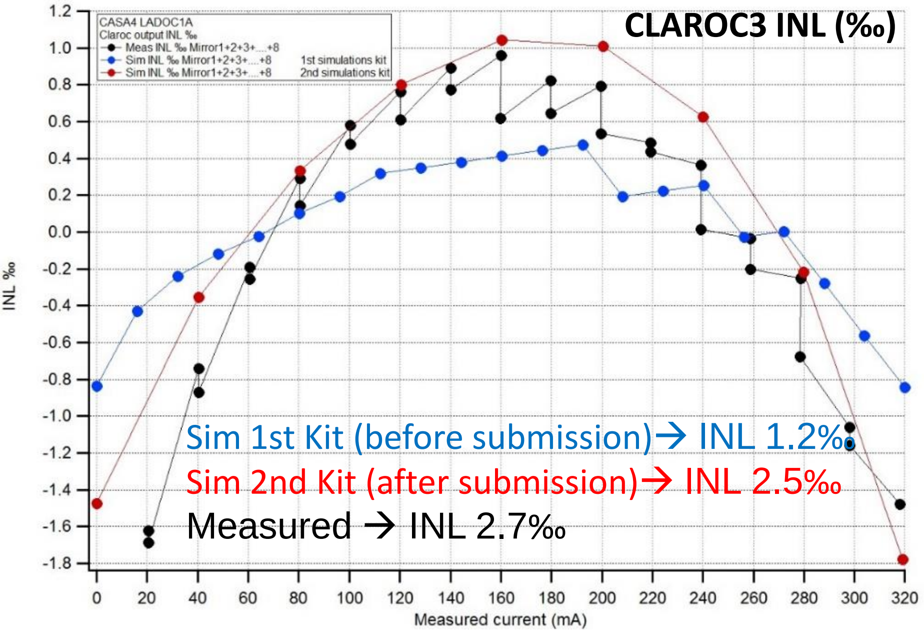


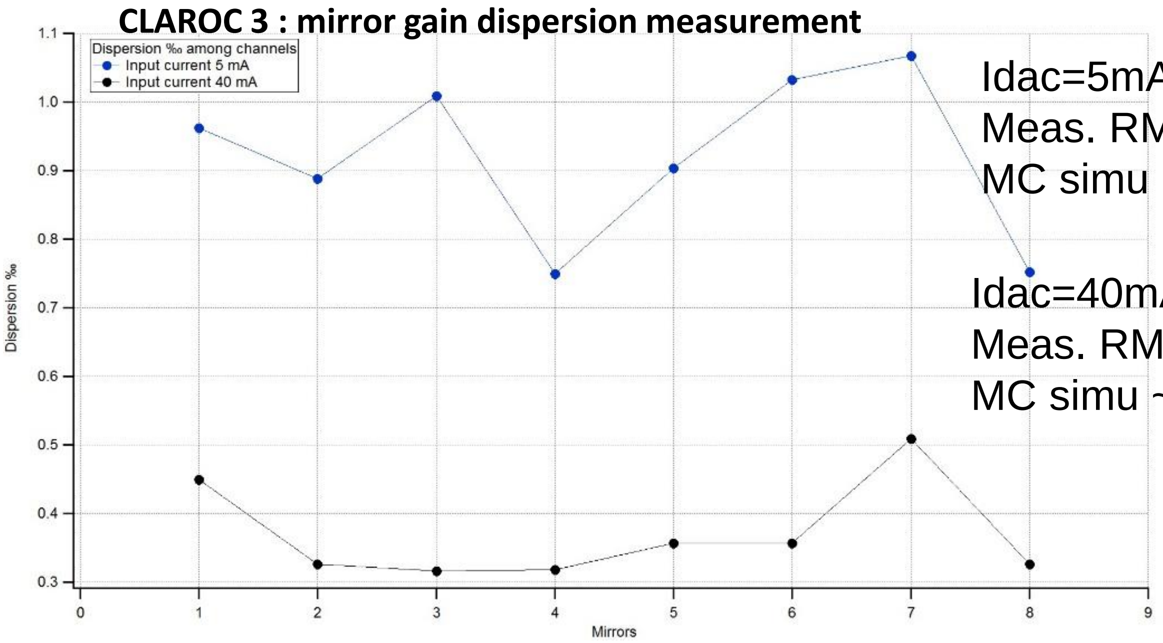
LADOC output current versus temperature



LADOC sensitivity to temperature :
2µA/°C – 430ppm/°C

CLAROC3 measurements





Idac=5mA
Meas. RMS ~ 1 ‰
MC simu ~ 0.1 ‰

Idac=40mA
Meas. RMS ~ 0.4 ‰
MC simu ~ 0.07 ‰

- **Non linearity is larger than expected : +/-1‰**

Due to early effect : Simulation difficulties
(evolving models, simulation reliability, etc.)

- Not negligible mirror gain dispersion

Difficult to be controlled

→ use of a constant gain (8) mirror and transfer of the 3 bits (MSB) of CLAROC to LADOC (LSB)

→ To improve linearity and compensate the Vt shift of the irradiated transistors we must add an amplifier to improve the mirror gain.

Developments for calibration upgrade: ASICs evolution in 4 steps

CLAROC and LADOC timeline

2017
STEP 0

CLAROC1

XFAB 180 nm
HF switch

Commercial DAC

Test Vehicule:
to evaluate the XFAB technology

2019
STEP 1

CLAROC2

XFAB 180 nm

HF switch

13-bit DAC

1st complete prototype with HF switches and DAC
Both XFAB 180 nm

2021
STEP 2

CLAROC3

XFAB 180 nm
HF switch

LADOC1

TSMC 130 nm
13-bit DAC

2[nd] **prototype** with **HF switches and DAC** functions **in 2 different chips** and **in different technology**
HF switches in XFAB 180 nm
13-bit DAC in TSMC 130 nm

2022
STEP 3

CLAROC4

XFAB 180 nm
HF switch

LADOC2

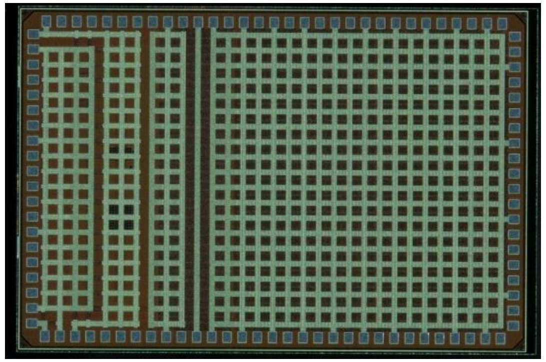
TSMC 130 nm
16-bit DAC

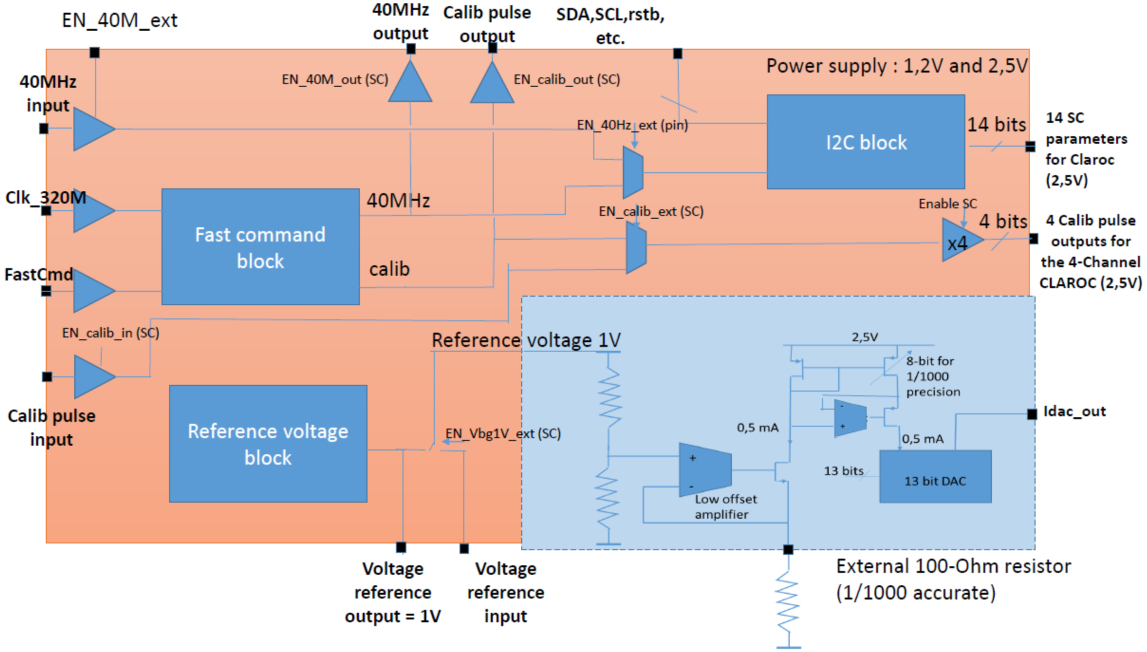
3[rd] **prototype** with two separated chips, still with different techno.
HF switches in XFAB 180 nm
16-bit DAC in TSMC 130 nm

LADOC2

- **DAC extended from 13 to 16 bits : 3 bits LSB have been added. Current from 625nA to 40mA**
- **The current source improved : to ensure a better temperature stability**
- **Provides to CLAROC 2.5V slow control signals (instead of 1.2V in LADOC1)**
- **Provides to CLAROC 2.5V fast signals (instead of 1.2V in LADOC1)**

LADOC 2 layout
- 3,4mm x 2,3mm
- TSMC130nm
- Submitted in April 2022
- Received in July 2022
- Package : BGA 196

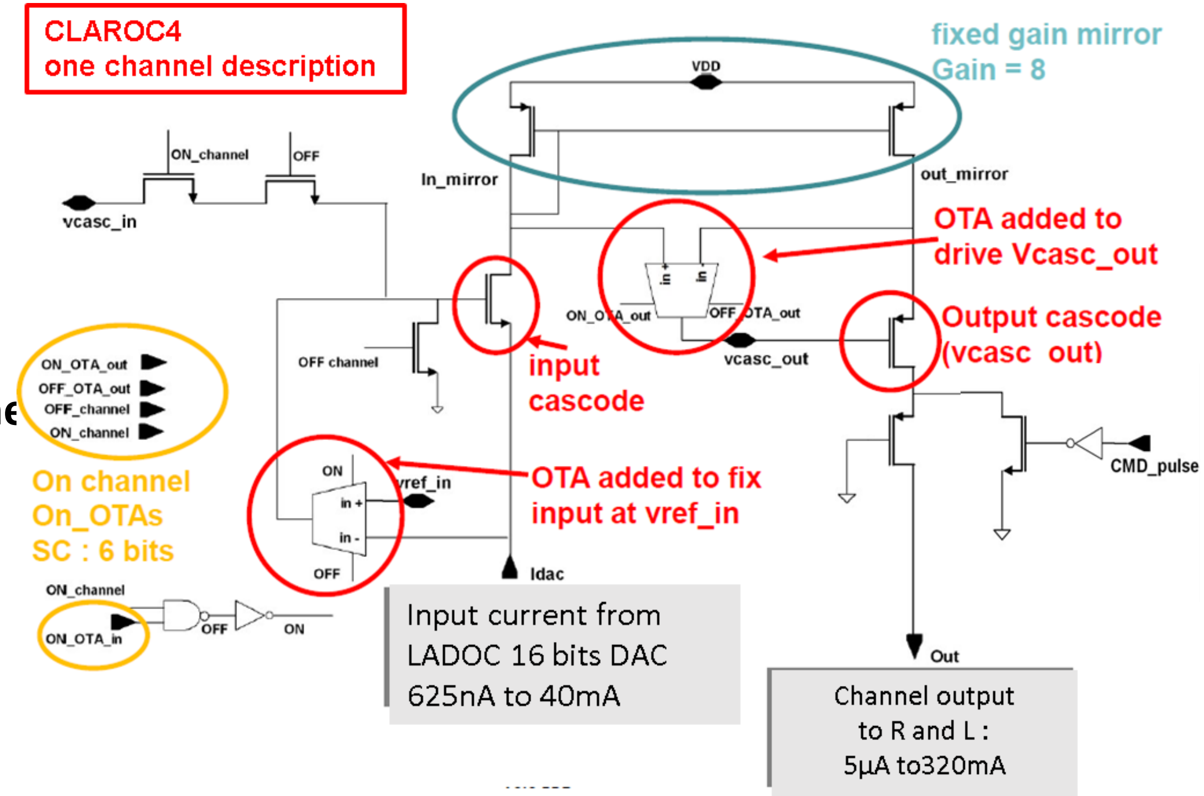


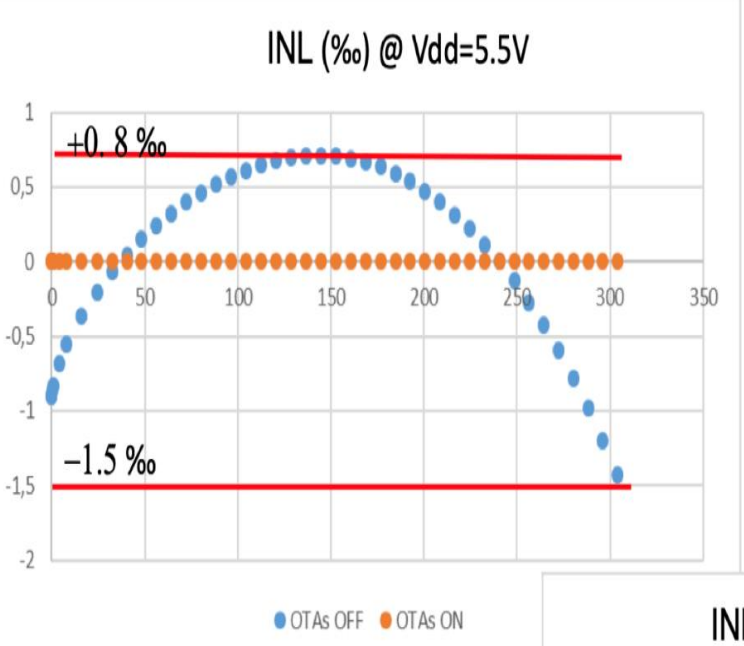


Notice: It is not a true 16-bit DAC, but it is a 16-bit DAC range with 10-bit accuracy

CLAROC4

- **The mirror gain becomes constant (= 8)**
- **An OTA is added to improve the mirror gain**
  - **Completely eliminates Early effect**
- **A second OTA is added at the input in order to control the input voltage (at 2.5V) and to keep a good linearity for LADOC**



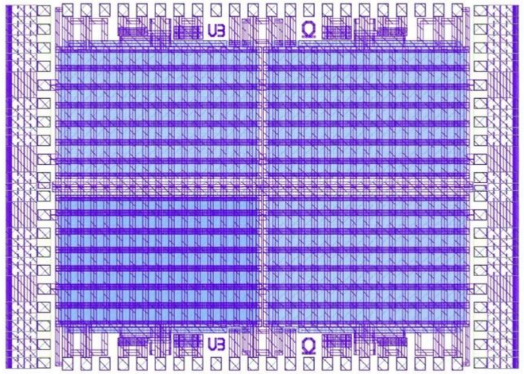


INL without OTAs (OFF) = 2,3 ‰ (CLAROC3)

INL with OTAs =0.001 ‰

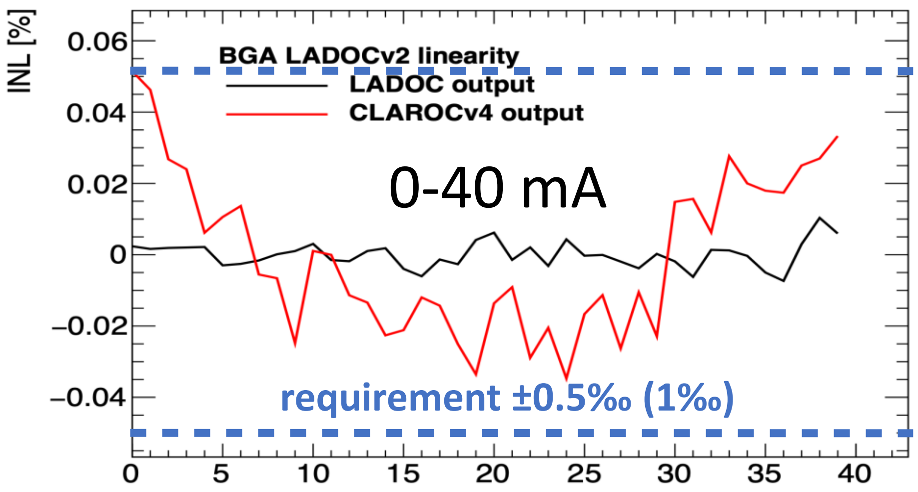
CLAROC4 : non linearity simulation

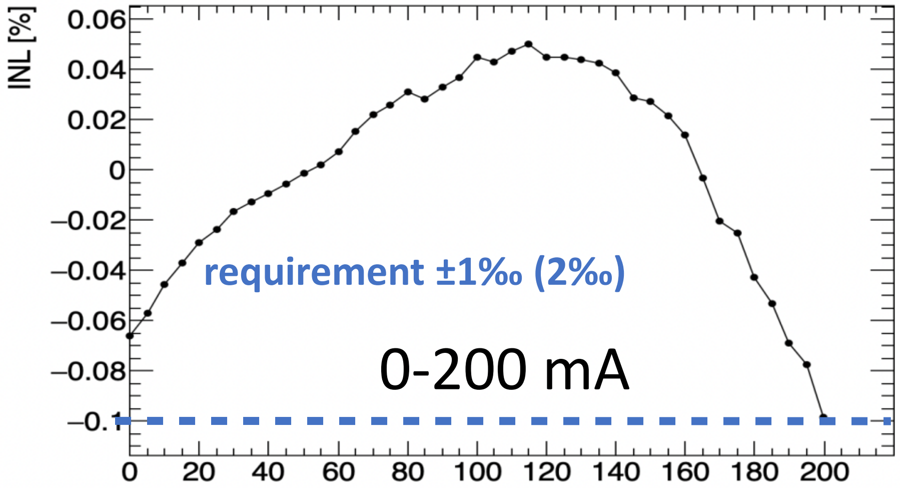
INL (‰) OTA on@ Vdd=5.5V



CLAROC4 layout
- 2,4mm x 2,3mm
- XFAB180nm
- Submitted in March 2022
- Received in September 2022
- Package : BGA 196

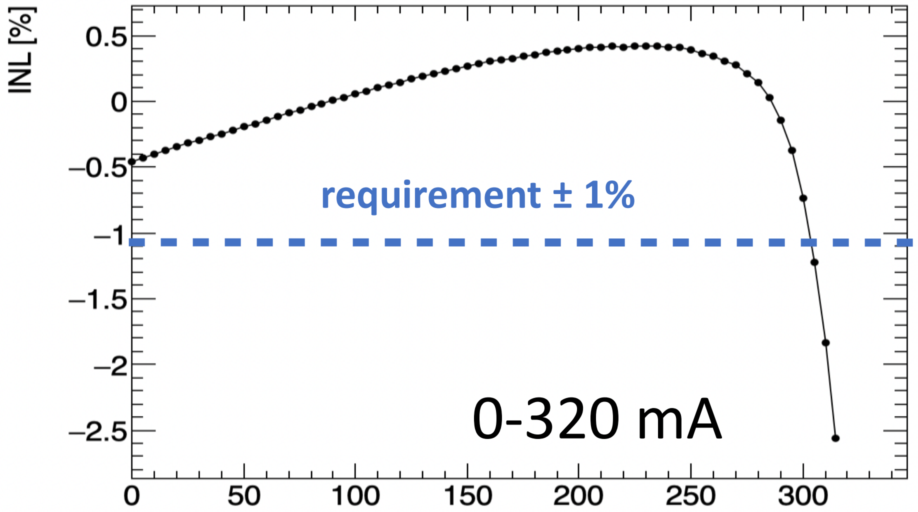
Linearity for the different ranges





The INL is within specifications for small and medium ranges : output current < 200 mA

Ladoc2+Claroc4

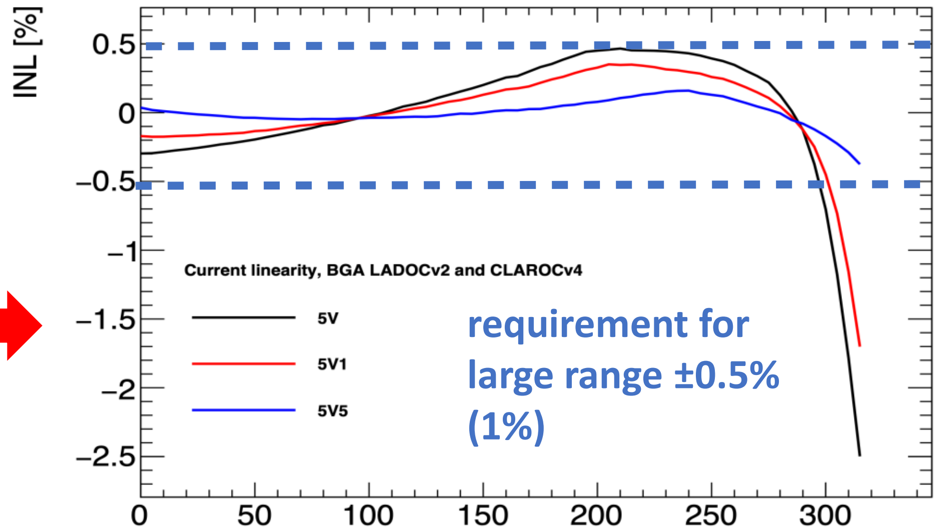


Not within specification for current > 200 mA

→ Saturation

Increasing Vdd to 5.5V

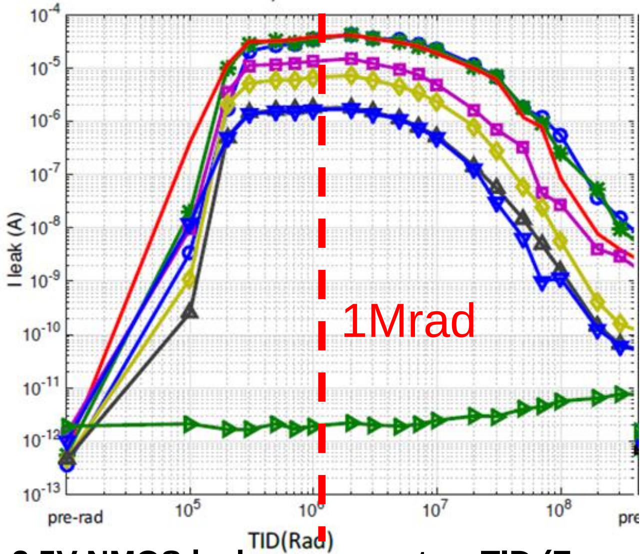
→ Within specs



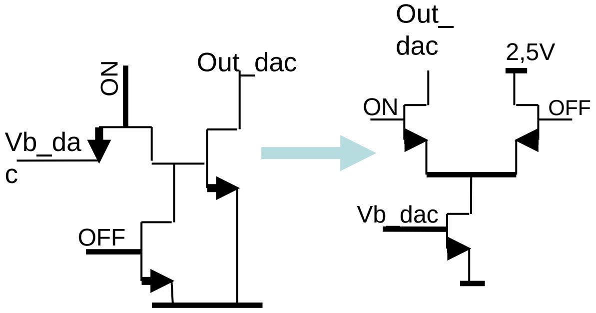
CLAROC4 and LADOC2 irradiation tests

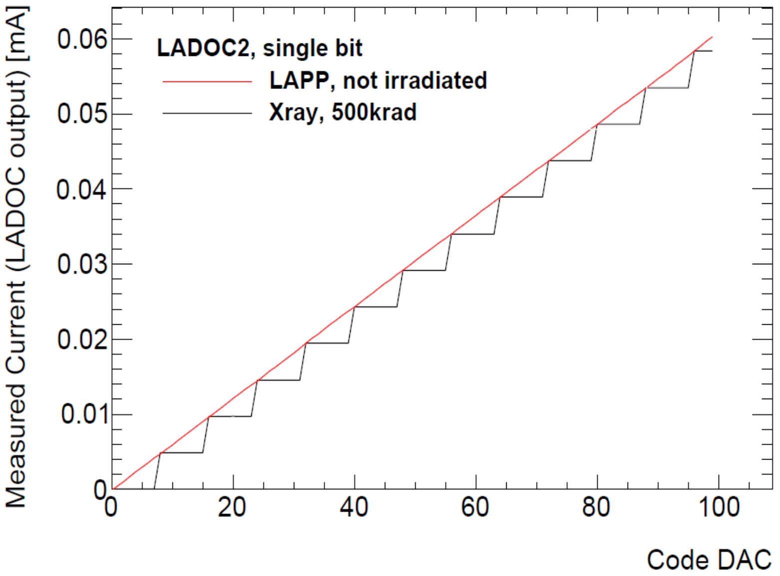
2 X-ray campaigns at CERN were performed :

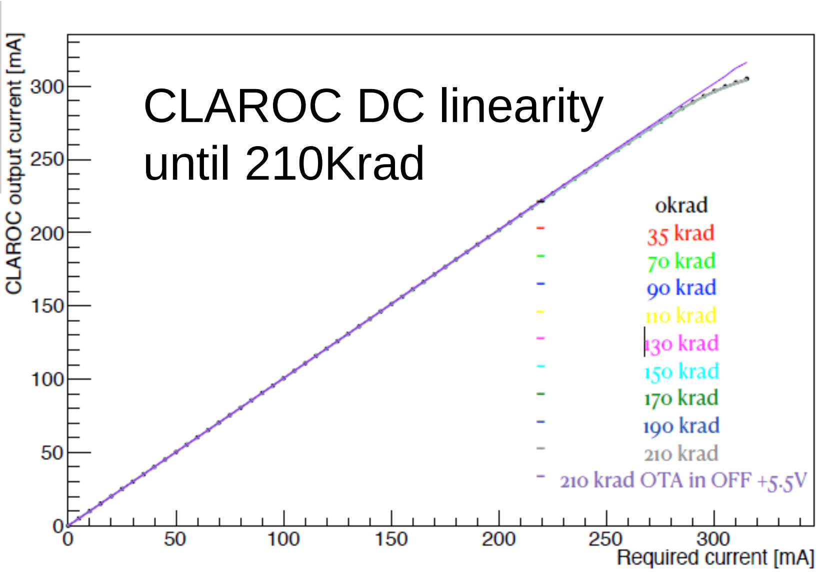
• **LADOC2 :** 3-bit sub-DAC (0-> 5µA) dies after only **60 krad** due to current leakage in 2.5V NMOS.



2.5V NMOS leakage current vs TID (From Michelis @CERN)







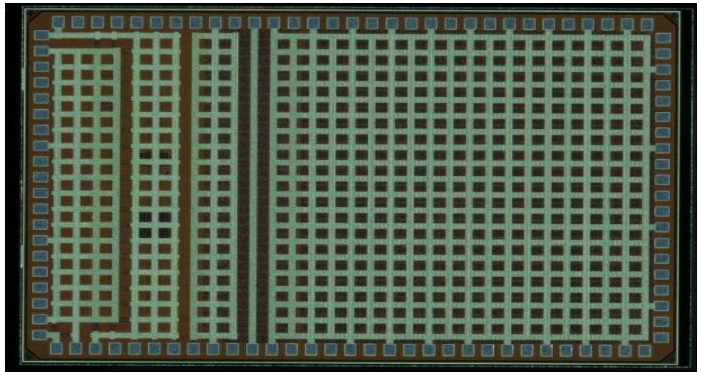
•**CLAROC4 :**

- PMOS transistor of the HF switch has only a very tiny VT shift after 200 krad (40 mV)
- NMOS command for the HF switch presents leakage current at low doses (20Krad) when it is ON which is not the normal use. When it is OFF, no effect of irradiation

Summary

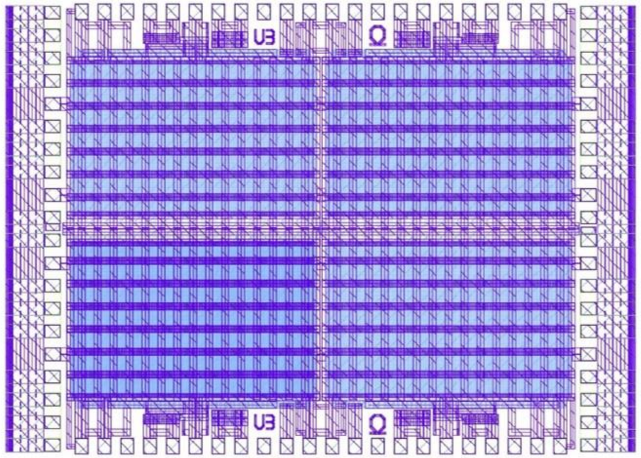
LADOC2 :

- Fullfills the requirements,
- Unexpected irradiation problems encountered at very low dose has to be corrected



CLAROC4 :

- Now fullfills the specifications
- Difficulties encountered using non-mainstream technology (changing models, simulation reliability, …)



Now efforts move to test the chips on the calibration board

For the calibration system, we need ~6000 dies of each :

→ Pre-production end 2023

→ Series production mid 2025

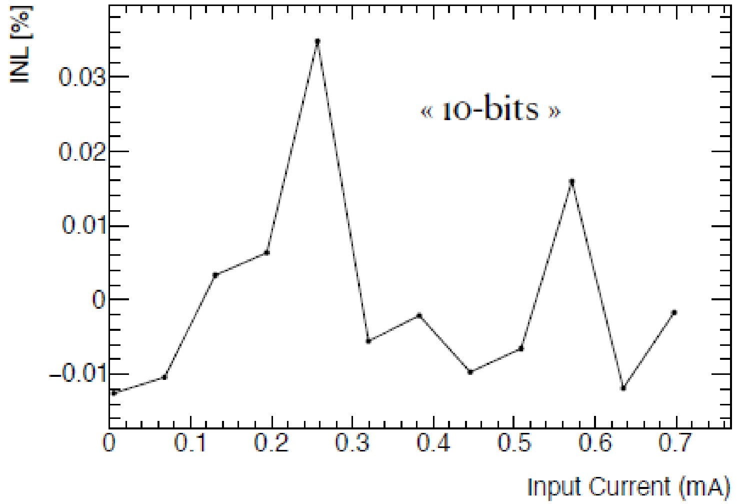
Thank you

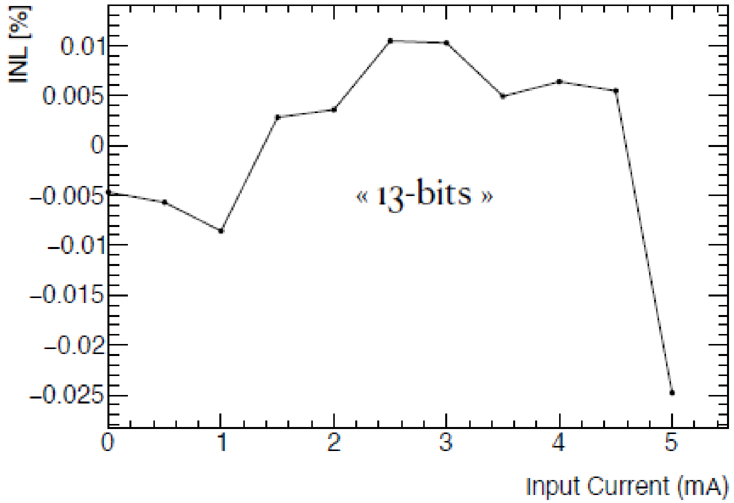
Backup slides

Quantities

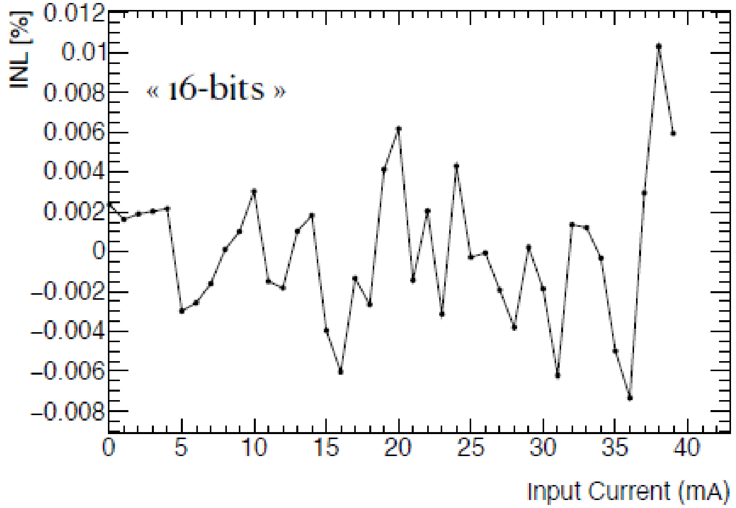
- Need to calibrate ~200000 calorimeter cells
  - About 1 calibration line for 8 cells (depending on the position in the detector)
- 130 boards to be produced (including spares)
  - 122 (+8) calibration boards with 128 channels each
  - Inserted in LAr front-end crates (about 1 CABANE for 15 FEB2s)
  - A total of 145 boards to be fabricated, accounting for pre-production (80%) and production (90%) yields
- ASICs:
  - 4640 ASICs of each type need to be produced (145 x 32)
  - 5568 ASICS of each type need to be fabricated, accounting for pre-production and production yields (80%) -> 11136 ASICs in total

LADOC 2 linearity performance measurement



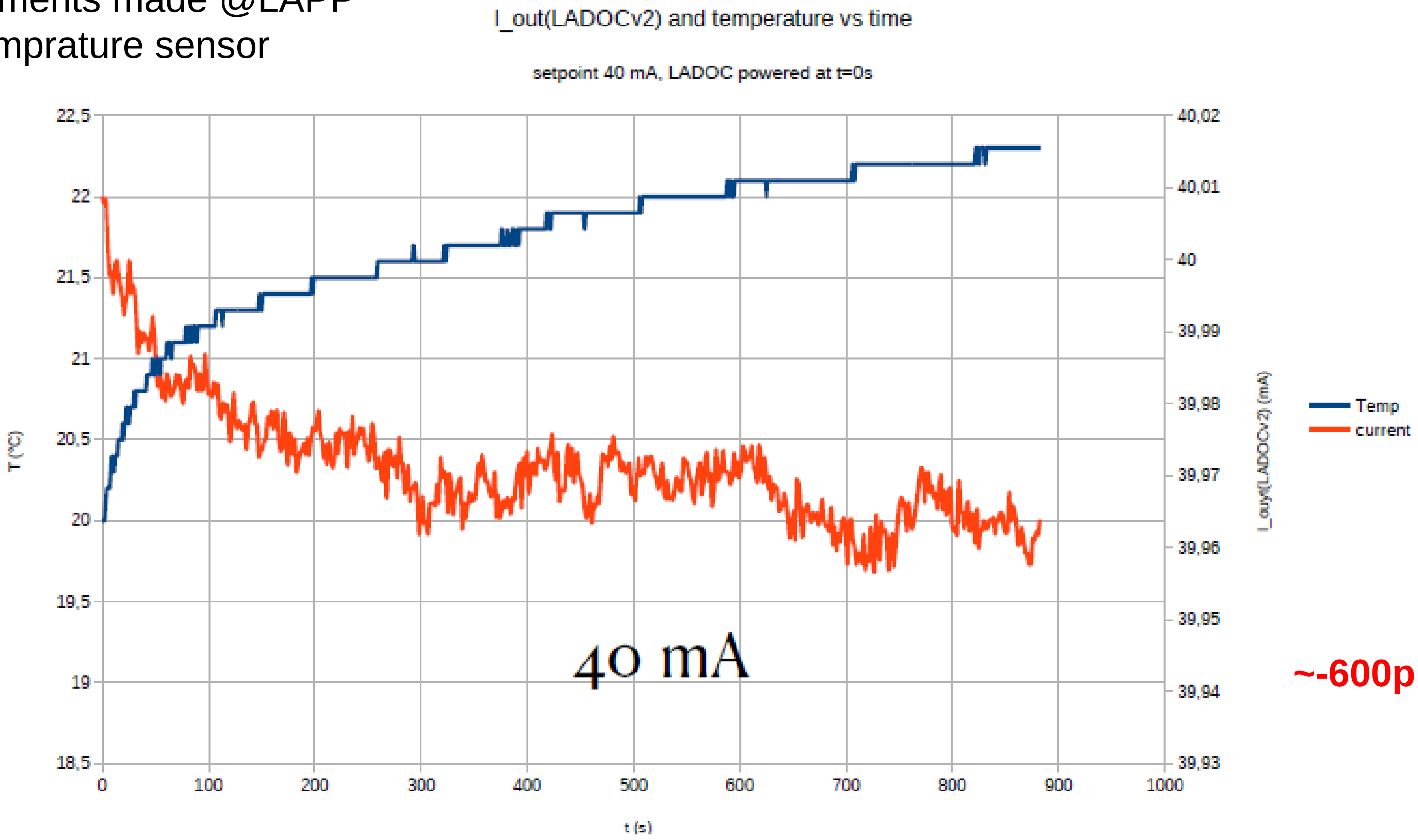


Largely within the 0,1% requirement (~10 times better)



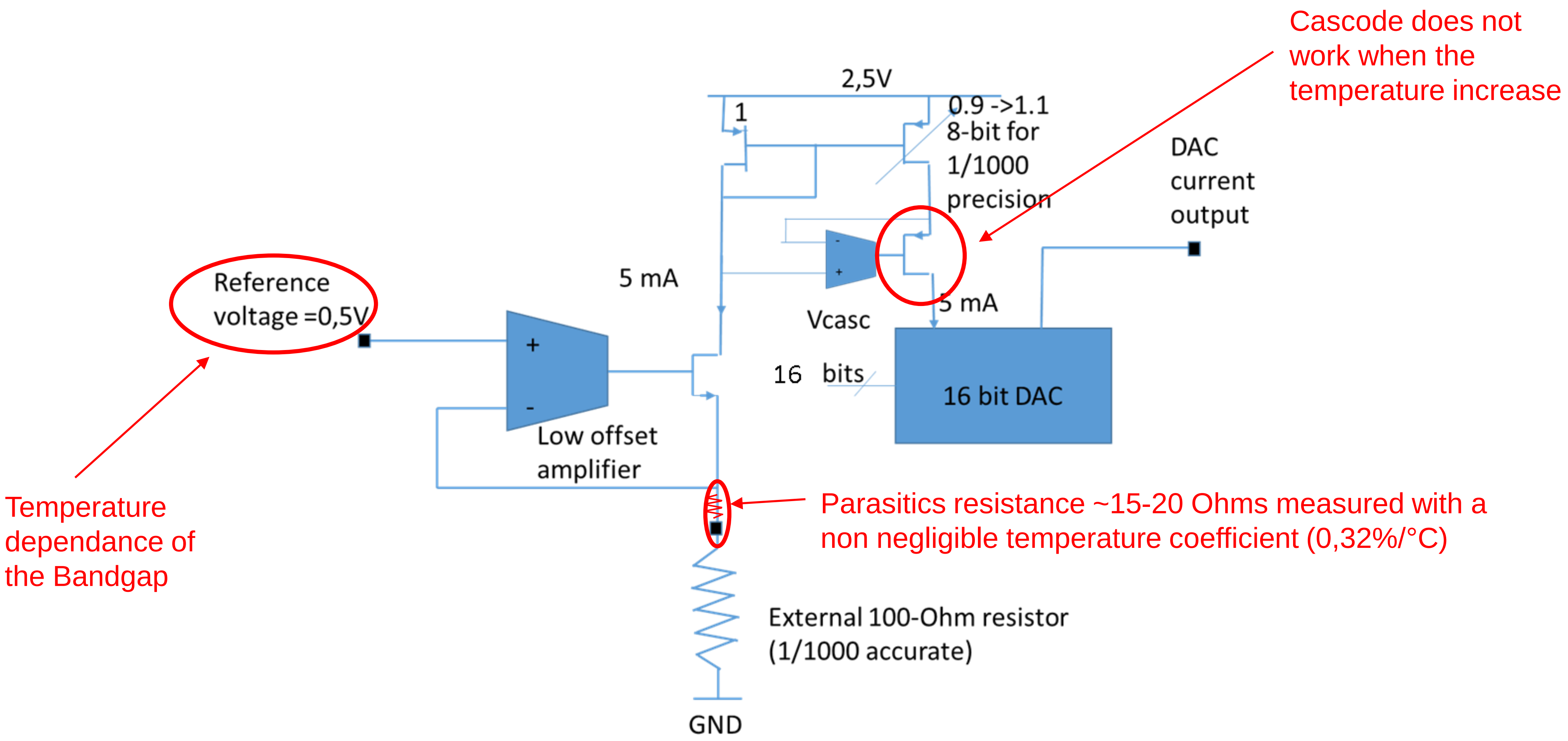
Temperature effect

Measurements made @LAPP
with a temprature sensor



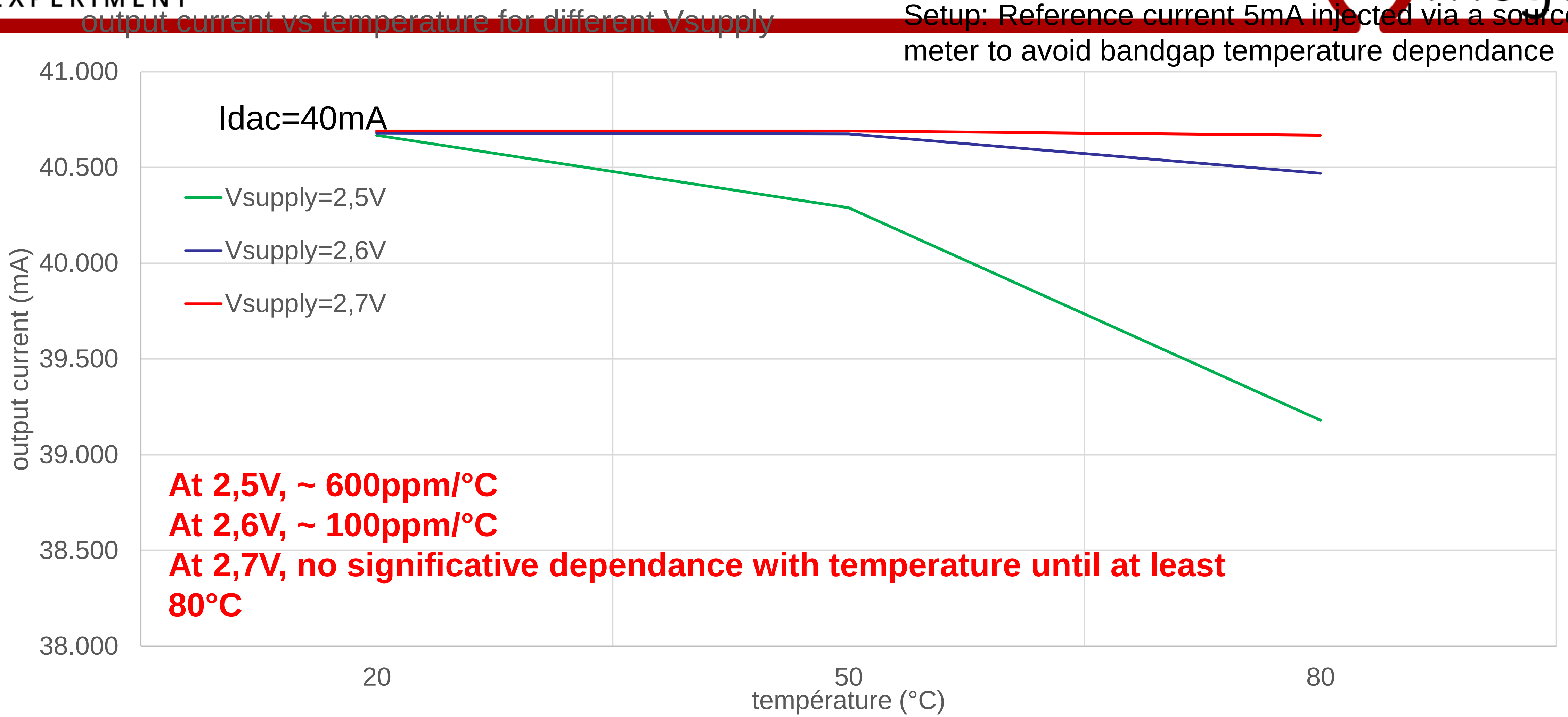
~-600ppm/°C

Temperature dependance Sources



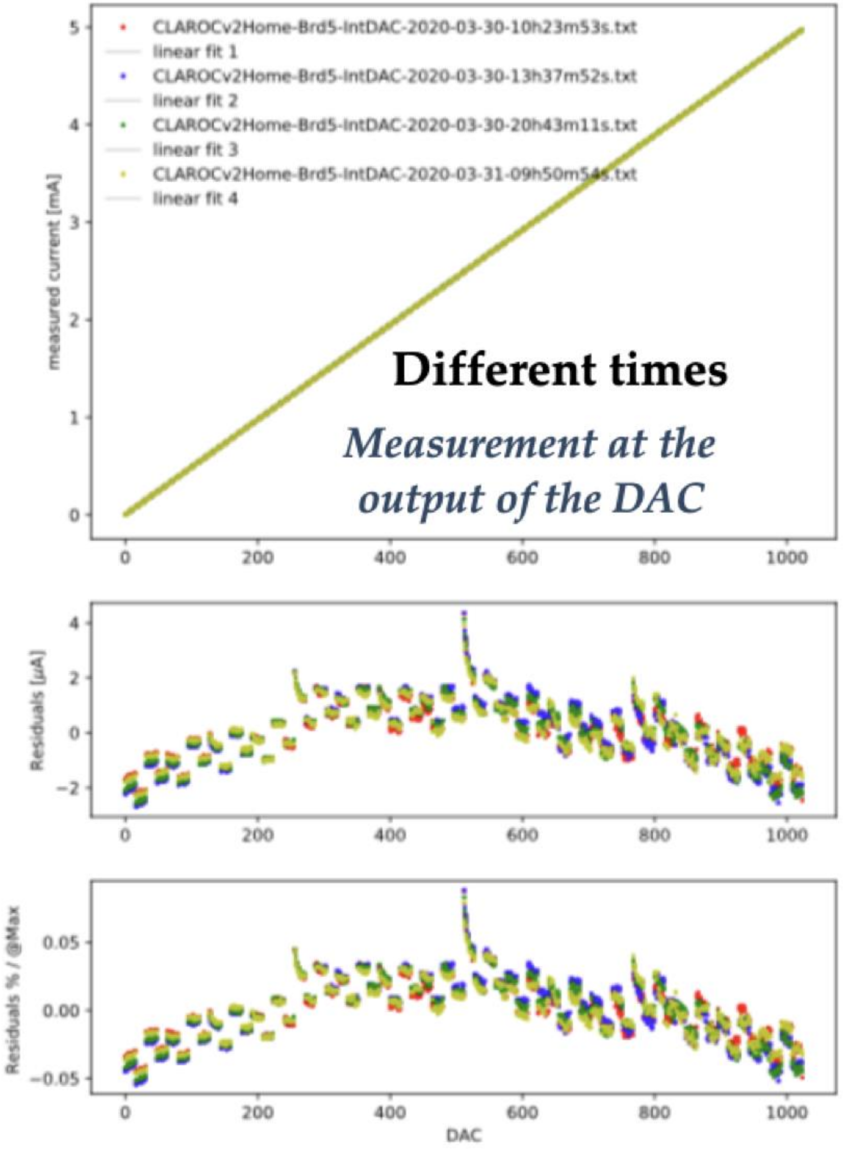
Temperature dependance : cascode

Setup: Reference current 5mA injected via a source-meter to avoid bandgap temperature dependance

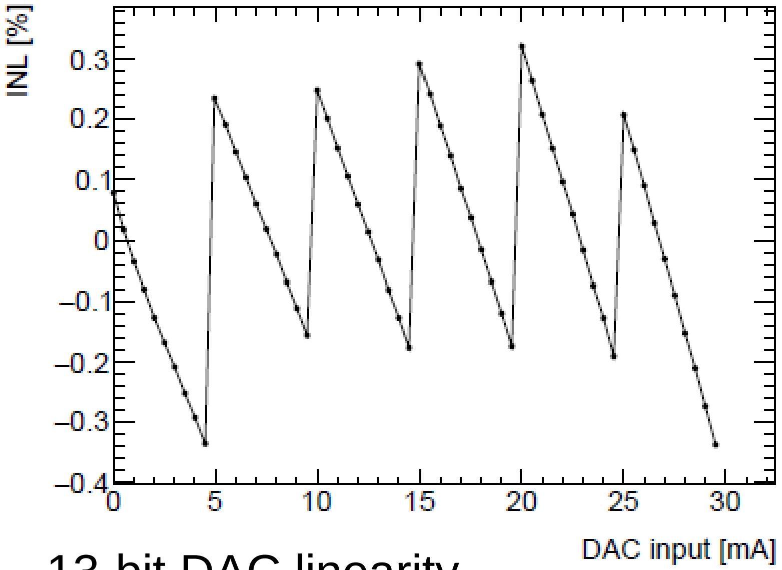


At 2,5V, ~ 600ppm/°C
At 2,6V, ~ 100ppm/°C
At 2,7V, no significative dependance with temperature until at least 80°C

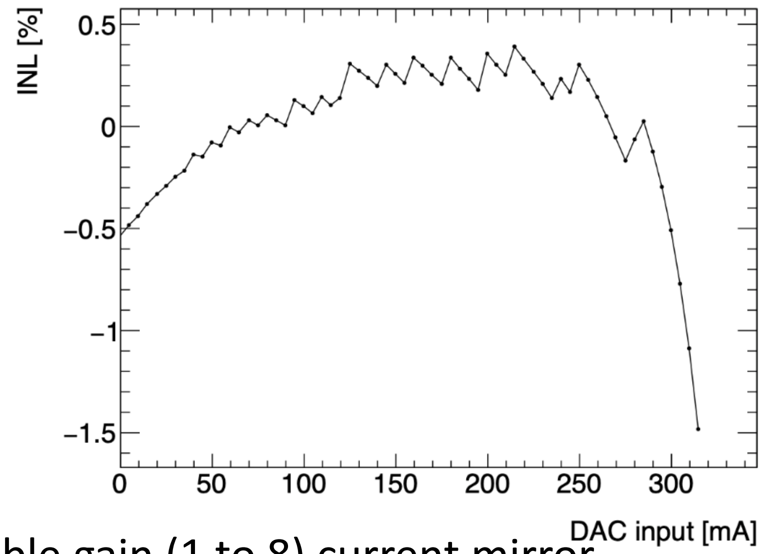
CLAROC 2 DAC measurements



10-bit DAC linearity



13-bit DAC linearity

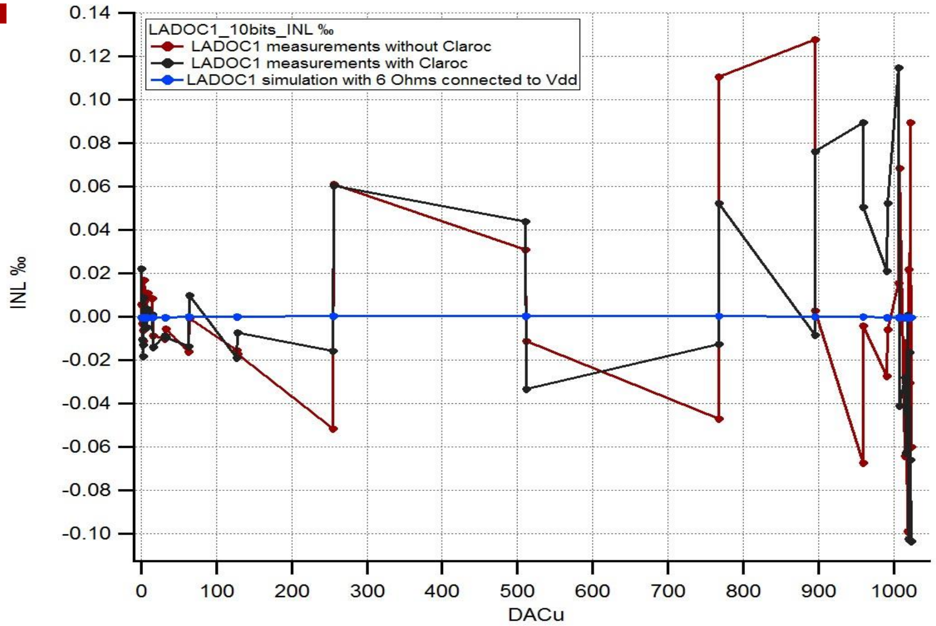


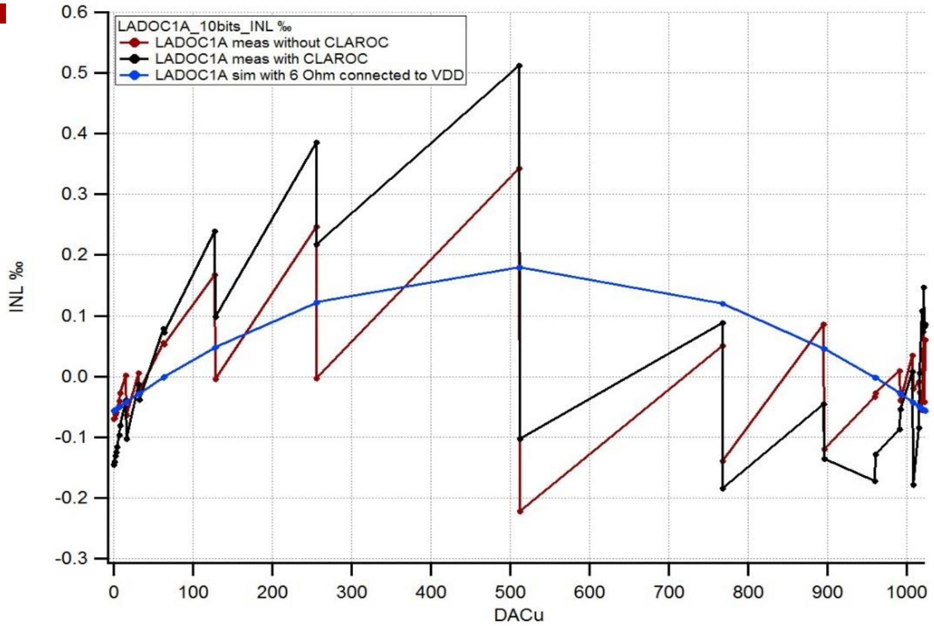
3-bit tuneable gain (1 to 8) current mirror

LADOC : DAC linearity simulations and measurements

LADOC1

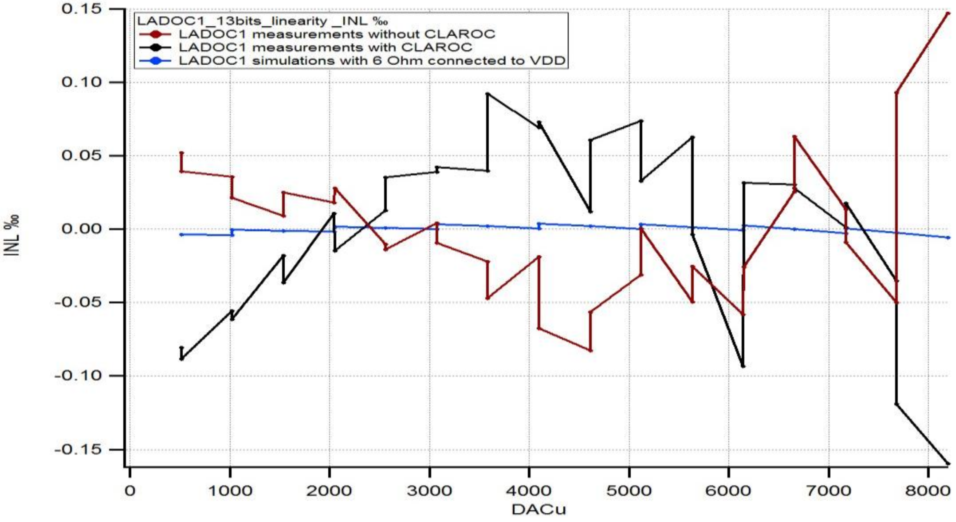
LADOC1a

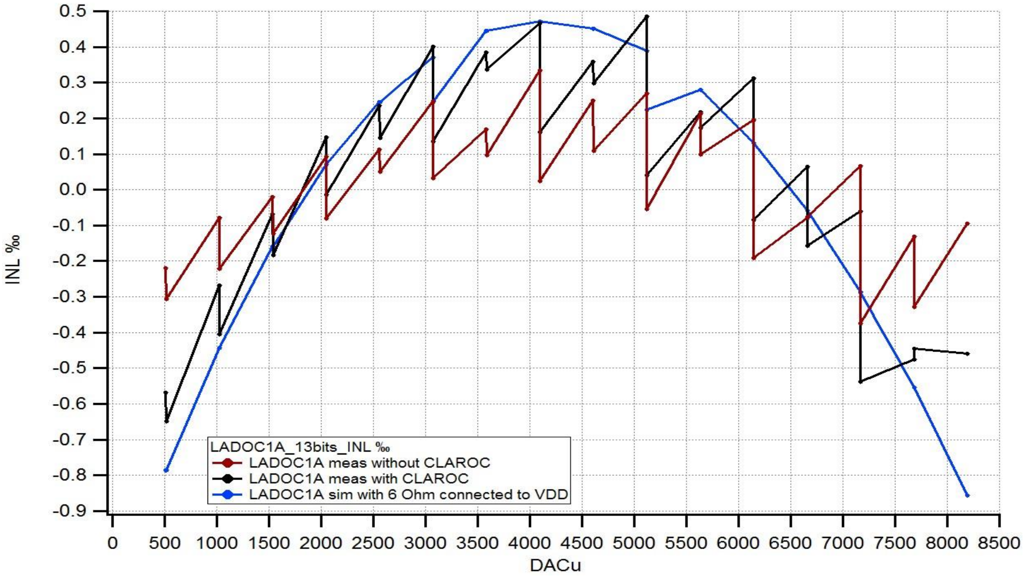




10-bit DAC

- LADOC Simulations (blue)
- LADOC output measurements without Claroc connected (red)
- LADOC output measurements with Claroc connected (black)



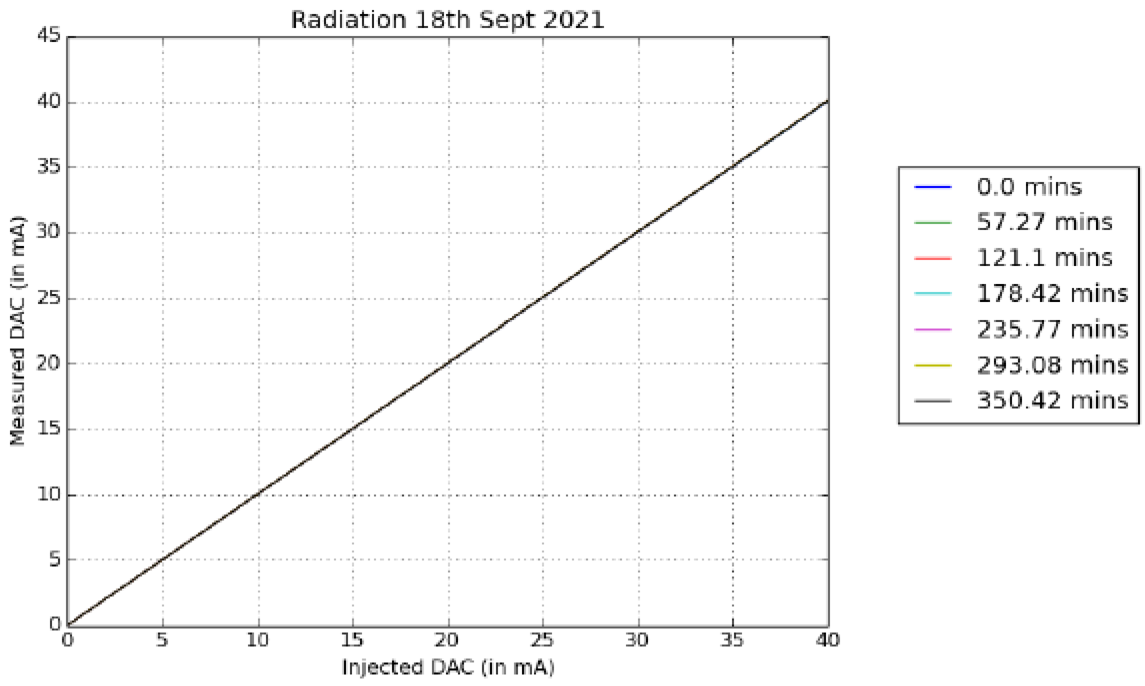


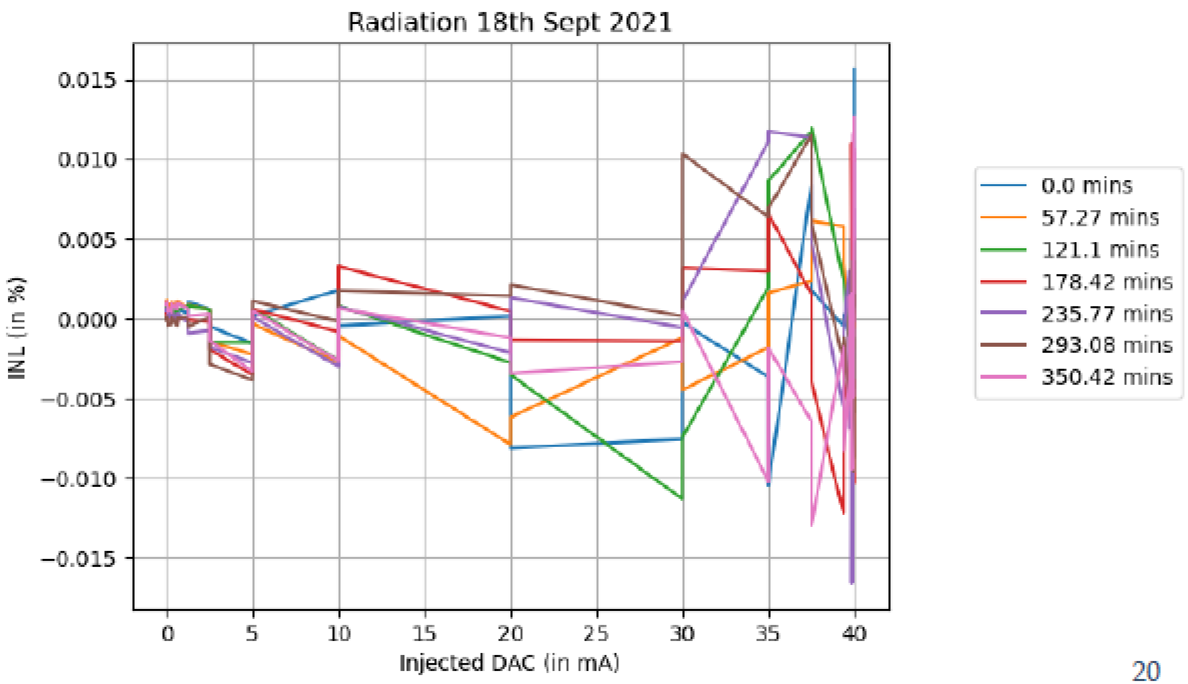
13-bit DAC

- LADOC Simulations (blue)
- LADOC output measurements without Claroc connected (red)
- LADOC output measurements with Claroc connected (black)

LADOC linearity after irradiation

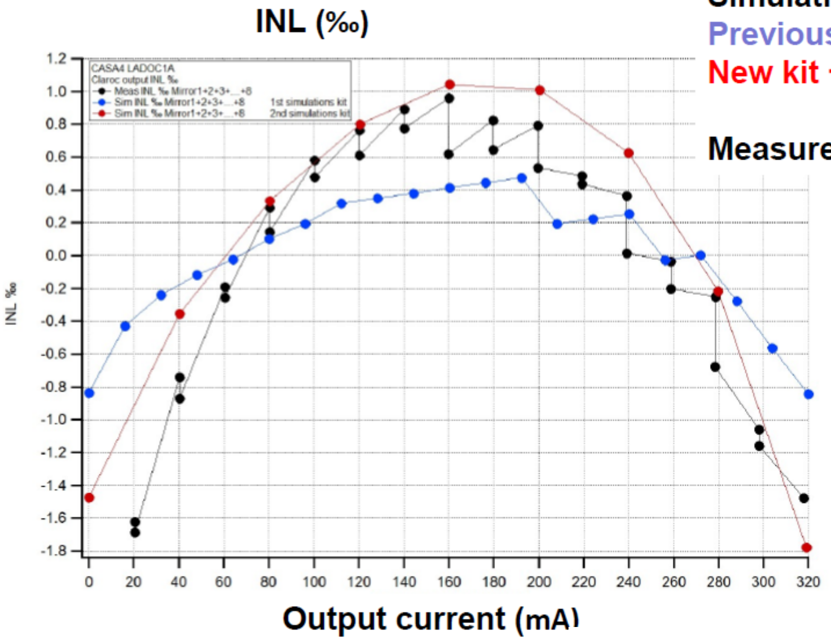
- Measured every 2-3 minutes during the two nights.
- Show here one curve per hour i.e each curve adds up ~350 krad and 6.5e12 p/cm2 (total ~5 Mrad)
  - no any degradation seen over time, and after the two nights
  - **INL <0.05% after full irradiation**





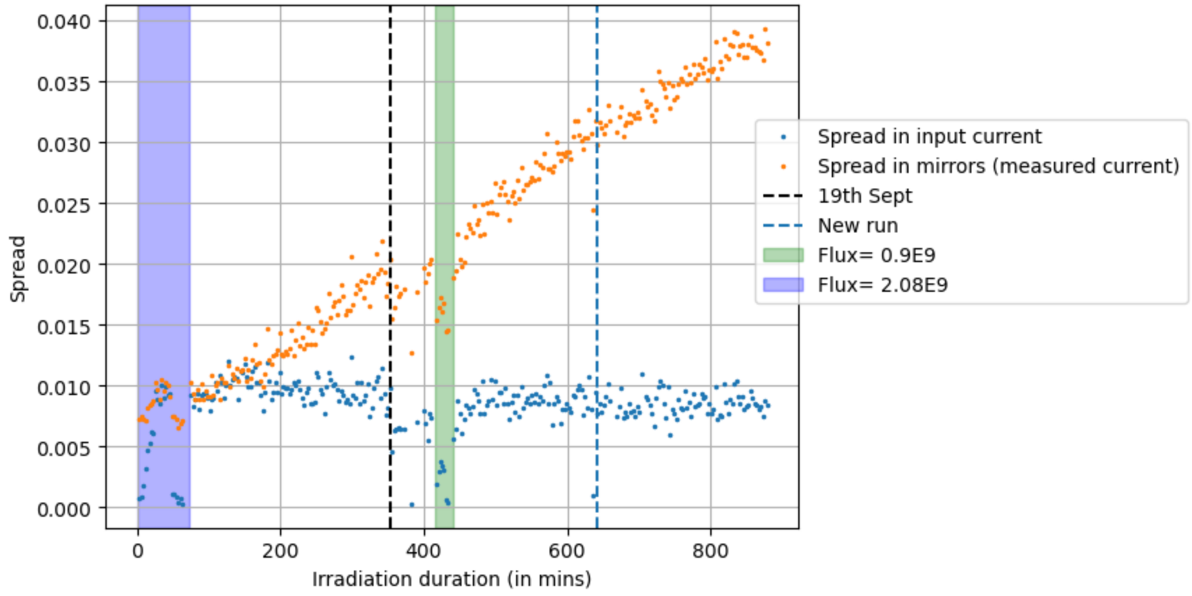
20

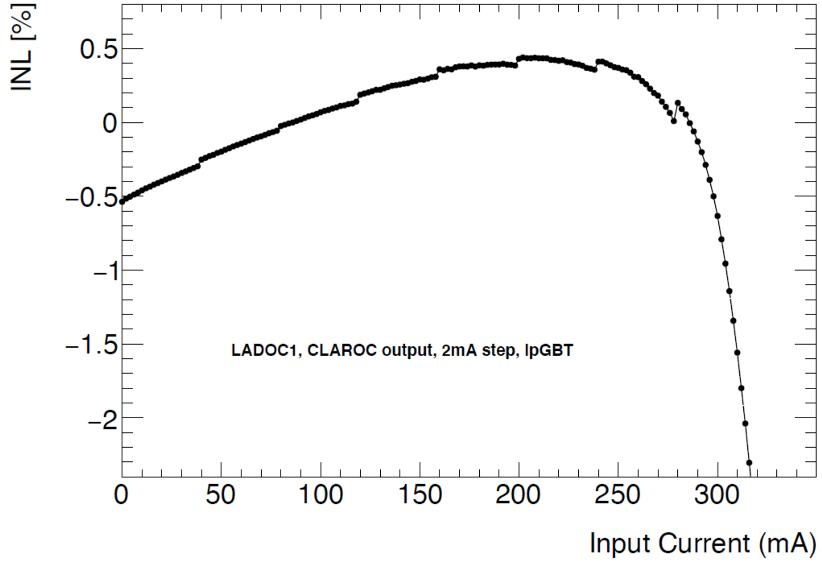
ATLAS CLAROC3 measurement



Simulations :
Previous kit → INL 1.2 ‰
New kit → INL 2.5 ‰

Measure → INL 2.7 ‰





Developments for calibration upgrade : ASICs evolution in 4 steps

CASA = **C**alibration **AS**ICs for **A**TLAS

2017
STEP 0

CLAROCv1
XFAB 180 nm
HF switch

Commercial DAC

Test vehicle

2019
STEP 1

CLAROCv2
XFAB 180 nm
HF switch
DAC 13bits

2021
STEP 2

CLAROCv3
XFAB 180 nm
HF switch

LADOCv1
TSMC 130 nm
DAC **13bits**

2022
STEP 3

CLAROCv4
XFAB 180 nm
HF switch

LADOCv2
TSMC 130 nm
DAC **16bits**