A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs.

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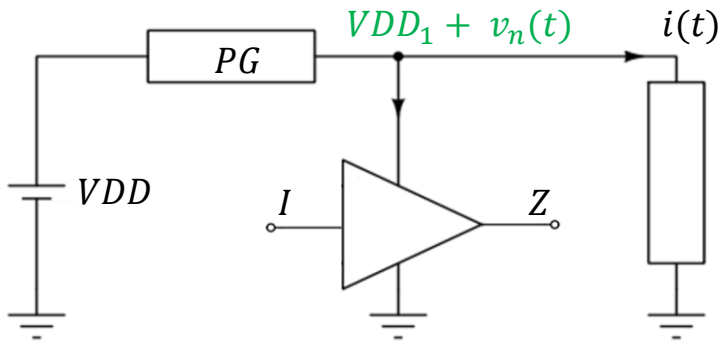
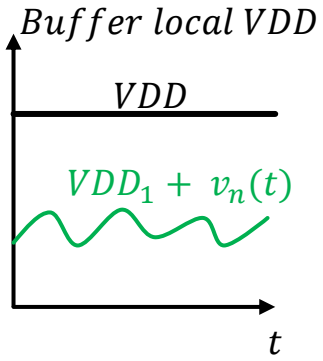
Summary

- Introduction: power supply induced jitter and timing resolution for an ASIC.
- Procedure and simulation steps for deriving IR-drop-induced jitter.
- Practical example: evaluating power-supply induced clock jitter for ALTIROC3 HGTD ASIC.

Power supply induced jitter

IR drop -> voltage drop across the ASIC power grid due to current flowing in it.

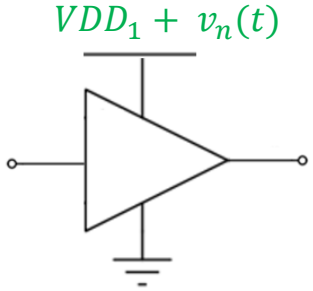


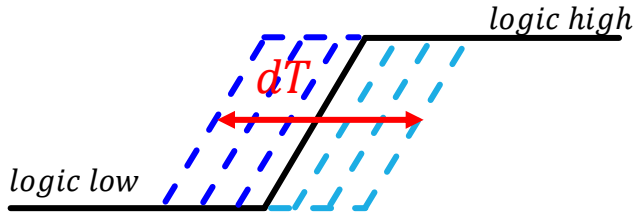


$$1)\ \frac{di(t)}{dt} \rightarrow v_n(t)$$

- Static: due to average current crossing conductor.
- **Dynamic**: dynamic current drawn by the circuit.

Power supply noise degrades propagation delay and output slope -> **jitter** (dT).





$$2)\ \frac{di(t)}{dt} \rightarrow v_n(t) \rightarrow \boldsymbol{dT}$$

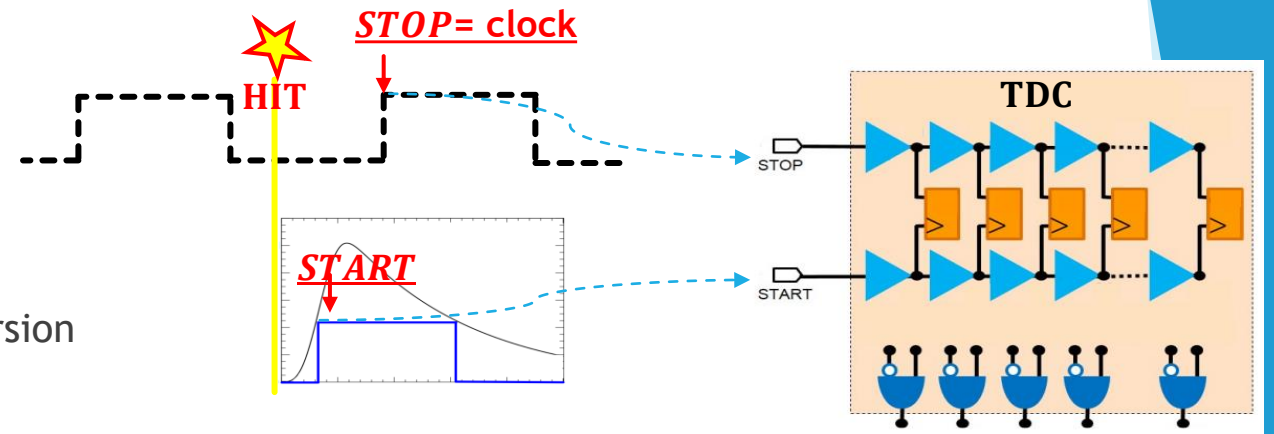
High timing precision ASICs – TDC based chain timing resolution

4D tracking: include timing measurement in tracking.

- **T**ime **O**f **A**rrival (**TOA**): time elapsed between arrival time of the hit and a reference (ex: ASIC clock)
- **T**ime **O**ver **T**hreshold (**TOT**): energy measurement.

TDC-based chain:

1. Hit is digitalized (analog front-end)
2. **T**ime-to-**d**igital **c**onverter (**TDC**) performs conversion



Timing resolution:

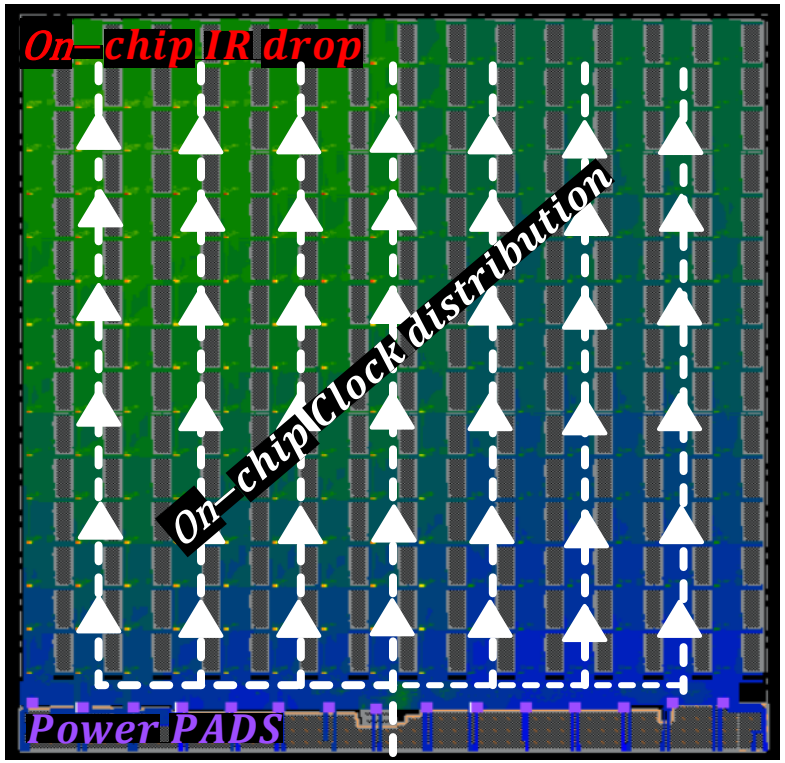
$$\sigma^2_{ASIC} = \sigma^2_{analogFE} + \sigma^2_{conversion} + \boldsymbol{\sigma^2_{clock}}$$

σ^2_{clock} : generation (PLL, dividers,…) and **distribution**

Timing resolution and power supply induced jitter?

σ^2_{clock} : generation (PLL, dividers,…) and **distribution**

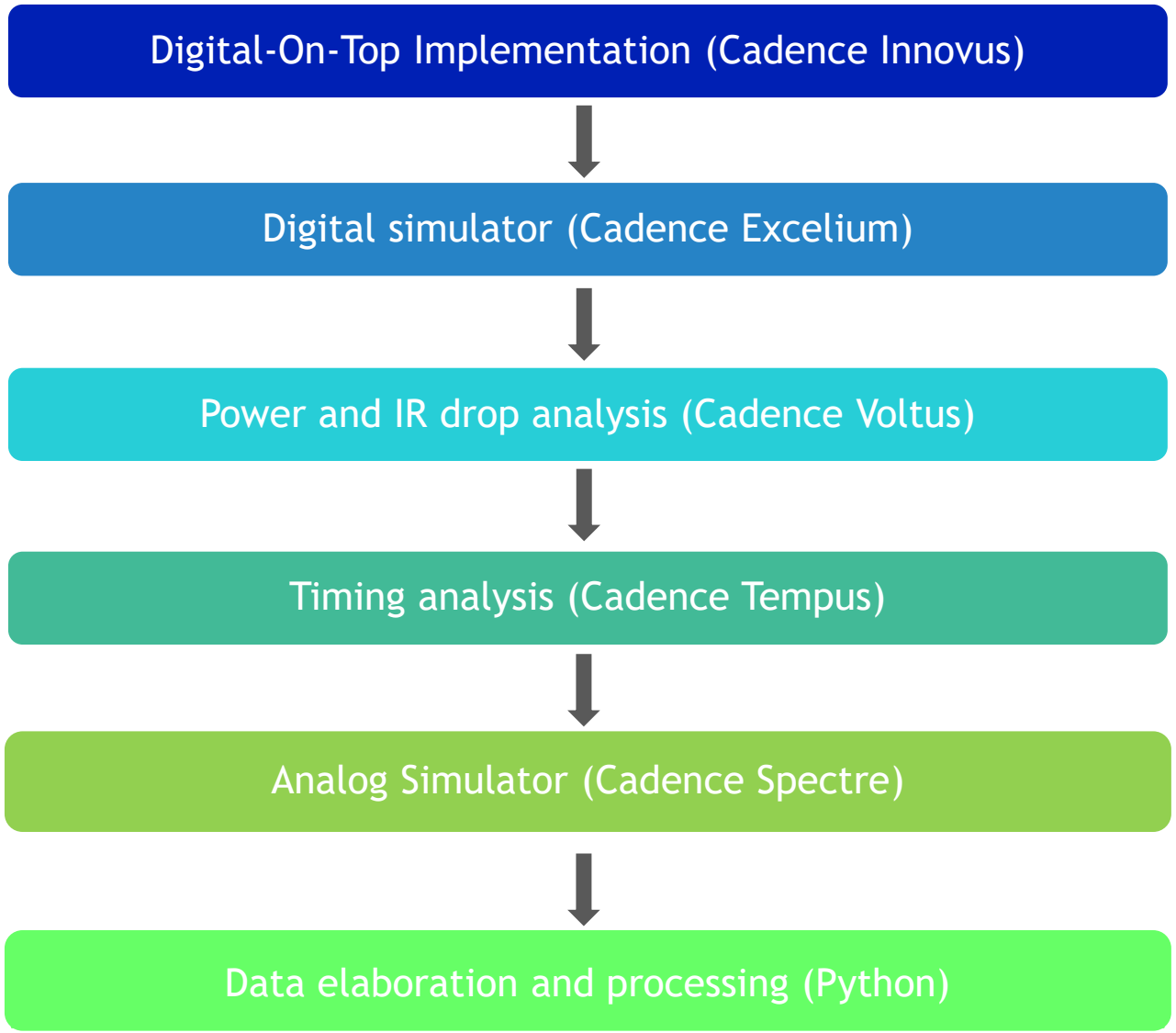
On-chip clock distribution can be affected by on-chip IR-drop and IR-drop-induced clock jitter.



- **What is the impact of on-chip dynamic IR-drop on clock distribution?**
- **Knowing $v_n(t)$, is it possible to know dT for every pixel in the ASIC?**

$$\frac{di(t)}{dt} \rightarrow v_n(t) \rightarrow dT$$

Flow and procedure based on commercial Cadence suite.



Procedure and simulation steps - 1

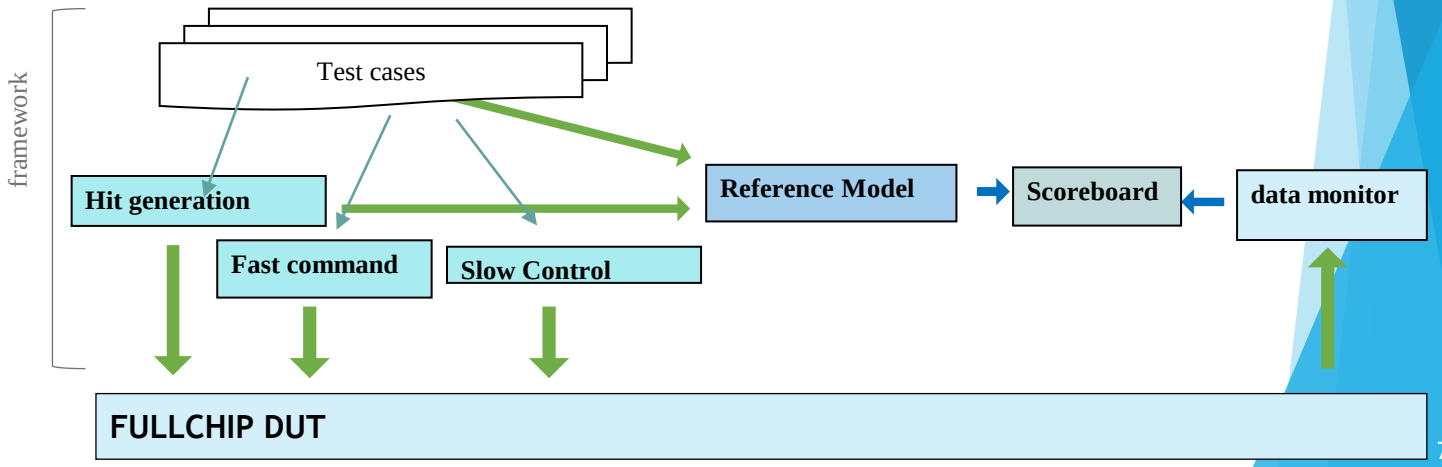
1. **Fullchip Digital-On-Top design**
   - Fullchip design assembled in Cadence Innovus.
   - Analog macro characterized with libfile, abstract and Verilog models.

Output: **netlist and SDF for realistic simulation**.
Corners, typ, min and max.

2. **Simulation environment** to emulate real-life of the ASIC
   - Digital simulation for full-chip verification.
   - Realistic stimuli, ASIC configurations, output bandwidth,…

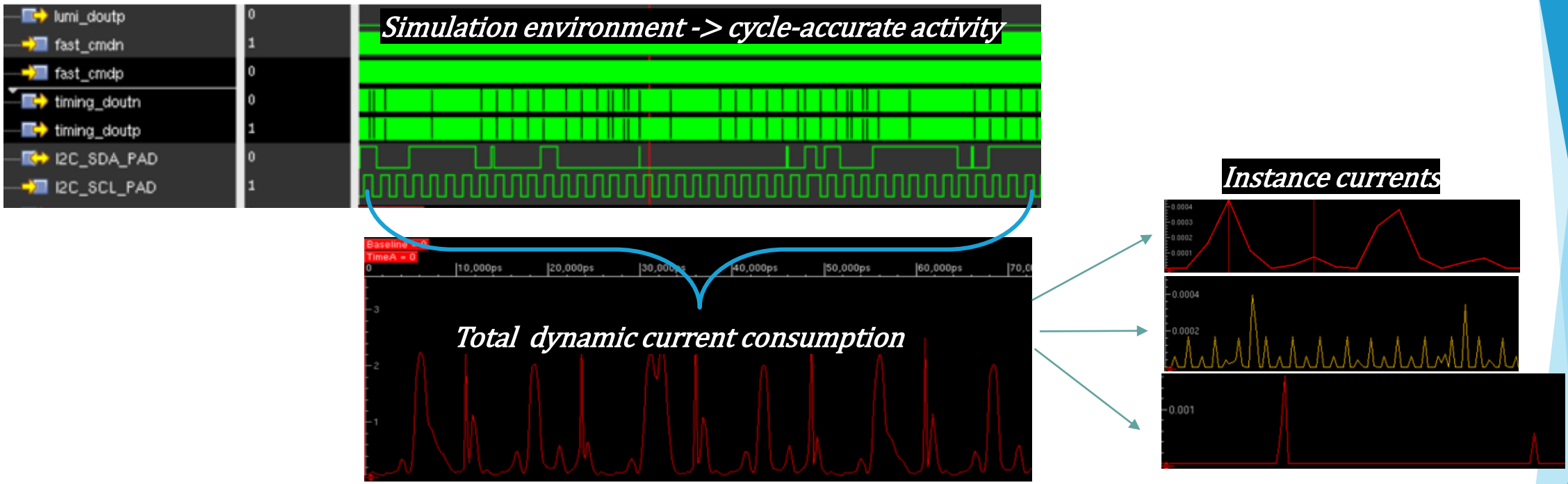
Output: activity vectors.

Cycle-accurate Instance-based activity information.



Procedure and simulation steps - 2

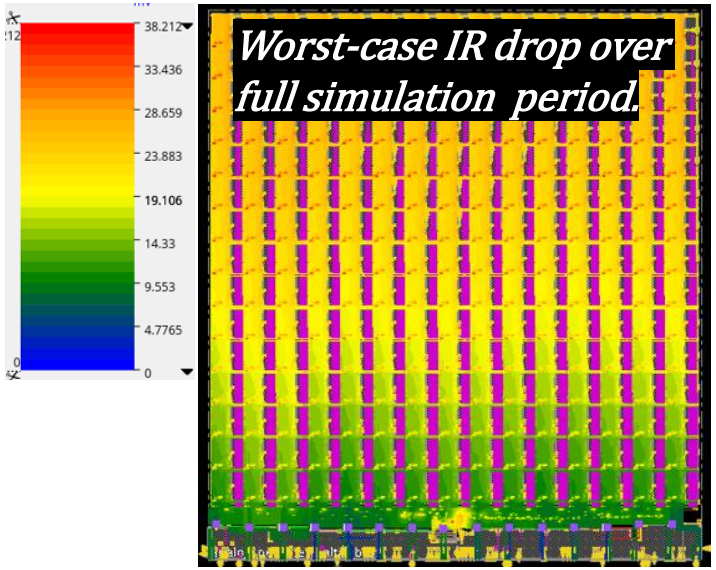
3. **Dynamic power in Cadence Voltus**
   - DoT approach: fullchip analysis
   - Dynamic power analysis extracts **current consumption** for every cell in design, based on activity information per cycle.



Procedure and simulation steps - 3

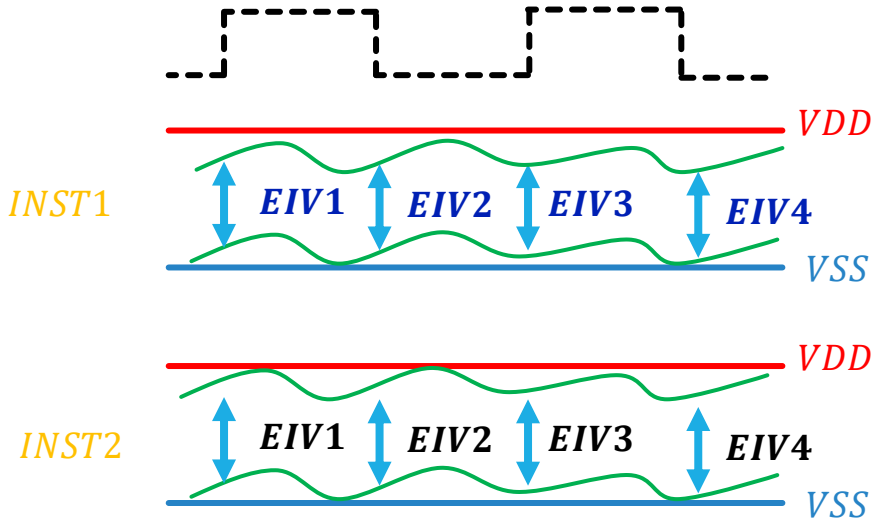
4. **Dynamic IR-drop analysis in Cadence Voltus**

Dynamic IR drop applies current waveforms to power grid, extracts IR drop for power nets (net-based analysis) and for instances (domain-based analysis).



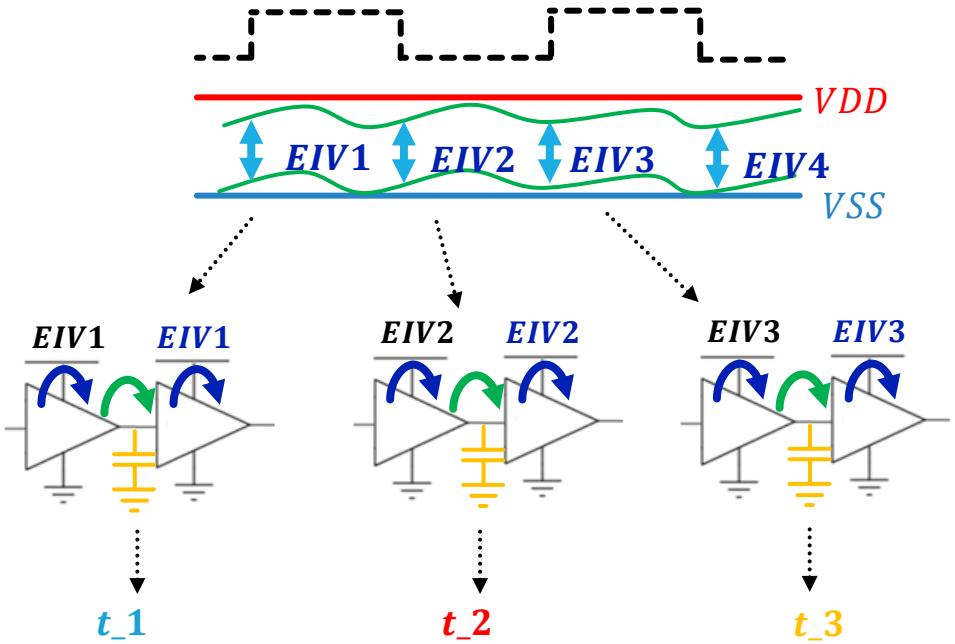
Output: **Effective Instance Voltage file (EIV)**

Real VDD-VSS (Effective instance voltage) seen by every cell in design, for every cycle, at the moment of switching.



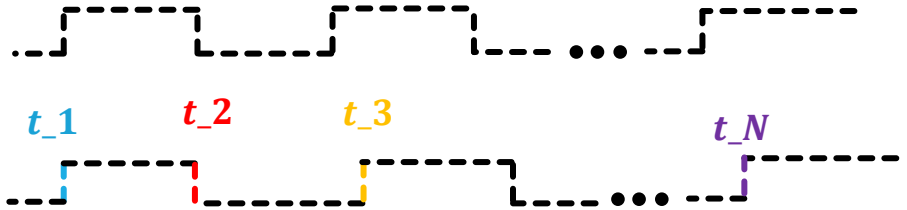
Procedure and simulation steps - 4

5. **Cycle-to-Cycle analog simulation with realistic power supplies.**
   - Static Timing Analysis tool (Cadence Tempus) is provided with EIV files and exports the path to be analyzed to analog simulator (Cadence Spectre) via a Spice netlist.
   - One analog simulation for every switching cycle of EIV file, each element annotated with its EIV (EIV1, EIV2,…)
   - Measure rising and falling time through cells and nets.



Output: summing up all the cell and net delays in the path, which now are impacted by IR-drop effect:

Effective Arrival time including IR drop effect, per cycle.

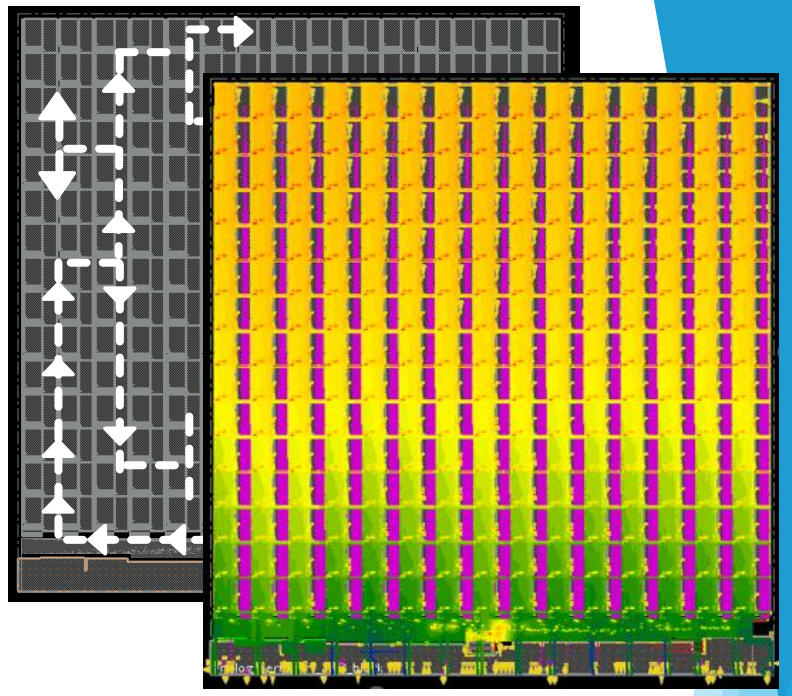


Ir-drop-induced peak-to-peak clock jitter.

$$Peak - To - Peak\ Jitter = Max(t_0, t_1, t_2, .. t_N) - Min(t_0, t_1, t_2, .. t_N)$$

Practical example: ALTIROC3 case study.

Dedicated presentation: *"Verification Environment for ALTIROC ASIC of the ATLAS High Granularity Timing Detector"*, https://indico.cern.ch/event/1255624/contributions/5443840.



- 2x2cm ASIC, 15x15 pixels.
- TOA/TOT measurements, TDC-based chain.
- Measure clock40MHz distributed from periphery to full pixel matrix. $\pm\, 150ps\ skew$.
- Peripheral wire-bonding for VDD/VSS.
- Increasing IR drop over the matrix.

Study IR-drop-induced jitter in real-life conditions.

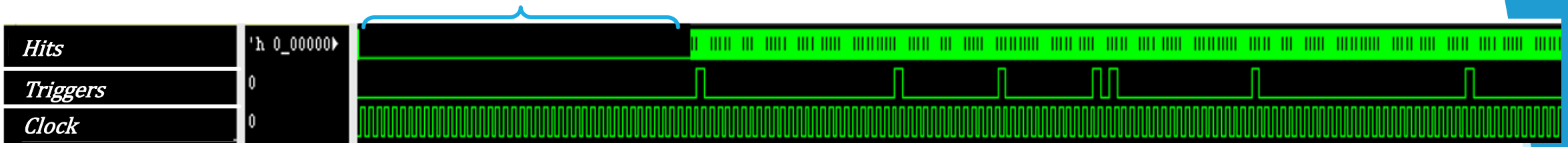
- Impinging hits triggers timing measurement and storage.
- Triggered readout activates data transmission.

} Varying digital activity inside ASIC -> stability of power grid and jitter of measure clock?

Practical example: ALTIROC3 case study.

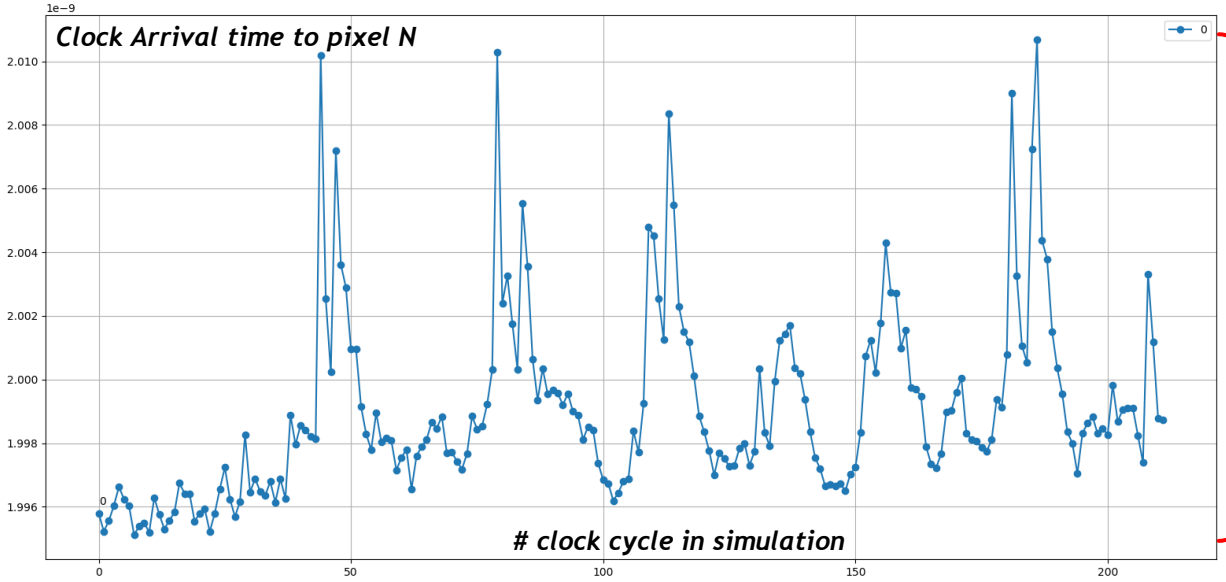
Simulation scenario

1. «IDLE state»: ASIC out of reset, no hits nor triggers (fsm in IDLE state,…). No activity.



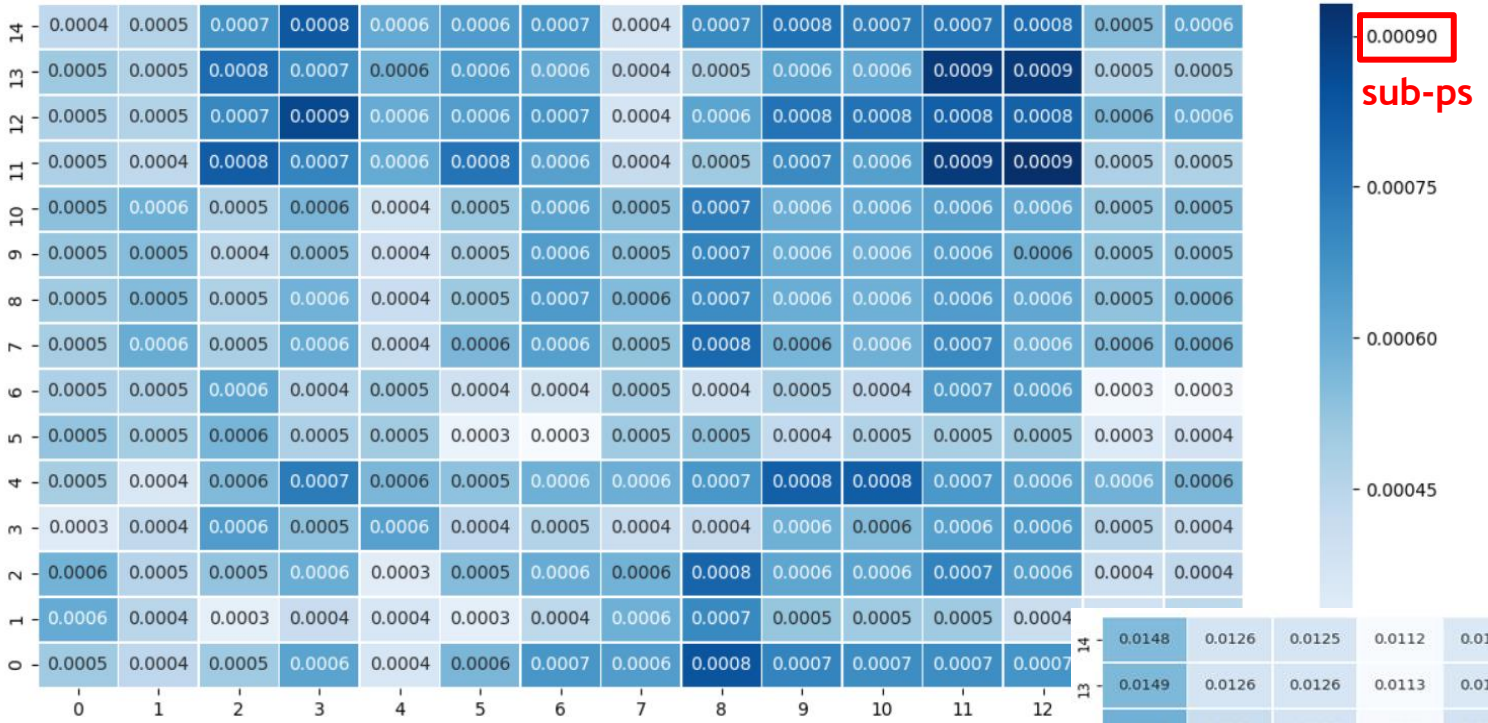
2. «Normal operation»: hits and triggers injected following real physics events.

Evolution in time of clock delay is derived for all 225 pixels and peak-to-peak jitter is derived



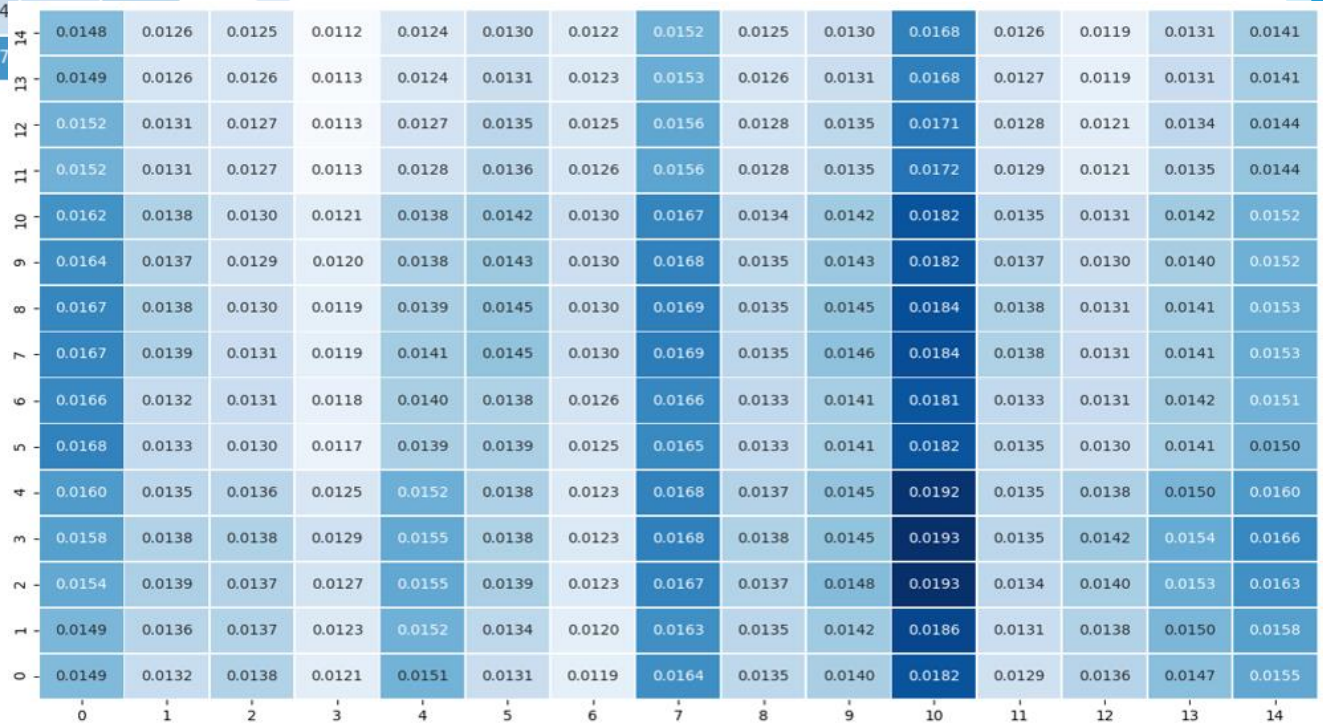
$$Peak - To - Peak\ Jitter = Max(t_0, t_1, t_2, .. t_N) - Min(t_0, t_1, t_2, .. t_N)$$

Practical example: ALTIROC3 case study.

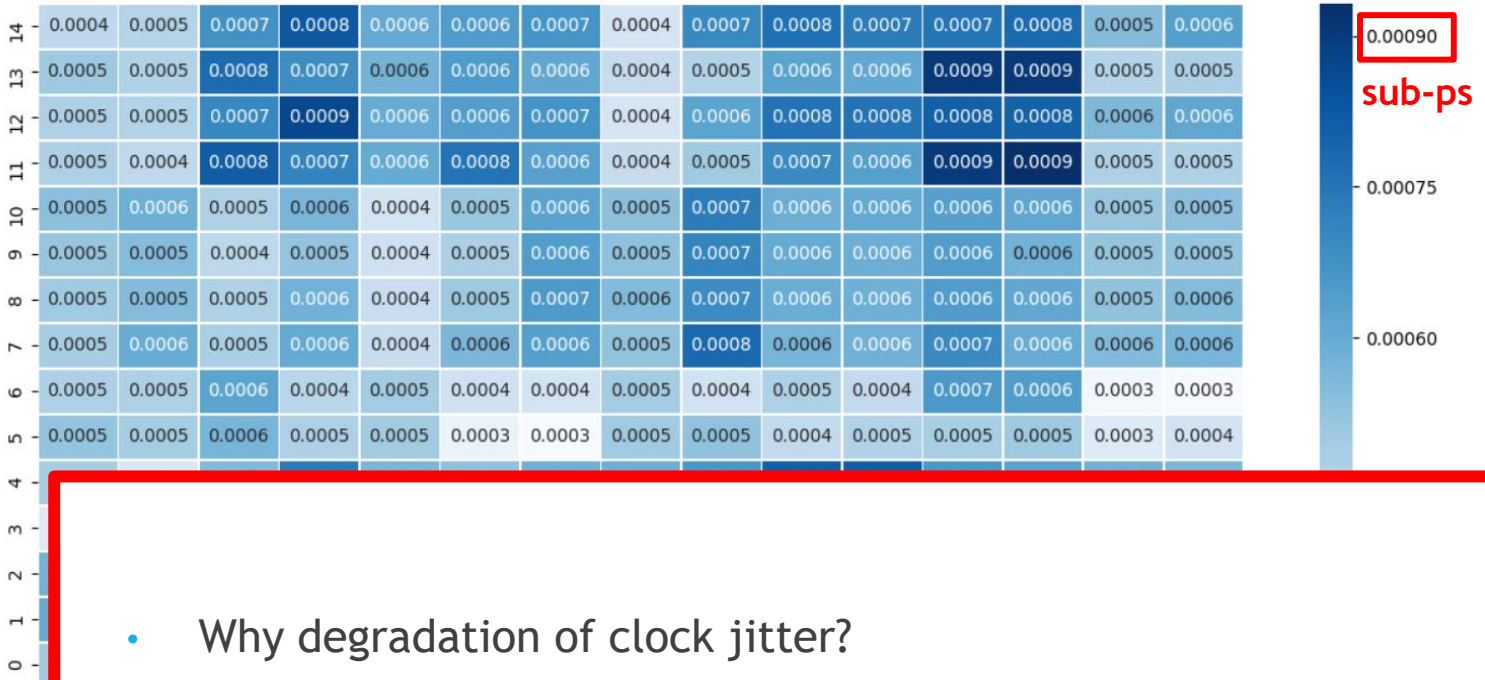


- Typ corner (1.2V, typ sdf delays).
- Peak-to-Peak jitter in ns.
- Worst case per pixel is reported here.

- Scenario 1) (top)
  - No hits/triggers
  - Sub-ps IR-drop-induced jitter
- Full simulation length (right)
  - Digital activity produces jitter degradation.



Practical example: ALTIROC3 case study.



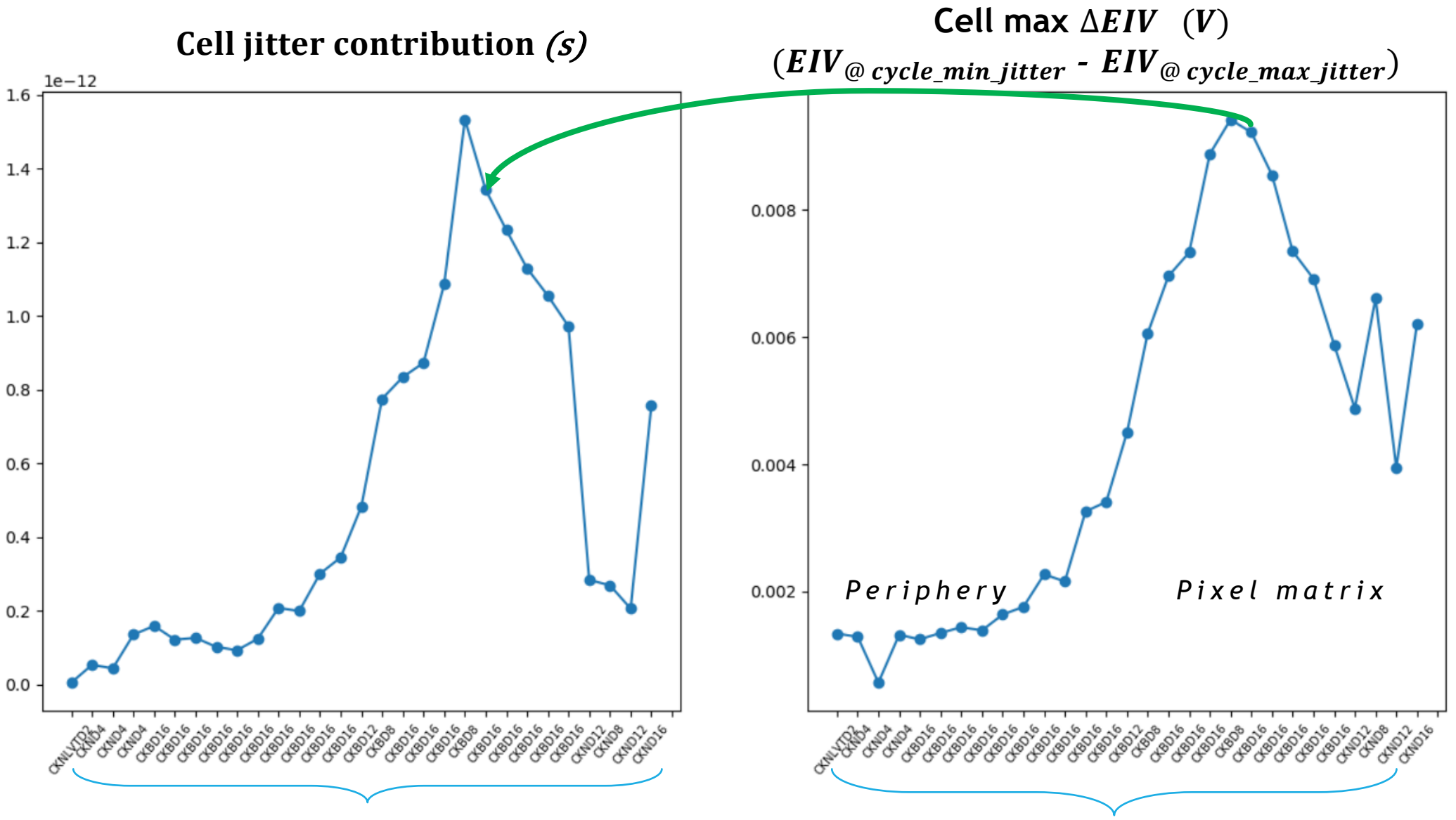
- Typ corner (1.2V, typ sdf delays).
- Peak-to-Peak jitter in ns.
- Worst case <u>per pixel</u> is reported here.

- Why degradation of clock jitter?
- Which elements in the clock distribution to pixel *N* suffer the most?

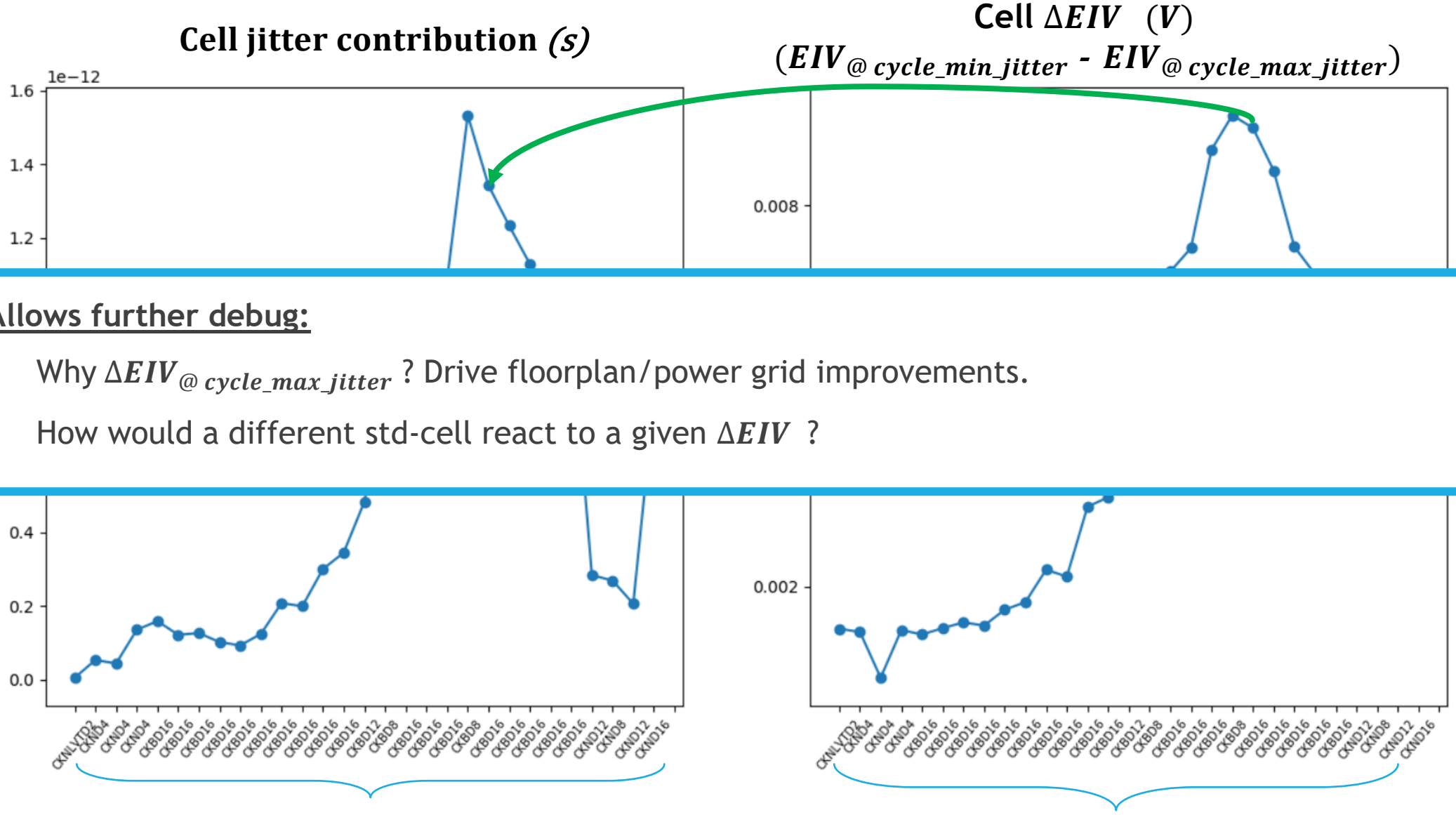
- No hits/triggers
- Sub-ps IR-drop-induced jitter

- Full simulation length (right)
  - Digital activity produces jitter degradation.

Jitter degradation of clock to Pixel N



Single pixel jitter degradation study



Allows further debug:

- Why $\Delta EIV_{@\ cycle\_max\_jitter}$? Drive floorplan/power grid improvements.
- How would a different std-cell react to a given ΔEIV ?

Clock distribution to pixel N

Conclusions

Jitter analysis methodology allows deriving **realistic delays inside ASIC considering IR-drop effects**

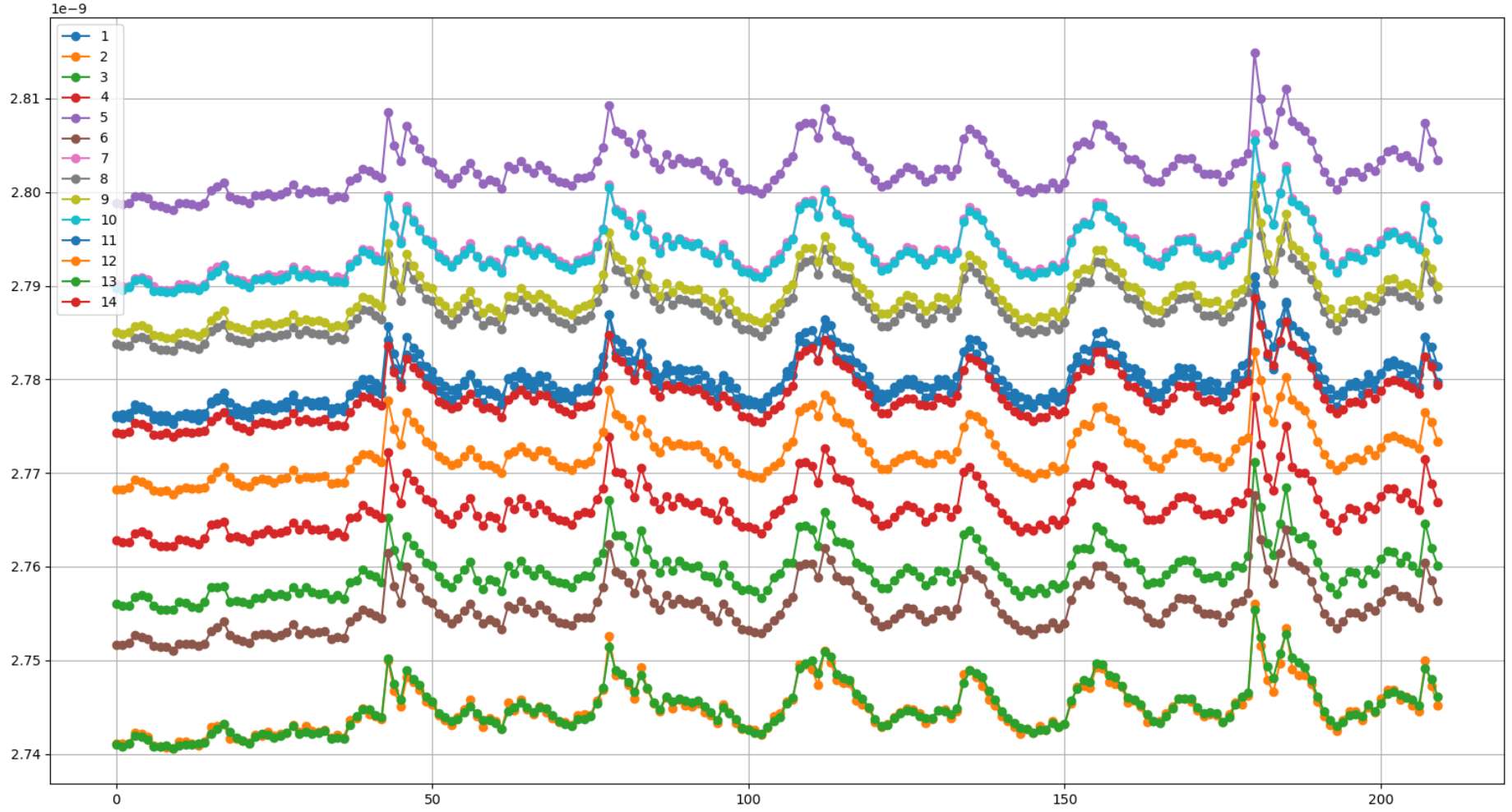
- High-Resolution timing ASICs.

… whatever application where jitter is important (ex: PLL, High-speed circuits.).

Questions?

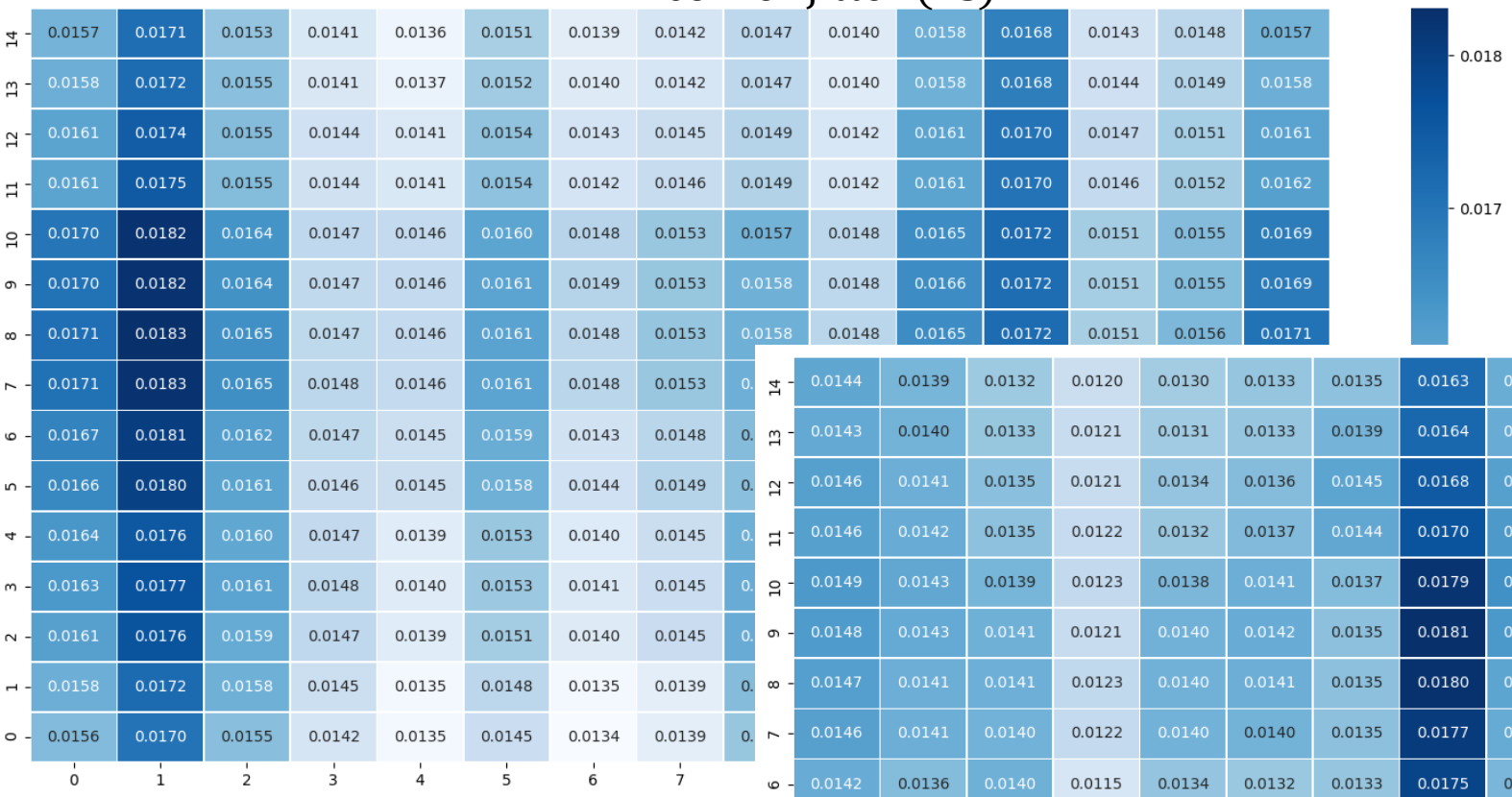
Backup

Clock arrival time 2nd scenario for 15 pixels in a column.

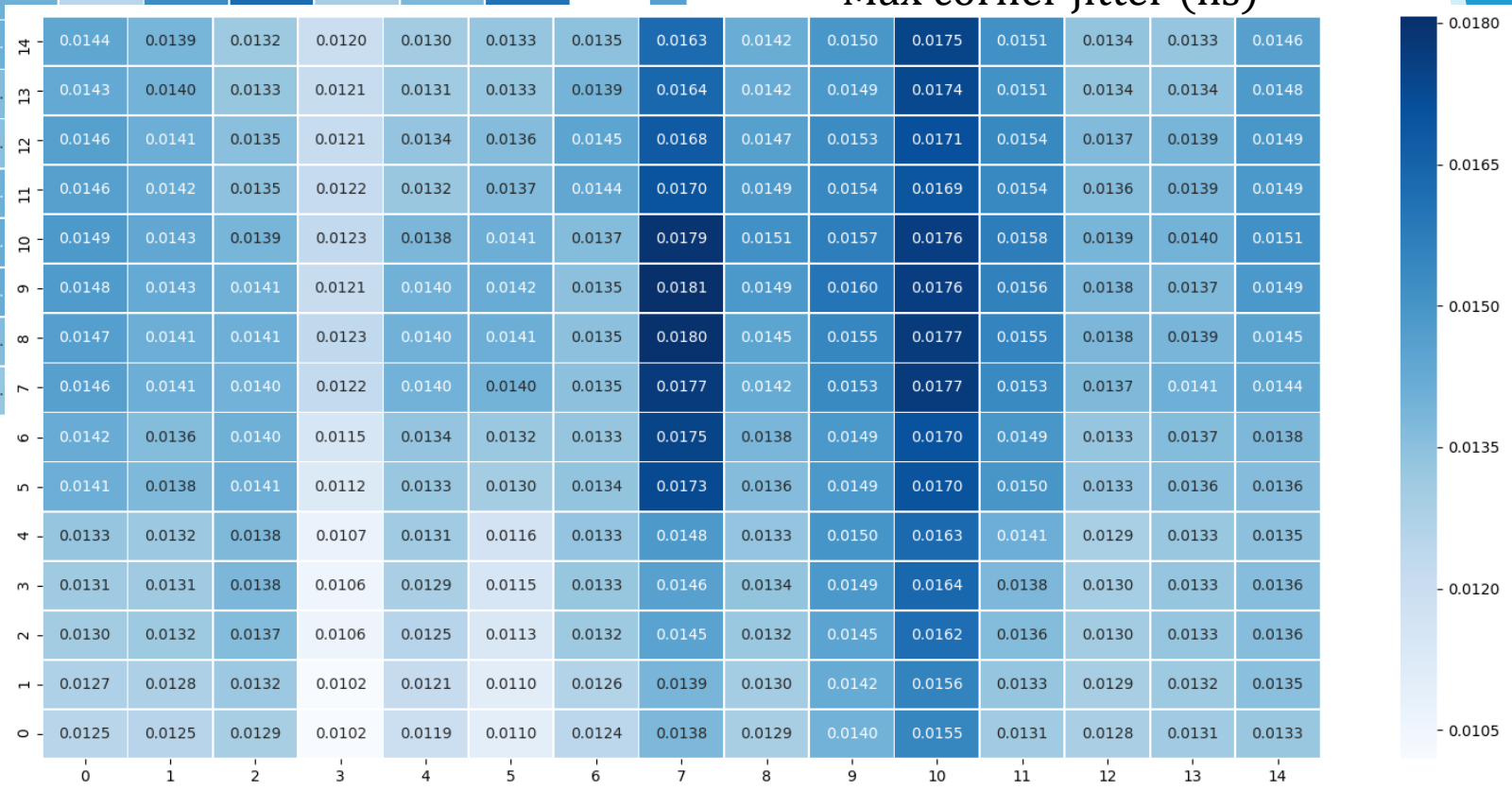


Min and Max corners

Min corner jitter (ns)



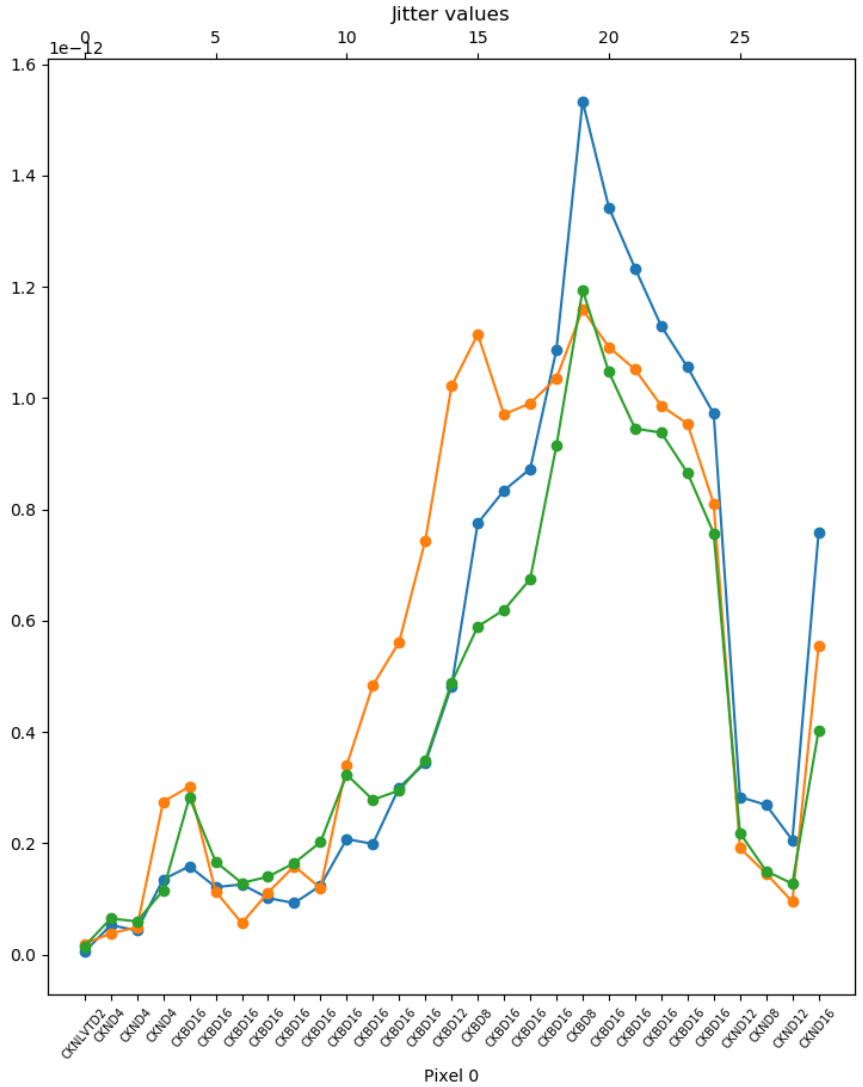
Max corner jitter (ns)

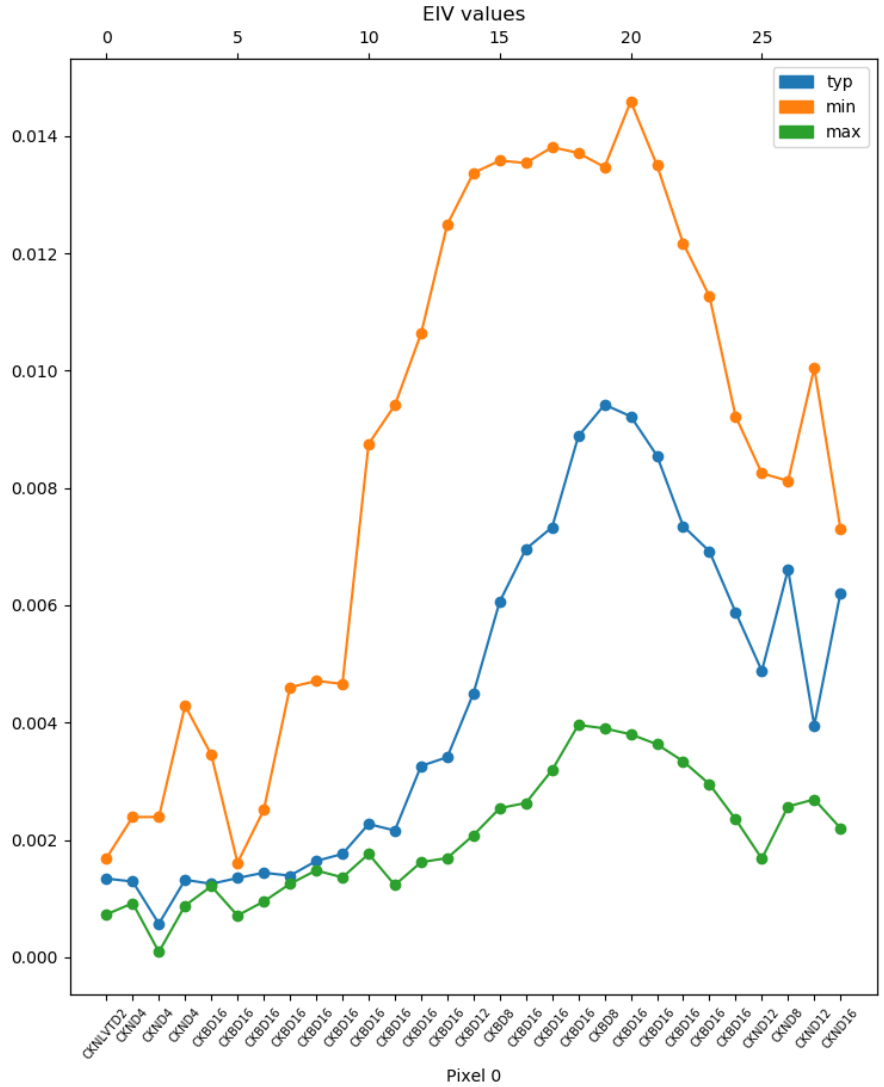


Single pixel jitter degradation study in 3 corners

EIV and jitter degradation of clock path to pixel 0 in 3 different corners.

Cycle with min and max arrival time is different in different cornes (Typ: 11-182 Min: 7-186 Max: 10-183)



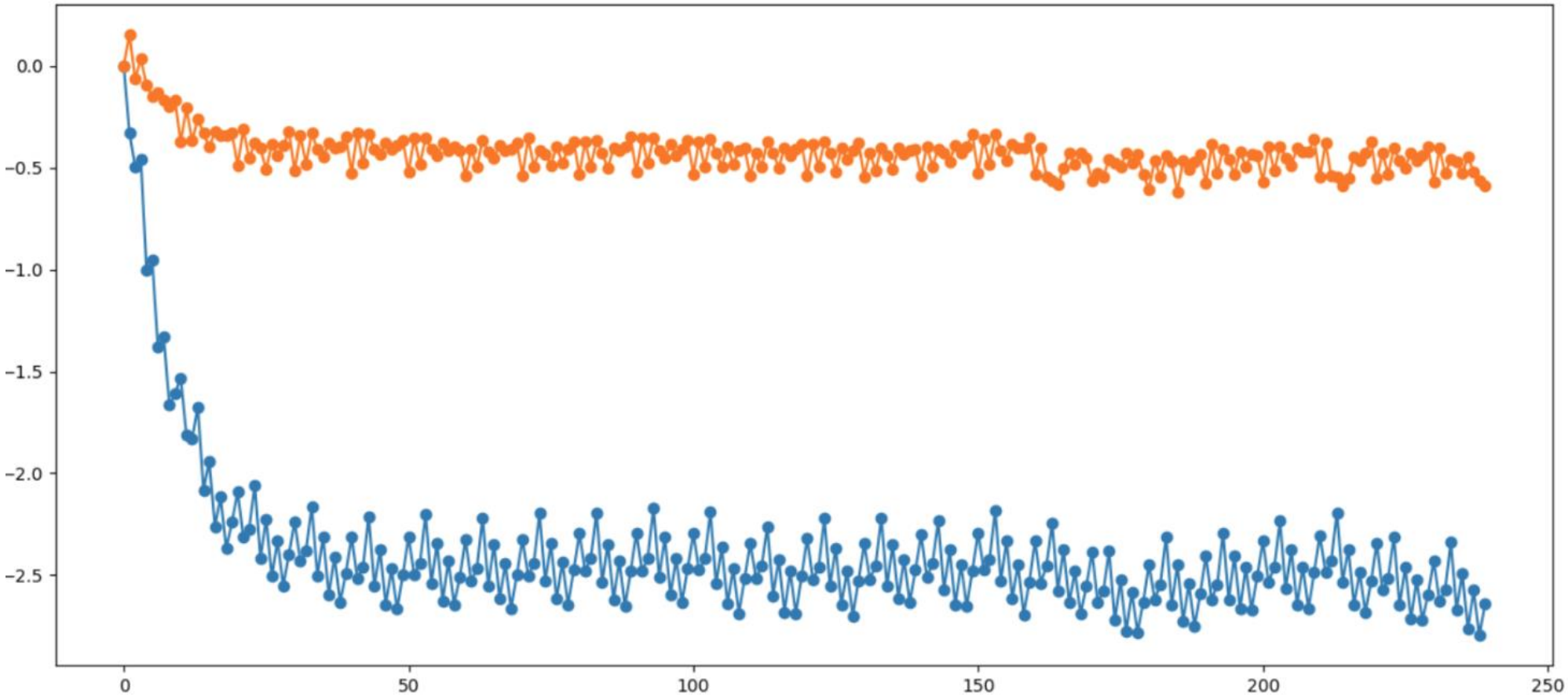


MIN -> larger ΔEIV, faster cell transition times (jitter is less affected by ΔEIV).

MAX -> smaller ΔEIV, larger cell transition times (jitter is more affected by ΔEIV).

balance?

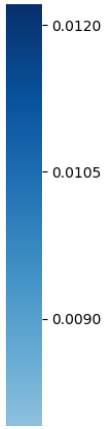
Voltage degradation



CLOCK DIGITAL

TYP jitter (ns)

	0	1	2	3	4	5	6	7	8	9	10	11
14	0.0107	0.0093	0.0093	0.0090	0.0086	0.0085	0.0102	0.0108	0.0097	0.0103	0.0122	0.0104
13	0.0108	0.0094	0.0090	0.0087	0.0085	0.0083	0.0101	0.0107	0.0098	0.0102	0.0118	0.0100
12	0.0104	0.0091	0.0088	0.0084	0.0082	0.0080	0.0097	0.0103	0.0095	0.0100	0.0115	0.0097
11	0.0099	0.0089	0.0082	0.0084	0.0080	0.0075	0.0094	0.0098	0.0092	0.0096	0.0113	0.0096
10	0.0095	0.0085	0.0078	0.0081	0.0077	0.0072	0.0091	0.0094	0.0089	0.0093	0.0108	0.0093
9	0.0090	0.0082	0.0075	0.0079	0.0075	0.0070	0.0086	0.0091	0.0085	0.0090	0.0104	0.0090
8	0.0085	0.0079	0.0073	0.0076	0.0072	0.0067	0.0083	0.0087	0.0082	0.0086	0.0100	0.0087
7	0.0081	0.0075	0.0071	0.0074	0.0069	0.0065	0.0079	0.0082	0.0079	0.0083	0.0095	0.0084
6	0.0078	0.0071	0.0068	0.0071	0.0065	0.0063	0.0075	0.0079	0.0075	0.0080	0.0090	0.0080
5	0.0074	0.0067	0.0065	0.0068	0.0062	0.0060	0.0071	0.0073	0.0072	0.0076	0.0086	0.0077
4	0.0071	0.0063	0.0062	0.0065	0.0059	0.0059	0.0067	0.0068	0.0068	0.0072	0.0080	0.0073
3	0.0069	0.0061	0.0060	0.0062	0.0057	0.0056	0.0063	0.0063	0.0064	0.0068	0.0075	0.0069
2	0.0065	0.0058	0.0058	0.0059	0.0055	0.0054	0.0059	0.0058	0.0059	0.0065	0.0069	0.0065
1	0.0062	0.0056	0.0055	0.0057	0.0053	0.0052	0.0056	0.0053	0.0056	0.0059	0.0064	0.0061
0	0.0058	0.0054	0.0054	0.0054	0.0051	0.0050	0.0052	0.0049	0.0052	0.0056	0.0059	0.0058



Skewed clock (very different from clock 40MHz measurement)

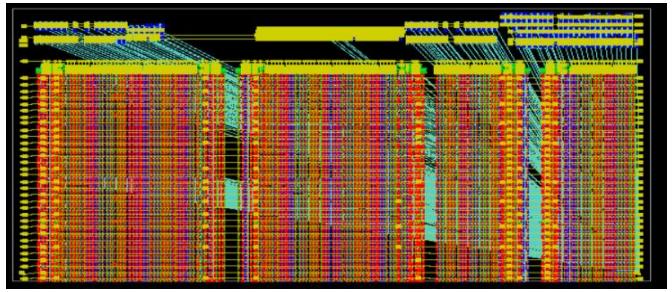
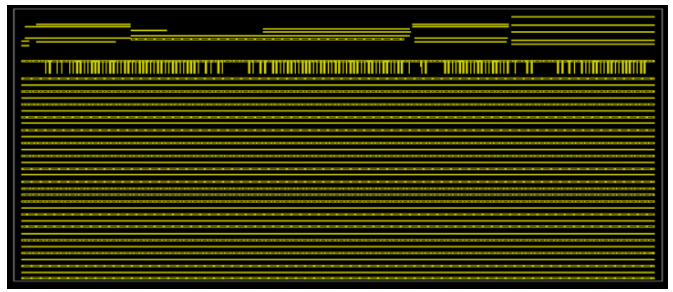
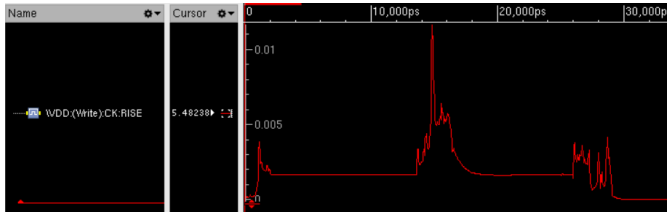
TYP insertion delay (ns)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
14	3.4431	3.3693	3.2661	3.1609	3.0561	2.9520	2.8460	2.6898	2.7917	2.8968	3.0003	3.1035	3.2046	3.3058	3.3794
13	3.3753	3.3006	3.1974	3.0922	2.9873	2.8833	2.7772	2.6211	2.7230	2.8280	2.9315	3.0347	3.1359	3.2370	3.3106
12	3.2832	3.2089	3.1057	3.0004	2.8956	2.7915	2.6855	2.5293	2.6313	2.7363	2.8398	2.9430	3.0442	3.1454	3.2189
11	3.1758	3.1015	2.9984	2.8932	2.7883	2.6842	2.5782	2.4220	2.5240	2.6290	2.7324	2.8356	2.9368	3.0380	3.1115
10	3.0819	3.0076	2.9044	2.7992	2.6943	2.5902	2.4842	2.3280	2.4300	2.5350	2.6385	2.7416	2.8428	2.9440	3.0176
9	2.9873	2.9130	2.8098	2.7045	2.5997	2.4956	2.3896	2.2334	2.3353	2.4403	2.5440	2.6470	2.7482	2.8493	2.9229
8	2.8919	2.8175	2.7144	2.6091	2.5042	2.4001	2.2941	2.1380	2.2399	2.3449	2.4485	2.5516	2.6528	2.7539	2.8275
7	2.7947	2.7196	2.6164	2.5112	2.4063	2.3023	2.1962	2.0401	2.1420	2.2470	2.3506	2.4537	2.5548	2.6560	2.7296
6	2.6964	2.6206	2.5174	2.4122	2.3073	2.2032	2.0972	1.9410	2.0430	2.1480	2.2516	2.3546	2.4558	2.5570	2.6306
5	2.5988	2.5224	2.4193	2.3141	2.2092	2.1051	1.9990	1.8429	1.9448	2.0499	2.1534	2.2565	2.3577	2.4589	2.5324
4	2.5005	2.4237	2.3205	2.2153	2.1105	2.0064	1.9003	1.7442	1.8461	1.9511	2.0547	2.1578	2.2590	2.3601	2.4337
3	2.4015	2.3242	2.2210	2.1158	2.0109	1.9068	1.8008	1.6446	1.7466	1.8516	1.9552	2.0583	2.1595	2.2606	2.3342
2	2.3039	2.2261	2.1229	2.0177	1.9129	1.8088	1.7027	1.5466	1.6485	1.7536	1.8572	1.9602	2.0615	2.1626	2.2361
1	2.2041	2.1258	2.0227	1.9174	1.8126	1.7085	1.6025	1.4463	1.5482	1.6532	1.7569	1.8599	1.9611	2.0623	2.1359
0	2.1048	2.0263	1.9231	1.8179	1.7130	1.6090	1.5029	1.3467	1.4487	1.5537	1.6573	1.7603	1.8616	1.9627	2.0362

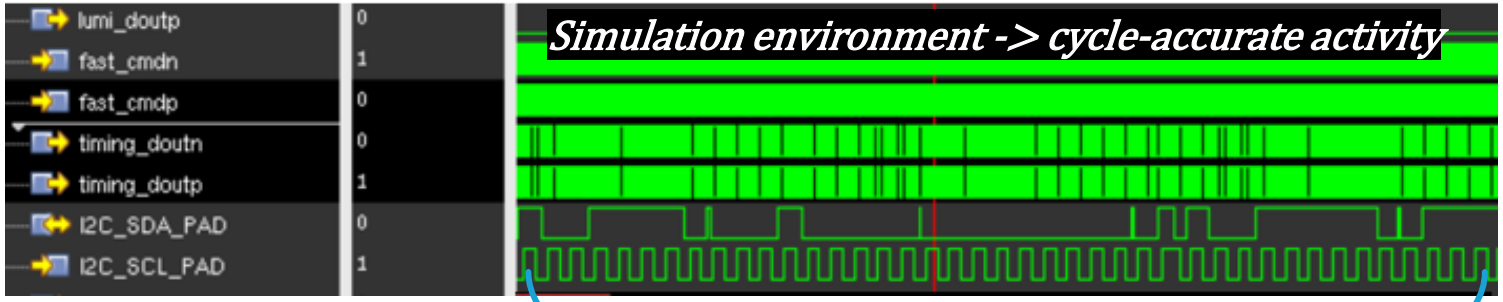
Procedure and simulation steps - 2

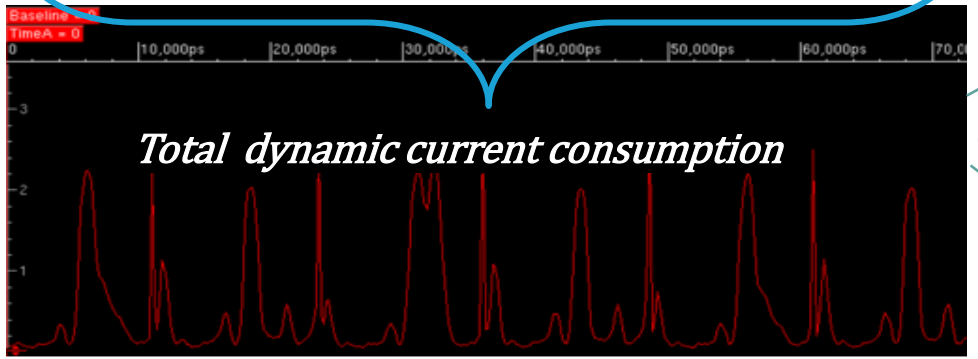
3. Dynamic power in Cadence Voltus

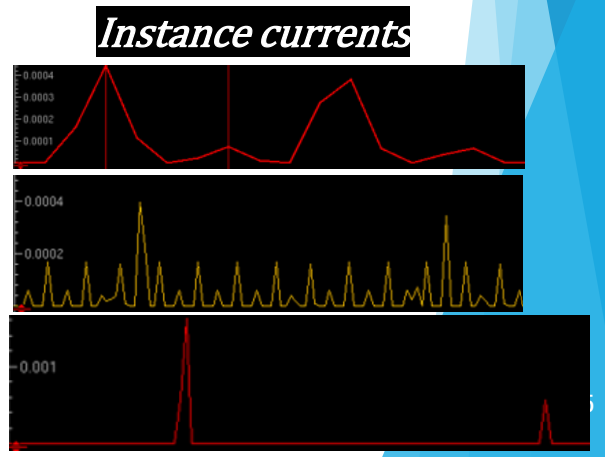
- DoT approach: fullchip analysis
  - Power Grid Libraries needed for analog macros (capacitance, current distribution).

- Dynamic power analysis extracts **current consumption** per cell based on activity information per cycle.



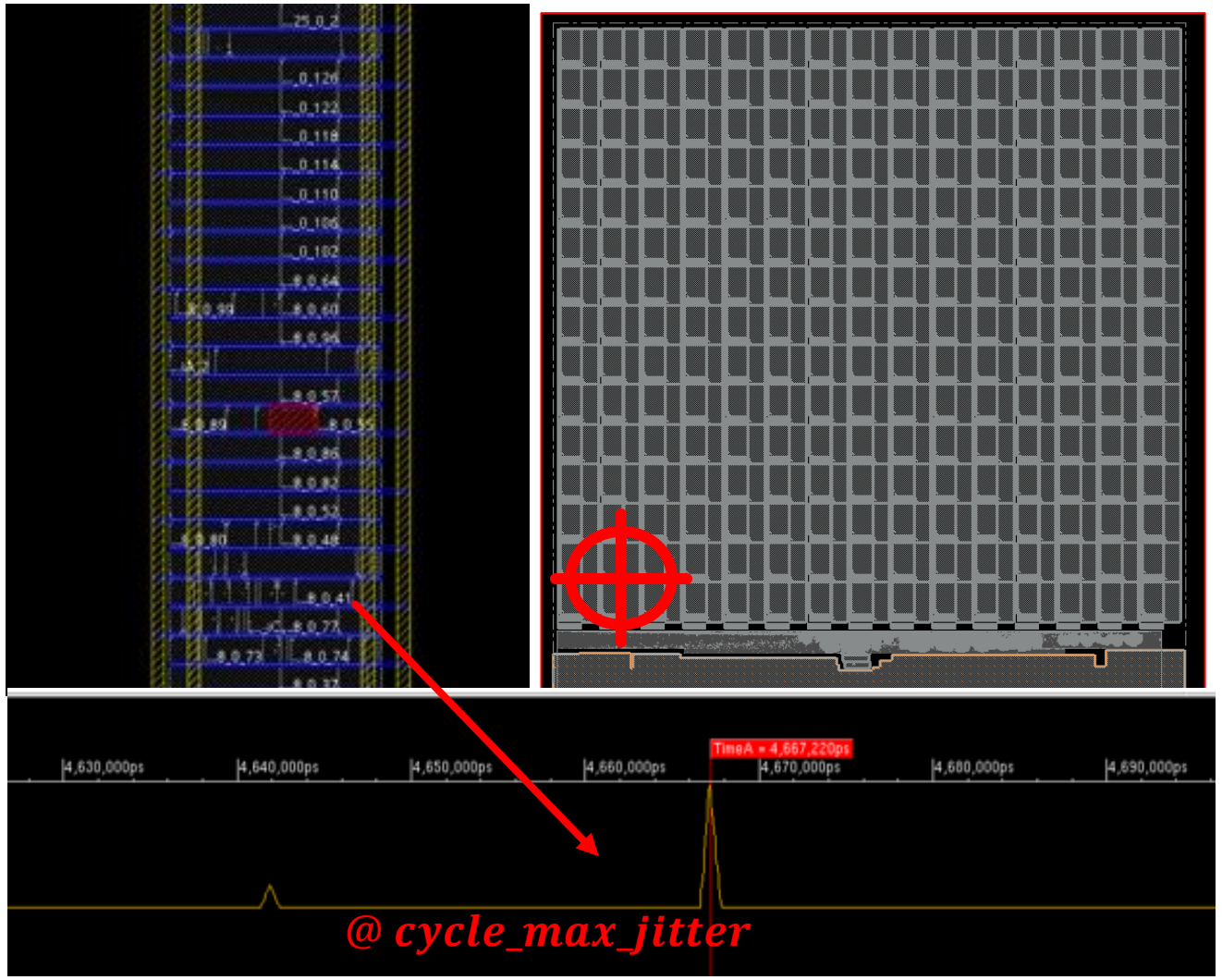


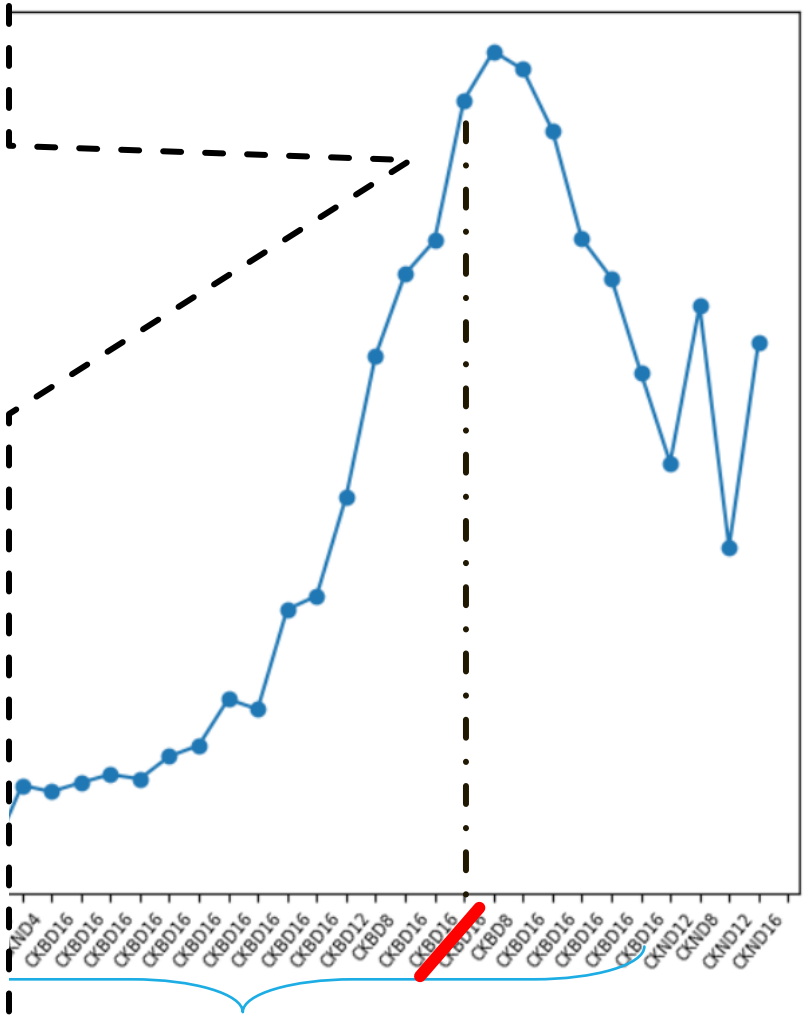


Single pixel jitter degradation study

Cell ΔEIV (V) Why?

$(EIV_{@\ cycle\_min\_jitter} - EIV_{@\ cycle\_max\_jitter})$

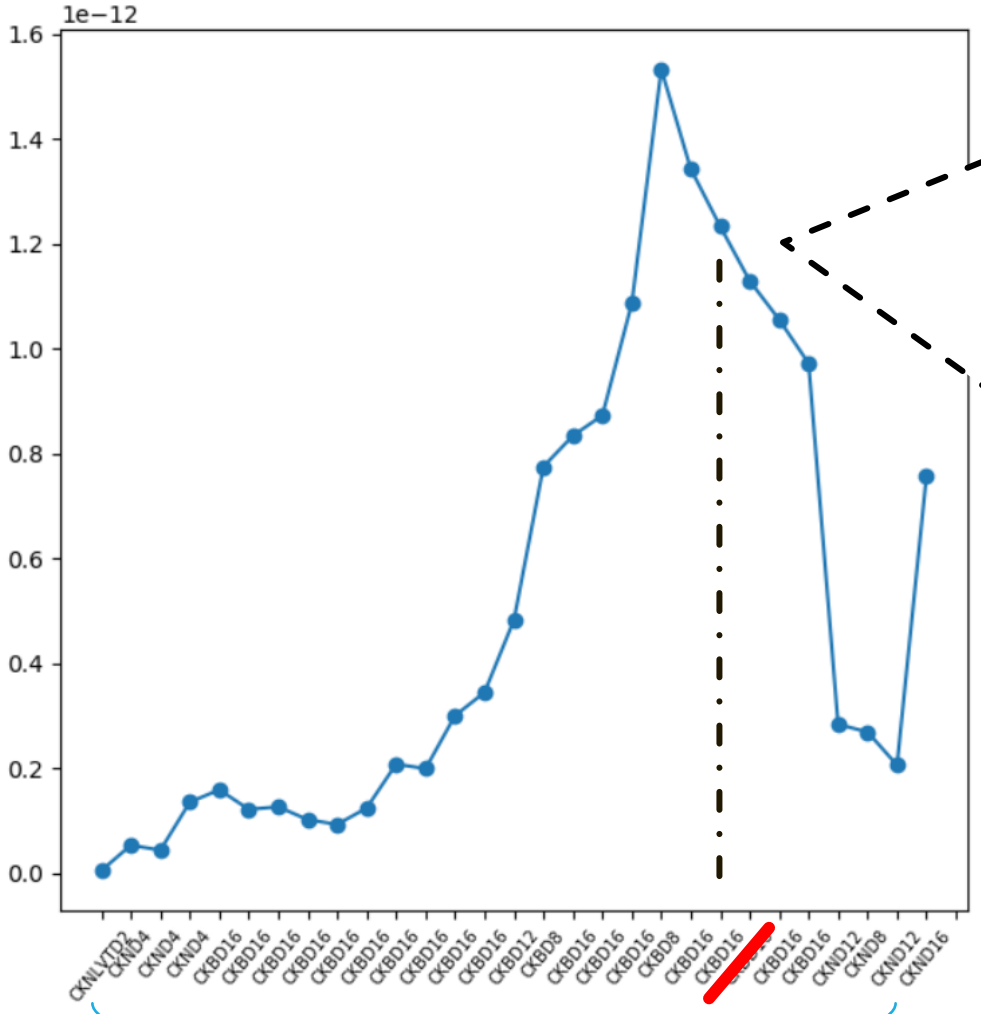




Clock distribution to pixel N

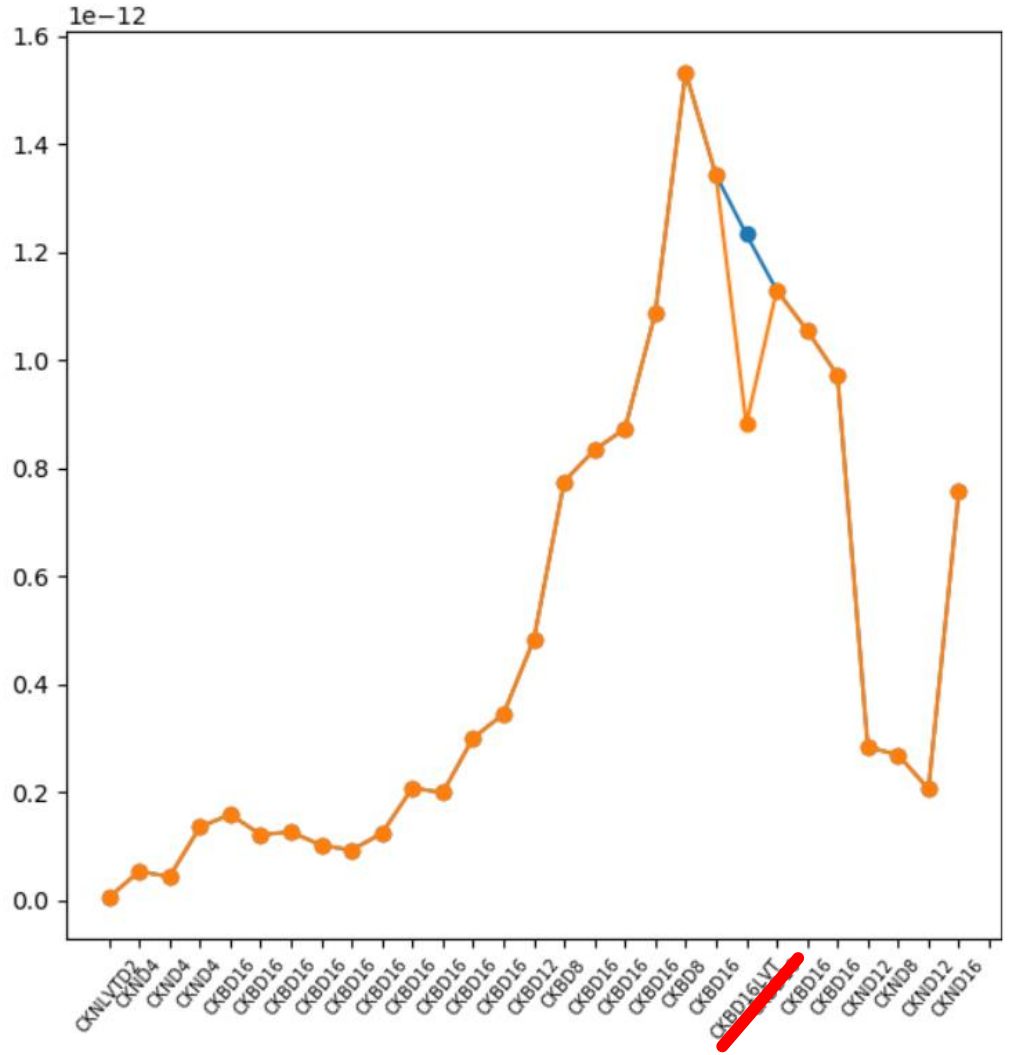
Single pixel jitter degradation study

Cell jitter contribution *(s)*



Clock distribution to pixel N

NV_{th} *to* LV_{th}?

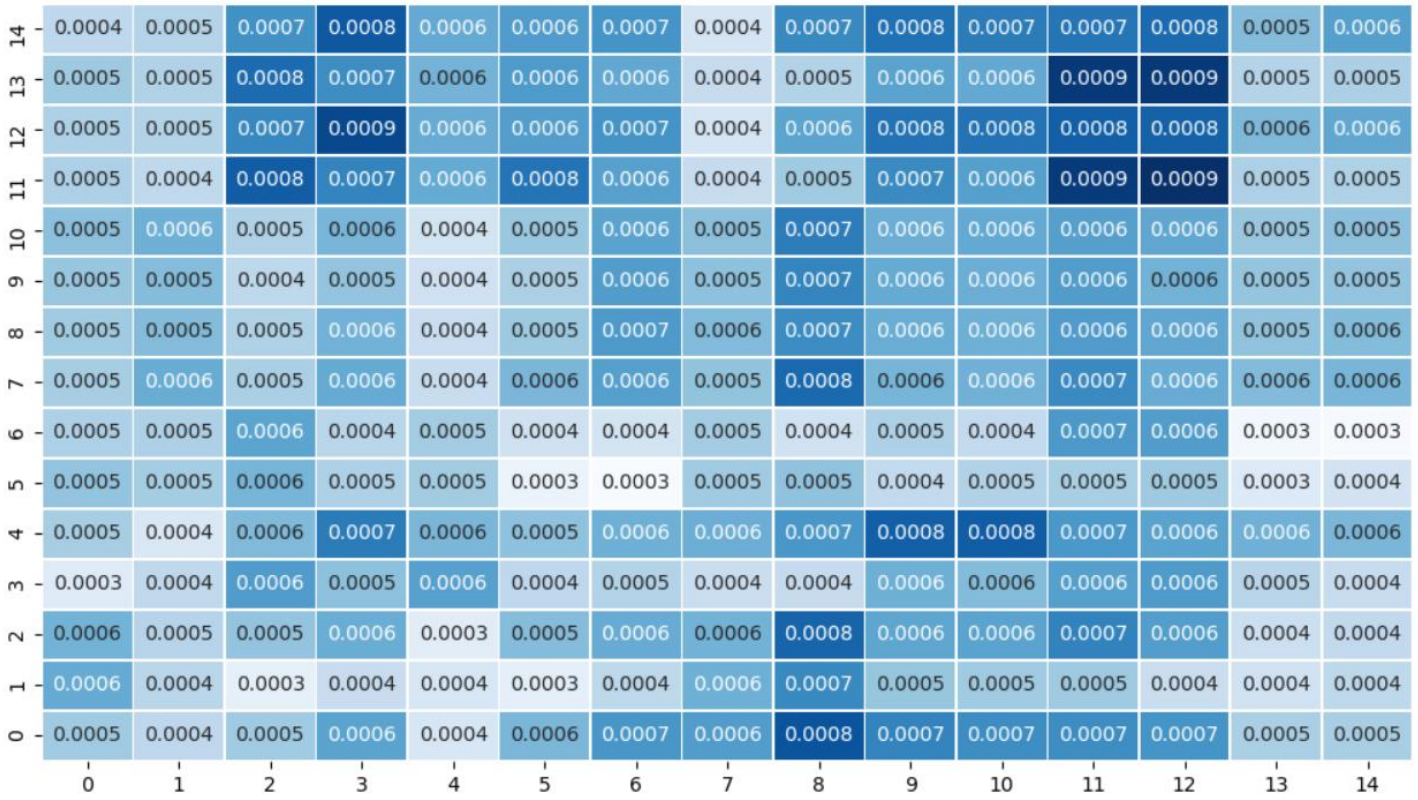


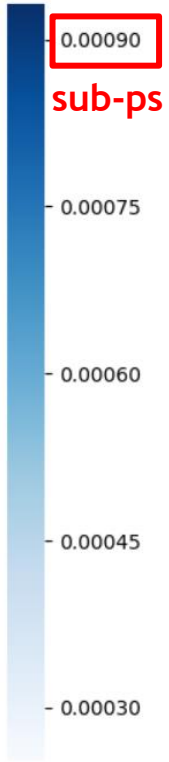
ALTIROC3 study. Scenario 1) results (No activity)

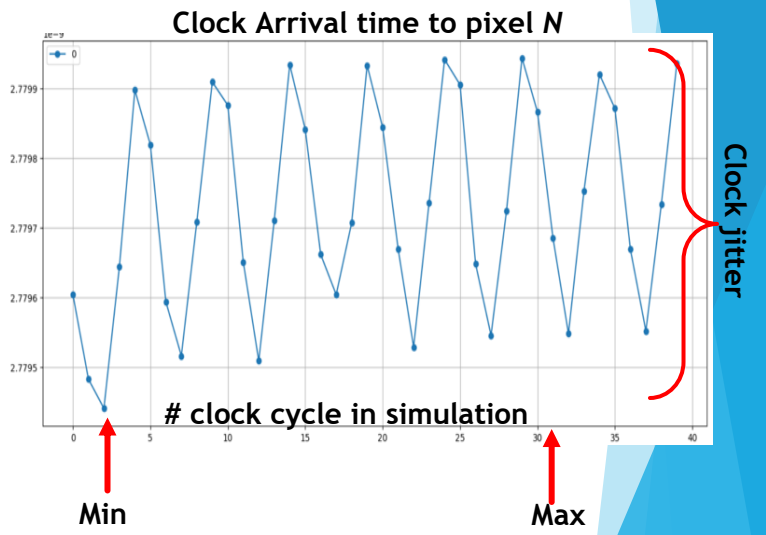
Typ corner, Peak-to-Peak jitter in ns. Worst case per pixel is reported here.

In different pixels, $Max(t_0,..t_N)$ and $Min(t_0,..t_N)$ could be located in different simulation cycles.

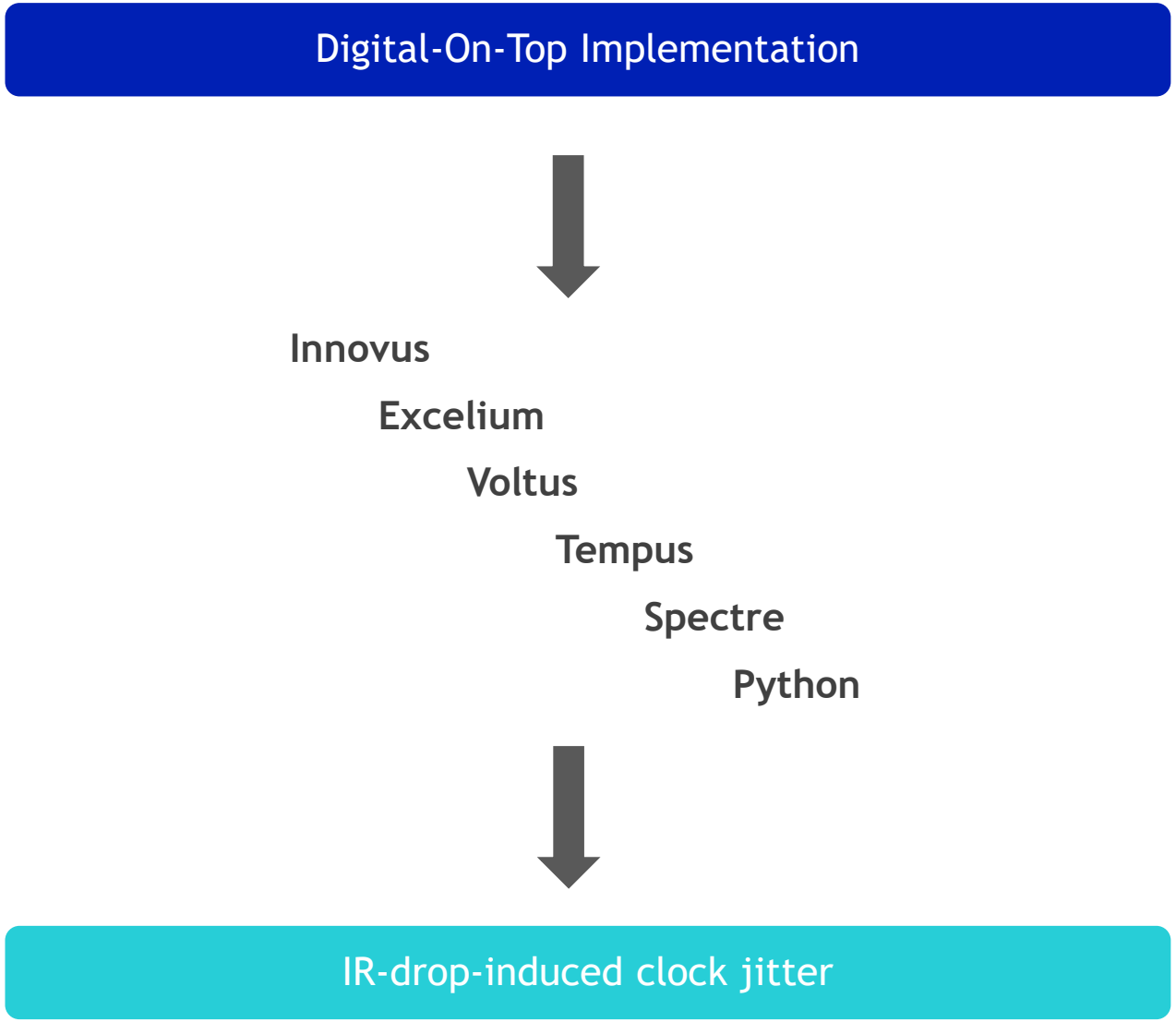
- Ex $Max(t_0,..t_N)$ for Pixel0 in cycle K, $Min(t_0,..t_N)$ in cycle M -> $Jitter_{pix0} = t_K - t_M$
- Ex $Max(t_0,..t_N)$ for Pixel15 in cycle O, $Min(t_0,..t_N)$ in cycle P -> $Jitter_{pix15} = t_O - t_P$







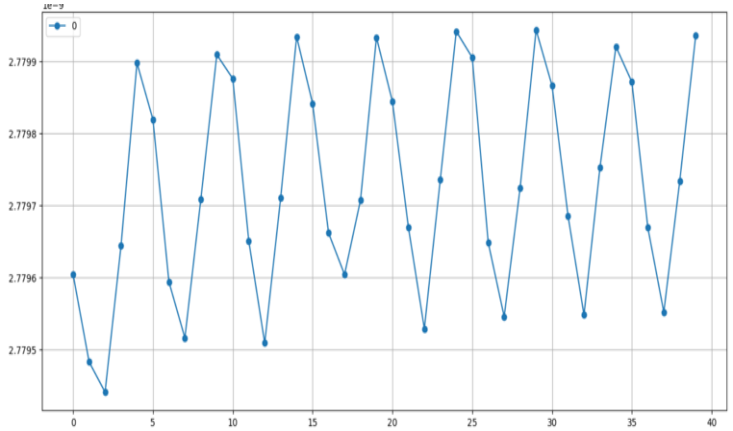
Flow and procedure based on commercial Cadence suite.

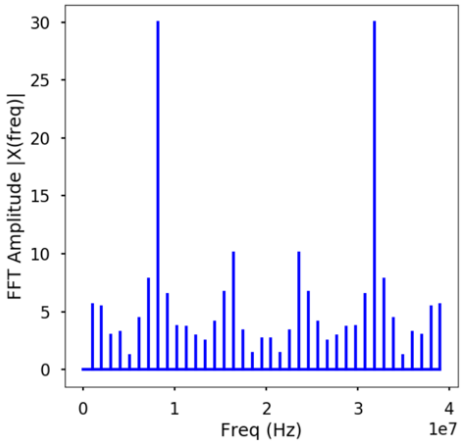


Future perspectives

Possible future developments

- Frequency-domain analysis.





- Package parasitics model: additional drop, resonances,…?