

# A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs.

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### Summary

- Introduction: power supply induced jitter and timing resolution for an ASIC.
- Procedure and simulation steps for deriving IR-drop-induced jitter.
- Practical example: evaluating power-supply induced clock jitter for ALTIROC3 HGTD ASIC.



# Power supply induced jitter

<u>**IR drop**</u> -> voltage drop across the ASIC power grid due to current flowing in it.



- Static: due to average current crossing conductor.
- **Dynamic**: dynamic current drawn by the circuit.

Power supply noise degrades propagation delay and output slope -> <u>jitter</u> (dT).



#### Time Of Arrival (TOA): time elapsed between arrival time of the hit and a reference (ex: ASIC clock)

• Time Over Threshold (TOT): energy measurement.

4D tracking: include timing measurement in tracking.

TDC-based chain:

- 1. Hit is digitalized (analog front-end)
- 2. Time-to-digital converter (TDC) performs conversion

Timing resolution:

•

$$\sigma_{ASIC}^2 = \sigma_{analogFE}^2 + \sigma_{conversion}^2 + \sigma_{clock}^2$$

 $\sigma_{clock}^2$  : generation (PLL, dividers,...) and <u>distribution</u>

4

# High timing precision ASICs - TDC based chain timing resolution



# Timing resolution and power supply induced jitter?

 $\sigma_{clock}^2$  : generation (PLL, dividers,...) and <u>distribution</u>

On-chip clock distribution can be affected by on-chip IR-drop and IR-drop-induced clock jitter.



- What is the impact of on-chip dynamic IR-drop on clock distribution?
- Knowing  $v_n(t)$ , is it possible to know dT for every pixel in the ASIC?

$$\frac{di(t)}{dt} \to v_n(t) \to dT$$



# Flow and procedure based on commercial Cadence suite.





- 1. Fullchip Digital-On-Top design
  - Fullchip design assembled in Cadence Innovus.
  - Analog macro characterized with libfile, abstract and Verilog models.



Output: <u>netlist and SDF for realistic simulation</u>. Corners, typ, min and max.

- 2. Simulation environment to emulate real-life of the ASIC
  - Digital simulation for full-chip verification.
  - Realistic stimuli, ASIC configurations, output bandwidth,...



library (name\_of\_library)
technology ( cmos ) ;

leakage\_power\_unit :

voltage\_unit : "lV" ;
pulling resistance\_uni

delay\_model : tab: date : "date\_of\_creat: revision : revision\_nu time\_unit : "lns" ;

- 3. Dynamic power in Cadence Voltus
  - DoT approach: fullchip analysis
  - Dynamic power analysis extracts <u>current consumption</u> for every cell in design, based on activity information <u>per cycle</u>.





4. Dynamic IR-drop analysis in Cadence Voltus

Dynamic IR drop applies current waveforms to power grid, extracts IR drop for power nets (net-based analysis) and for instances (domain-based analysis).





- 5. Cycle-to-Cycle analog simulation with realistic power supplies.
  - Static Timing Analysis tool (Cadence Tempus) is provided with EIV files and exports the path to be analyzed to analog simulator (Cadence Spectre) via a Spice netlist.
  - One analog simulation for every switching cycle of EIV file, each element annotated with its EIV (EIV1, EIV2,...)
  - Measure rising and falling time through <u>cells and nets.</u>



Output: summing up all the cell and net delays in the path, which now are impacted by IR-drop effect:

Effective Arrival time including IR drop effect, per cycle.



Ir-drop-induced peak-to-peak clock jitter.

 $Peak - To - Peak Jitter = Max(t_0, t_1, t_2, \dots, t_N) - Min(t_0, t_1, t_2, \dots, t_N)$ 





Dedicated presentation: "Verification Environment for ALTIROC ASIC of the ATLAS High Granularity Timing Detector", <a href="https://indico.cern.ch/event/1255624/contributions/5443840">https://indico.cern.ch/event/1255624/contributions/5443840</a>.

- 2x2cm ASIC, 15x15 pixels.
- TOA/TOT measurements, TDC-based chain.
- Measure clock40MHz distributed from periphery to full pixel matrix.  $\pm 150 ps \ skew$ .
- Peripheral wire-bonding for VDD/VSS.
- Increasing IR drop over the matrix.

Study IR-drop-induced jitter in real-life conditions.

- Impinging hits triggers timing measurement and storage.
- Triggered readout activates data transmission.

Varying digital activity inside ASIC -> stability of power grid and jitter of measure clock?

# clock cycle in simulation

#### Simulation scenario

2.004

2.002

2.000

1.998

1.996

1. «IDLE state»: ASIC out of reset, no hits nor triggers (fsm in IDLE state,...). No activity.



$$Peak - To - Peak Jitter = Max(t_0, t_1, t_2, \dots, t_N) - Min(t_0, t_1, t_2, \dots, t_N)$$

	ò	1	2	3	4	5	6	7	8	ģ	10	11	12		5.0120
0 -	0.0005	0.0004	0.0005	0.0006	0.0004	0.0006	0.0007	0.0006	0.0008	0.0007	0.0007	0.0007	0.0007	0.014	0.0126
н -	0.0006	0.0004	0.0003	0.0004	0.0004	0.0003	0.0004	0.0006	0.0007	0.0005	0.0005	0.0005	0.0004	+ - 0.014	0.0126
~ -	0.0006	0.0005	0.0005	0.0006	0.0003	0.0005	0.0006	0.0006	0.0008	0.0006	0.0006	0.0007	0.0006	0.0004	0.0004
m -	0.0003	0.0004	0.0006	0.0005	0.0006	0.0004	0.0005	0.0004	0.0004	0.0006	0.0006	0.0006	0.0006	0.0005	0.0004
4 -	0.0005	0.0004	0.0006	0.0007	0.0006	0.0005	0.0006	0.0006	0.0007	0.0008	0.0008	0.0007	0.0006	0.0006	0.0006
<u>ہ</u>	0.0005	0.0005	0.0006	0.0005	0.0005	0.0003	0.0003	0.0005	0.0005	0.0004	0.0005	0.0005	0.0005	0.0003	0.0004
9 -	0.0005	0.0005	0.0006	0.0004	0.0005	0.0004	0.0004	0.0005	0.0004	0.0005	0.0004	0.0007	0.0006	0.0003	0.0003
2	0.0005	0.0006	0.0005	0.0006	0.0004	0.0006	0.0006	0.0005	0.0008	0.0006	0.0006	0.0007	0.0006	0.0006	0.0006
- 00	0.0005	0.0005	0.0005	0.0006	0.0004	0.0005	0.0007	0.0006	0.0007	0.0006	0.0006	0.0006	0.0006	0.0005	0.0006
ი -	0.0005	0.0005	0.0004	0.0005	0.0004	0.0005	0.0006	0.0005	0.0007	0.0006	0.0006	0.0006	0.0006	0.0005	0.0005
10	0.0005	0.0006	0.0005	0.0006	0.0004	0.0005	0.0006	0.0005	0.0007	0.0006	0.0006	0.0006	0.0006	0.0005	0.0005
11	0.0005	0.0004	0.0008	0.0007	0.0006	0.0008	0.0006	0.0004	0.0005	0.0007	0.0006	0.0009	0.0009	0.0005	0.0005
12	0.0005	0.0005	0.0007	0.0009	0.0006	0.0006	0.0007	0.0004	0.0006	0.0008	0.0008	0.0008	0.0008	0.0006	0.0006
13	0.0005	0.0005	0.0008	0.0007	0.0006	0.0006	0.0006	0.0004	0.0005	0.0006	0.0006	0.0009	0.0009	0.0005	0.0005
14	0.0004	0.0005	0.0007	0.0008	0.0006	0.0006	0.0007	0.0004	0.0007	0.0008	0.0007	0.0007	0.0008	0.0005	0.0006

#### 0.00090 sub-ps

0.00075

- 0.00045

0.0112

0.0113

0.0113

0.0113

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0.0120

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10 -

4 -

m -

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- -

0.0149

0

0 - 0.0149

- 0.00060
- Typ corner (1.2V, typ sdf delays).
- Peak-to-Peak jitter in ns. •
- Worst case per pixel is • reported here.

0.0125

0.0126

0.0128

0.0128

0.0134

0.0135

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11

(CERN) Y
NV

0.0119	0.0131	0.0141	<b>19</b> ps
0.0119	0.0131	0.0141	
0.0121	0.0134	0.0144	- 0.0180
0.0121	0.0135	0.0144	
0.0131	0.0142	0.0152	
0.0130	0.0140	0.0152	- 0.0165
0.0131	0.0141	0.0153	
0.0131	0.0141	0.0153	
0.0131	0.0142	0.0151	- 0.0150
0.0130	0.0141	0.0150	
0.0138	0.0150	0.0160	- 0.0135
0.0142	0.0154	0.0166	
0.0140	0.0153	0.0163	
0.0138	0.0150	0.0158	- 0.0120
0.0136	0.0147	0.0155	
12	13	14	

- Scenario 1) (top) •
  - No hits/triggers •
  - Sub-ps IR-drop-induced jitter
- Full simulation length (right) •
  - Digital activity produces jitter • degradation.

- 14	0.0004	0.0005	0.0007	0.0008	0.0006	0.0006	0.0007	0.0004	0.0007	0.0008	0.0007	0.0007	0.0008	0.0005	0.0006		0.00090	
т 1	0.0005	0.0005	0.0008	0.0007	0.0006	0.0006	0.0006	0.0004	0.0005	0.0006	0.0006	0.0009	0.0009	0.0005	0.0005		sub-p	c
- 13	0.0005	0.0005	0.0007	0.0009	0.0006	0.0006	0.0007	0.0004	0.0006	0.0008	0.0008	0.0008	0.0008	0.0006	0.0006		sup-p	3
= -	0.0005	0.0004	0.0008	0.0007	0.0006	0.0008	0.0006	0.0004	0.0005	0.0007	0.0006	0.0009	0.0009	0.0005	0.0005		0.00075	
9 -	0.0005	0.0006	0.0005	0.0006	0.0004	0.0005	0.0006	0.0005	0.0007	0.0006	0.0006	0.0006	0.0006	0.0005	0.0005		- 0.00075	
ი -	0.0005	0.0005	0.0004	0.0005	0.0004	0.0005	0.0006	0.0005	0.0007	0.0006	0.0006	0.0006	0.0006	0.0005	0.0005			
∞ -	0.0005	0.0005	0.0005	0.0006	0.0004	0.0005	0.0007	0.0006	0.0007	0.0006	0.0006	0.0006	0.0006	0.0005	0.0006			
	0.0005	0.0006	0.0005	0.0006	0.0004	0.0006	0.0006	0.0005	0.0008	0.0006	0.0006	0.0007	0.0006	0.0006	0.0006		- 0.00060	
o -	0.0005	0.0005	0.0006	0.0004	0.0005	0.0004	0.0004	0.0005	0.0004	0.0005	0.0004	0.0007	0.0006	0.0003	0.0003			
<u>ہ</u> -	0.0005	0.0005	0.0006	0.0005	0.0005	0.0003	0.0003	0.0005	0.0005	0.0004	0.0005	0.0005	0.0005	0.0003	0.0004			
4 -																		
m -																		
N -																		
			Why	, doc	arad	atio	n of	cloc	·k ii	ttor	>							
o -		•	vviiy	ues	siau	αιιυ			ון א.									
		•	Whi	ch e	lem	ents	in t	he c	lock	k dis	trib	utio	n to	pixe	el N	suffe	er the	most?



- Sub-ps IR-drop-induced jitter
- Full simulation length (right)
  - Digital activity produces jitter degradation.

														b.	0.0152	- 0.0165
- 00	0.0167	0.0138	0.0130	0.0119	0.0139	0.0145	0.0130	0.0169	0.0135	0.0145	0.0184	0.0138	0.0131	0.0141	0.0153	
r -	0.0167	0.0139	0.0131	0.0119	0.0141	0.0145	0.0130	0.0169	0.0135	0.0146	0.0184	0.0138	0.0131	0.0141	0.0153	
9 -	0.0166	0.0132	0.0131	0.0118	0.0140	0.0138	0.0126	0.0166	0.0133	0.0141	0.0181	0.0133	0.0131	0.0142	0.0151	- 0.0150
·Ω -	0.0168	0.0133	0.0130	0.0117	0.0139	0.0139	0.0125	0.0165	0.0133	0.0141	0.0182	0.0135	0.0130	0.0141	0.0150	
4 -	0.0160	0.0135	0.0136	0.0125	0.0152	0.0138	0.0123	0.0168	0.0137	0.0145	0.0192	0.0135	0.0138	0.0150	0.0160	- 0.0135
m -	0.0158	0.0138	0.0138	0.0129	0.0155	0.0138	0.0123	0.0168	0.0138	0.0145	0.0193	0.0135	0.0142	0.0154	0.0166	
~ -	0.0154	0.0139	0.0137	0.0127	0.0155	0.0139	0.0123	0.0167	0.0137	0.0148	0.0193	0.0134	0.0140	0.0153	0.0163	
	0.0149	0.0136	0.0137	0.0123	0.0152	0.0134	0.0120	0.0163	0.0135	0.0142	0.0186	0.0131	0.0138	0.0150	0.0158	- 0.0120
0 -	0.0149	0.0132	0.0138	0.0121	0.0151	0.0131	0.0119	0.0164	0.0135	0.0140	0.0182	0.0129	0.0136	0.0147	0.0155	
	ò	i	ż	3	4	5	6	7	8	9	10	ú	12	13	14	

Typ corner (1.2V, typ sdf

Peak-to-Peak jitter in ns.

Worst case <u>per pixel</u> is

reported here.

delays).

•

•



0.0141

0.0141

0.0144

0.0144

**19ps** 

- 0.0180



### Jitter degradation of clock to Pixel N

Clock distribution to pixel N



# Single pixel jitter degradation study

# Conclusions

Jitter analysis methodology allows deriving **realistic delays inside ASIC considering IR-drop effects** 

• High-Resolution timing ASICs.

... whatever application where jitter is important (ex: PLL, High-speed circuits.).





# Questions?



# Backup

# Clock arrival time 2<sup>nd</sup> scenario for 15 pixels in a column.





# Min and Max corners

							Mi	n cor	ner	jitte	er (ns	5)																
1       0.0157       0.0171       0.0153       0.0141       0.0136       0.0151       0.0139       0.0142       0.0147       0.0140       0.0158       0.0168       0.0143       0.0148       0.0157																												
- 13	0.0158	0.0172	0.0155	0.0141	0.0137	0.0152	0.0140	0.0142	0.0147	0.0140	0.0158	0.0168	0.0144	0.0149	0.0158													
12	0.0161	0.0174	0.0155	0.0144	0.0141	0.0154	0.0143	0.0145	0.0149	0.0142	0.0161	0.0170	0.0147	0.0151	0.0161													
11	0.0161	0.0175	0.0155	0.0144	0.0141	0.0154	0.0142	0.0146	0.0149	0.0142	0.0161	0.0170	0.0146	0.0152	0.0162			17										
10	0.0170	0.0182	0.0164	0.0147	0.0146	0.0160	0.0148	0.0153	0.0157	0.0148	0.0165	0.0172	0.0151	0.0155	0.0169		- 0.0	17										
ი -	0.0170	0.0182	0.0164	0.0147	0.0146	0.0161	0.0149	0.0153	0.0158	0.0148	0.0166	0.0172	0.0151	0.0155	0.0169													
- 00	0.0171	0.0183	0.0165	0.0147	0.0146	0.0161	0.0148	0.0153	0.0158	0.0148	0.0165	0.0172	0.0151	0.0156	0.0171				Ma	ах со	rner	jitte	r (ns	;)				
L -	0.0171	0.0183	0.0165	0.0148	0.0146	0.0161	0.0148	0.0153	0. 17 -	0.0144	0.0139	0.0132	0.0120	0.0130	0.0133	0.0135	0.0163	0.0142	0.0150	0.0175	0.0151	0.0134	0.0133	0.0146				
9 -	0.0167	0.0181	0.0162	0.0147	0.0145	0.0159	0.0143	0.0148	о. <u>т</u> -	0.0143	0.0140	0.0133	0.0121	0.0131	0.0133	0.0139	0.0164	0.0142	0.0149	0.0174	0.0151	0.0134	0.0134	0.0148				
- <u>م</u>	0.0166	0.0180	0.0161	0.0146	0.0145	0.0158	0.0144	0.0149	0. <u>21</u> -	0.0146	0.0141	0.0135	0.0121	0.0134	0.0136	0.0145	0.0168	0.0147	0.0153	0.0171	0.0154	0.0137	0.0139	0.0149				
4 -	0.0164	0.0176	0.0160	0.0147	0.0139	0.0153	0.0140	0.0145	₀. ᇊ-	0.0146	0.0142	0.0135	0.0122	0.0132	0.0137	0.0144	0.0170	0.0149	0.0154	0.0169	0.0154	0.0136	0.0139	0.0149				
- Μ	0.0163	0.0177	0.0161	0.0148	0.0140	0.0153	0.0141	0.0145	0. 엵 -	0.0149	0.0143	0.0139	0.0123	0.0138	0.0141	0.0137	0.0179	0.0151	0.0157	0.0176	0.0158	0.0139	0.0140	0.0151				
- 5	0.0161	0.0176	0.0159	0.0147	0.0139	0.0151	0.0140	0.0145	0. თ-	0.0148	0.0143	0.0141	0.0121	0.0140	0.0142	0.0135	0.0181	0.0149	0.0160	0.0176	0.0156	0.0138	0.0137	0.0149				
- 1	0.0158	0.0172	0.0158	0.0145	0.0135	0.0148	0.0135	0.0139	0. ∞ -	0.0147	0.0141	0.0141	0.0123	0.0140	0.0141	0.0135	0.0180	0.0145	0.0155	0.0177	0.0155	0.0138	0.0139	0.0145				
0 -	0.0156	0.0170	0.0155	0.0142	0.0135	0.0145	0.0134	0.0139	0. ト -	0.0146	0.0141	0.0140	0.0122	0.0140	0.0140	0.0135	0.0177	0.0142	0.0153	0.0177	0.0153	0.0137	0.0141	0.0144				
	0	1	2	3	4	5	6	7	- e	0.0142	0.0136	0.0140	0.0115	0.0134	0.0132	0.0133	0.0175	0.0138	0.0149	0.0170	0.0149	0.0133	0.0137	0.0138				
									- n	0.0141	0.0138	0.0141	0.0112	0.0133	0.0130	0.0134	0.0173	0.0136	0.0149	0.0170	0.0150	0.0133	0.0136	0.0136				
									4 -	0.0133	0.0132	0.0138	0.0107	0.0131	0.0116	0.0133	0.0148	0.0133	0.0150	0.0163	0.0141	0.0129	0.0133	0.0135				
									m -	0.0131	0.0131	0.0138	0.0106	0.0129	0.0115	0.0133	0.0146	0.0134	0.0149	0.0164	0.0138	0.0130	0.0133	0.0136				
									- יא	0.0130	0.0132	0.0137	0.0106	0.0125	0.0113	0.0132	0.0145	0.0132	0.0145	0.0162	0.0136	0.0130	0.0133	0.0136				
									- 1-	0.0127	0.0128	0.0132	0.0102	0.0121	0.0110	0.0126	0.0139	0.0130	0.0142	0.0156	0.0133	0.0129	0.0132	0.0135				
									o -	0.0125	0.0125	0.0129	0.0102	0.0119	0.0110	0.0124	0.0138	0.0129	0.0140	0.0155	0.0131	0.0128	0.0131	0.0133				

1 2 3

4 5

6

7

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CERN

- 0.0180

- 0.0165

- 0.0150

- 0.0135

- 0.0120

12

13

14

10

9

8

11

- 0.0105 21

# Single pixel jitter degradation study in 3 corners

EIV and jitter degradation of clock path to pixel 0 in 3 different corners.







# Voltage degradation





# **CLOCK DIGITAL**

### TYP jitter (ns)

14	0.0107	0.0093	0.0093	0.0090	0.0086	0.0085	0.0102	0.0108	0.0097	0.0103	0.0122	0.0104	0.0		0.0109	0.0122
- 13	0.0108	0.0094	0.0090	0.0087	0.0085	0.0083	0.0101	0.0107	0.0098	0.0102	0.0118	0.0100	0.0	091	0.0109	0.0120
- 12	0.0104	0.0091	0.0088	0.0084	0.0082	0.0080	0.0097	0.0103	0.0095	0.0100	0.0115	0.0097	0.0	089	0.0106	0.0117
11 -	0.0099	0.0089	0.0082	0.0084	0.0080	0.0075	0.0094	0.0098	0.0092	0.0096	0.0113	0.0096	0.0	086	0.0104	0.0113
10	0.0095	0.0085	0.0078	0.0081	0.0077	0.0072	0.0091	0.0094	0.0089	0.0093	0.0108	0.0093	0.0	082	0.0101	0.0109
ი -	0.0090	0.0082	0.0075	0.0079	0.0075	0.0070	0.0086	0.0091	0.0085	0.0090	0.0104	0.0090	0.0	080	0.0098	0.0106
- 00	0.0085	0.0079	0.0073	0.0076	0.0072	0.0067	0.0083	0.0087	0.0082	0.0086	0.0100	0.0087	0.0	078	0.0094	0.0102
r -	0.0081	0.0075	0.0071	0.0074	0.0069	0.0065	0.0079	0.0082	0.0079	0.0083	0.0095	0.0084	0.0	076	0.0091	0.0098
- ص	0.0078	0.0071	0.0068	0.0071	0.0065	0.0063	0.0075	0.0079	0.0075	0.0080	0.0090	0.0080	0.0	074	0.0087	0.0093
- <u>م</u>	0.0074	0.0067	0.0065	0.0068	0.0062	0.0060	0.0071	0.0073	0.0072	0.0076	0.0086	0.0077	0.(		3 4 4 3 1	3 3693
4 -	0.0071	0.0063	0.0062	0.0065	0.0059	0.0059	0.0067	0.0068	0.0068	0.0072	0.0080	0.0073	0.(	- 14 14	3.3753	3.3006
m -	0.0069	0.0061	0.0060	0.0062	0.0057	0.0056	0.0063	0.0063	0.0064	0.0068	0.0075	0.0069	0.(	- 2	3.2832	3.2089
~ -	0.0065	0.0058	0.0058	0.0059	0.0055	0.0054	0.0059	0.0058	0.0059	0.0065	0.0069	0.0065	0.(	1-	3.1758	3.1015
- H	0.0062	0.0056	0.0055	0.0057	0.0053	0.0052	0.0056	0.0053	0.0056	0.0059	0.0064	0.0061	0.(	01 -	3.0819	3.0076
0 -	0.0058	0.0054	0.0054	0.0054	0.0051	0.0050	0.0052	0.0049	0.0052	0.0056	0.0059	0.0058	0.(	<b>თ</b> -	2.9873	2.9130
	ò	i	2	3	4	5	6	7	8	9	10	11		00 -	2.8919	2.8175
															2.7947	2.7196
														9 -	2.6964	2.6206
														- <u>م</u>		2.5224

# Skewed clock (very different from clock 40MHz measurement)

- 0.0105

- 0.0120

- 0.0090

### TYP insertion delay (ns)

14	3.4431	3.3693	3.2661	3.1609	3.0561	2.9520	2.8460	2.6898	2.7917	2.8968	3.0003	3.1035	3.2046	3.3058	3.3794
13	3.3753	3.3006	3.1974	3.0922	2.9873	2.8833	2.7772	2.6211	2.7230	2.8280	2.9315	3.0347	3.1359	3.2370	3.3106
12	3.2832	3.2089	3.1057	3.0004	2.8956	2.7915	2.6855	2.5293	2.6313	2.7363	2.8398	2.9430	3.0442	3.1454	3.2189
11	3.1758	3.1015	2.9984	2.8932	2.7883	2.6842	2.5782	2.4220	2.5240	2.6290	2.7324	2.8356	2.9368	3.0380	3.1115
10	3.0819	3.0076	2.9044	2.7992	2.6943	2.5902	2.4842	2.3280	2.4300	2.5350	2.6385	2.7416	2.8428	2.9440	3.0176
ი -	2.9873	2.9130	2.8098	2.7045	2.5997	2.4956	2.3896	2.2334	2.3353	2.4403	2.5440	2.6470	2.7482	2.8493	2.9229
∞ -	2.8919	2.8175	2.7144	2.6091	2.5042	2.4001	2.2941	2.1380	2.2399	2.3449	2.4485	2.5516	2.6528	2.7539	2.8275
	2.7947	2.7196	2.6164	2.5112	2.4063	2.3023	2.1962	2.0401	2.1420	2.2470	2.3506	2.4537	2.5548	2.6560	2.7296
9 -	2.6964	2.6206	2.5174	2.4122	2.3073	2.2032	2.0972	1.9410	2.0430	2.1480	2.2516	2.3546	2.4558	2.5570	2.6306
∽ -	2.5988	2.5224	2.4193	2.3141	2.2092	2.1051	1.9990	1.8429	1.9448	2.0499	2.1534	2.2565	2.3577	2.4589	2.5324
4 -	2.5005	2.4237	2.3205	2.2153	2.1105	2.0064	1.9003	1.7442	1.8461	1.9511	2.0547	2.1578	2.2590	2.3601	2.4337
m -	2.4015	2.3242	2.2210	2.1158	2.0109	1.9068	1.8008	1.6446	1.7466	1.8516	1.9552	2.0583	2.1595	2.2606	2.3342
~ -	2.3039	2.2261	2.1229	2.0177	1.9129	1.8088	1.7027	1.5466	1.6485	1.7536	1.8572	1.9602	2.0615	2.1626	2.2361
	2.2041	2.1258	2.0227	1.9174	1.8126	1.7085	1.6025	1.4463	1.5482	1.6532	1.7569	1.8599	1.9611	2.0623	2.1359
o -	2.1048	2.0263	1.9231	1.8179	1.7130	1.6090	1.5029	1.3467	1.4487	1.5537	1.6573	1.7603	1.8616	1.9627	2.0362
	ò	i	2	3	4	5	6	ż	8	9	10	11	12	13	14



- 3.2

- 2.8

- 2.4

- 2.0

- 1.6

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- 3. Dynamic power in Cadence Voltus
  - DoT approach: fullchip analysis
    - Power Grid Libraries needed for analog macros (capacitance, current distribution).



• Dynamic power analysis extracts <u>current consumption</u> per cell based on activity information per cycle.





# Single pixel jitter degradation study





# Single pixel jitter degradation study



### ALTIROC3 study. Scenario 1) results (No activity)

Typ corner, Peak-to-Peak jitter in ns. Worst case per pixel is reported here.

In different pixels,  $Max(t_0, ..., t_N)$  and  $Min(t_0, ..., t_N)$  could be located in different simulation cycles.

- Ex  $Max(t_0, ..., t_N)$  for Pixel0 in cycle K,  $Min(t_0, ..., t_N)$  in cycle M -> Jitter  $_{pix0} = t_K t_M$
- Ex  $Max(t_0, ..., t_N)$  for Pixel15 in cycle O,  $Min(t_0, ..., t_N)$  in cycle P -> Jitter  $_{pix15} = t_0 t_P$





# Flow and procedure based on commercial Cadence suite.





# Future perspectives

### Possible future developments

• Frequency-domain analysis.







