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A simulation methodology for establishing IR-drop-induced clock jitter for high precision timing ASICs.

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The combination of 3D tracking and high-precision timing measurements has been identified by the European Committee for Future Accelerators as a fundamental requirement to increase detection capabilities for future applications. Among others, on-chip high-quality clock is a key factor determining the overall resolution of Timing ASICs. However, in large and dense chips, power-grid drops can severely affect the non-deterministic jitter of the clock, representing a limit to the performances. This contribution aims at presenting a simulation framework based on commercial tools to evaluate power supply-induced jitter, providing a pre-silicon methodology to assess its impact on timing indeterminism.

Summary (500 words)

The European Committee for Future Accelerators (ECFA) has identified high precision timing measurement as a critical research area for future accelerators. To address the challenges posed by increased luminosity and large particle track pile-up, the use of "4D techniques", which involve 3D tracking and Time of Arrival evaluation, is essential for improving vertex location in future High-Energy particle detectors.
High-performance sampling and high precision timing distribution are essential elements to be considered when dealing with resolutions on the order of tens of picoseconds. In this context, the classical approach of TDC-based chains is highly dependent on the quality of the reference clock distributed on ASIC to each measurement channel. The continuous scaling and integration of VLSI technology pose a severe limitation to the quality of the clock due to the phenomenon of power supply-induced jitter: the dynamic iR drop generated by the running logic reflects into a non-deterministic transition time of the CMOS logic, and eventually to an uncertainty in the time of arrival of the reference clock. Large Pixel ASICs are more sensitive to this phenomenon due to the commonly known limitations of power PADs position, area, and routing resources availability.
A simulation-based methodology exploiting commercial tools has been developed to correlate the ASIC activity with the induced clock jitter, to derive the non-deterministic components to be added as uncertainty in the measured value.
First, the digital-on-top design is simulated with digital tools and different stimuli, ranging from low activity (similar to an idle state) to high activity. The extracted activity information is then used to perform dynamic power and iR drop analysis, where the effective instance voltage (EIV), calculated as the difference between the supply and ground seen by the clock buffers, is derived and recorded at every cycle. Analog simulators are then used to simulate the extracted clock network together with the EIV values annotated per each cell, allowing to derive the real arrival time of the clock to all the sinks for every cycle. Finally, the contribution to the non-deterministic part of the jitter can be calculated identifying the two cycles with maximum difference in clock arrival time.
The proposed methodology provides the designer with a powerful tool to estimate the power supply induced jitter on clock trees, showing the effect of ASIC activity into the real arrival timing of the reference clock, allowing also further optimizations before tapeout. The technique will be shown together with its application

to the Altiroc3 ASIC, where the results clearly reflect the internal floorplan and power distribution characteristics.

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