Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology

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On behalf of the IGNITE collaboration

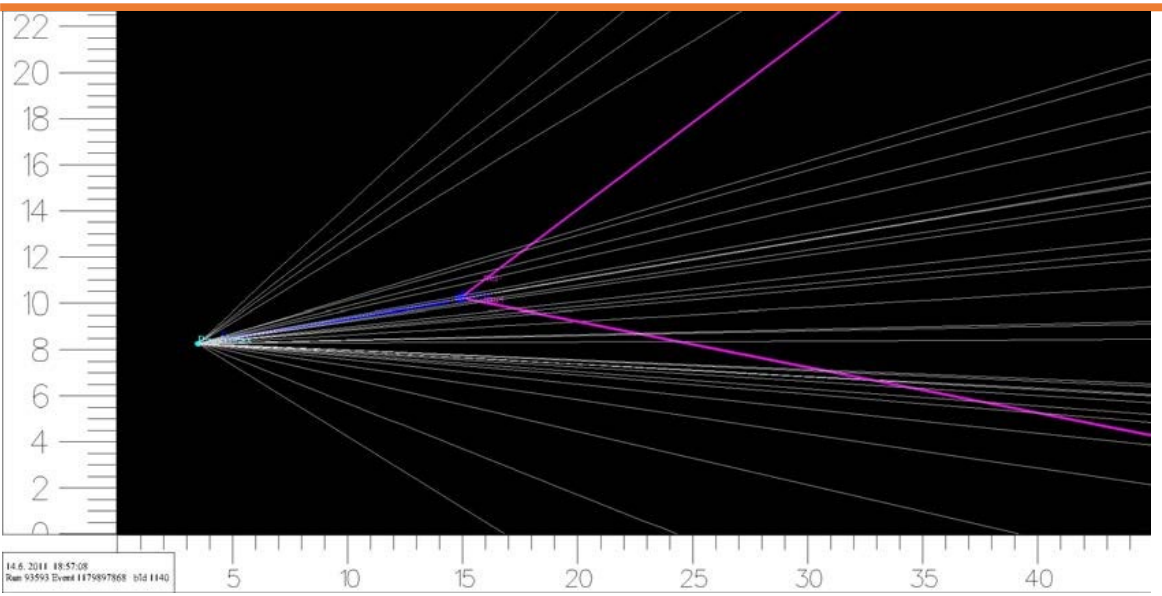
IGNITEd

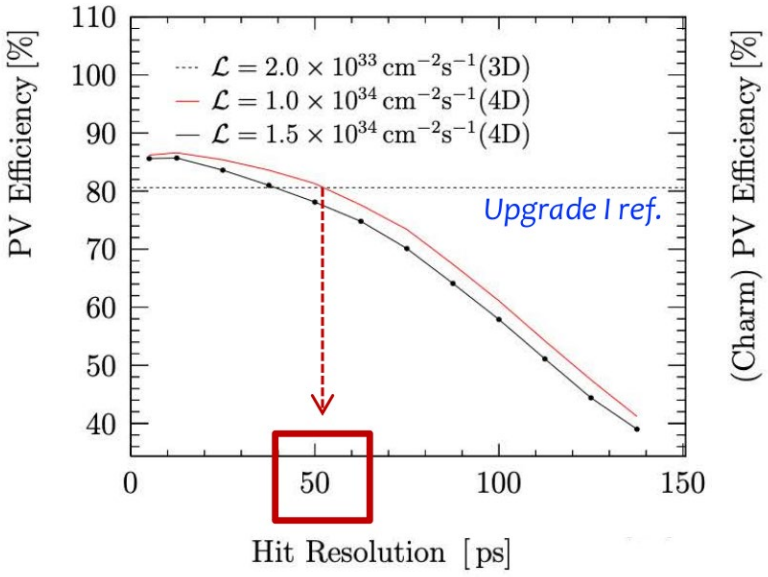
INFN

Istituto Nazionale di Fisica Nucleare

INFN Ground-up iNITiative for µElectronics developments

4D Tracking: reasons and requirements





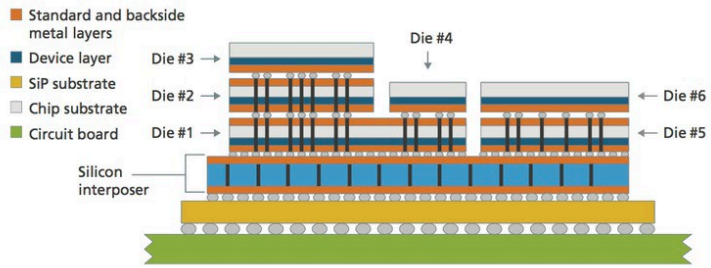
Plot from:
Considerations for the VELO detector at the LHCb Upgrade II
{CERN-LHCb-2022-001}

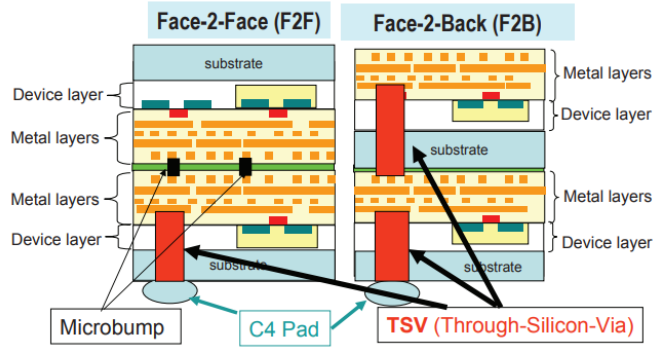
- 4D tracking: adding the time information at pixel level to conventional tracking.
- Helps to mitigate pile-up.
- Better discrimination of closely spaced tracks
  - avoid bad primary vertex reconstruction increasing reconstruction efficiency.

- Spatial resolution: ~ 10 µm rms.
- Timing resolution: < 50 ps rms comprising all contributions:
  - $\sigma_t = \sqrt{\sigma_{sens}^2 + \sigma_{afe}^2 + \sigma_{tdc}^2 + \sigma_{clk}^2}$
- Radiation hardness: high fluences $10^{16}\,\frac{MeVn_{eq}}{cm^2}$ to $10^{17}\,\frac{MeVn_{eq}}{cm^2}$
- Detection efficiency > 99 %.
- Material budget < 0.5% radiation length per layer.
- Power budget of 1.5 $\frac{W}{cm^2}$ (~ 25 µW/pixel with a 50 µm pitch).
- Data bandwidth ~100 $\frac{Gbps}{cm^2}$.

The IGNITE project

- A national initiative funded by INFN.
  - 14 INFN institutes
  - 70 people (physicist and engineers), 20 FTE
  - P.I. Adriano Lai (INFN Cagliari).
- Develop a 4D tracking system suitable for high-luminosity environments
  - integrated system composed by hybrid 28 nm pixel front-end ASIC, and a readout ASIC for high-bandwidth optical data transmission.
  - Use the TimeSPOT developments as the basis for the building blocks of the system.
- Challenges:
  - Obtain uniform sub 50 ps rms time resolution for all pixel matrix
  - Minimize power consumption and data throughput.
  - Deliver stable power to the pixels in a large-scale matrix.
  - Distribute data from the matrix to the read-out.
- Explore innovative 3D integration technologies

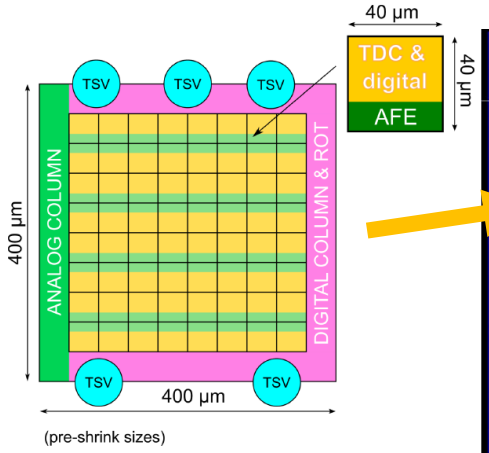




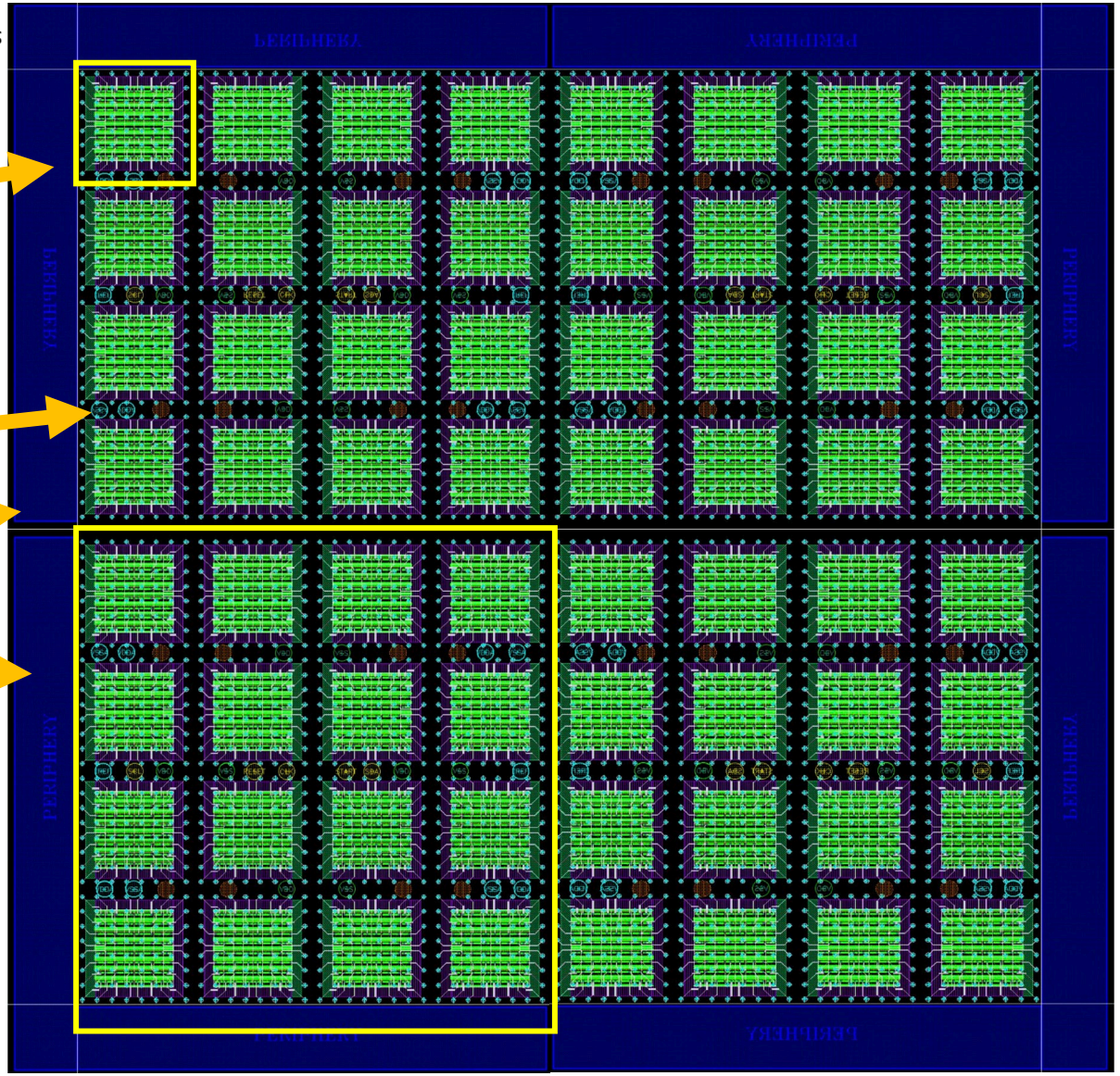
- 3D integrated circuits:
  - built by vertically stacking different chips together into a single package
  - The IC coupling is based on two consolidated technologies: TSV, Face2Back and Face2Face bonding.
- Enables the "Tiling" of the active area without inactive area due to wire-bonding.
- It is possible to separate the different stages and functions on multiple layers/ICs.
  - Optimal separation between analog and digital domains
  - More room for analog processing facilities
  - More room for digital processing facilities, giving the possibility to integrate further functionalities on groups of pixels (e.g. clustering and hit pre-processing)

IGNITE 4D ASIC

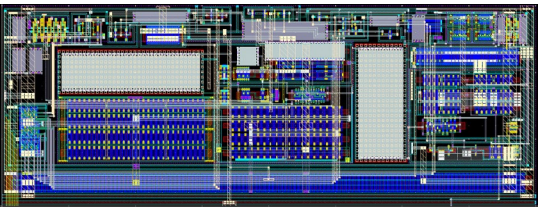
- Basic Tile Structure:
  - 8x8 pixels Tile
  - AFE + TDC for each pixel
  - Service spaces surrounding the tile for Analog and Digital services/power.

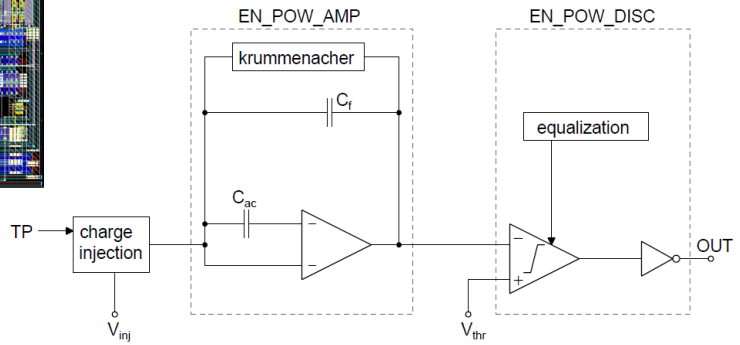


- Empty spaces between tiles
  - Can be used to place TSV
- Contacts are replicated on periphery
- 32x32 channels Tile is abuttable on 2 sides
  - The transition from the elementary 32x32 module to extended 64x64 ASIC is just by abutting.
- Completely independent tile when TSV are used: great advantage for implementation and verification procedures
- With this approach it is possible to read sensors with different pitches using the same pixel design
  - We can adjust the spaces between tiles and modify the RDL.

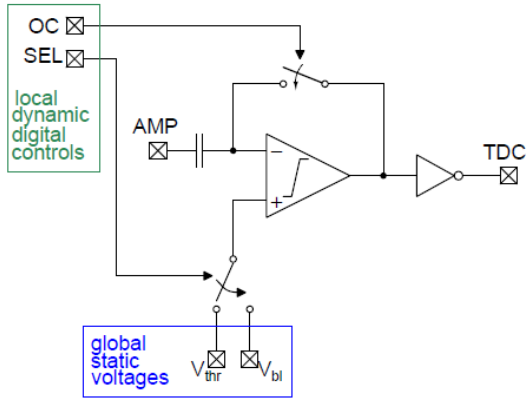


IGNITE: AFE

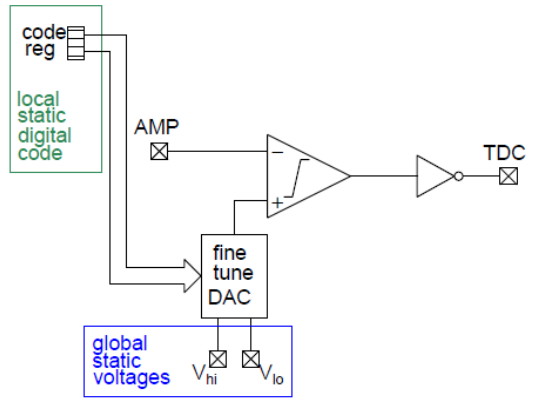




- Area: 36 µm x 13.5 µm.
- Different "solutions" (all geometrically and electrically compatible):
  - CSA: inverter-based core amplifier, Krummenacher feedback.
  - The Preamplifier and Discriminator can be switched-off independently per channel
  - Preamplifier:
    - two Charge Sensitive Amplifier (CSA), cascoded (CAS) and not cascoded (noCAS).
  - Discriminator:
    - one with discrete time Offset Compensation (OC),
    - one with a Fine-Tune DAC (FT).
- Local charge injection circuit.
- Programmable power: 4 µW -> 21 µW
  - Nominal : 10.8 µW per channel.

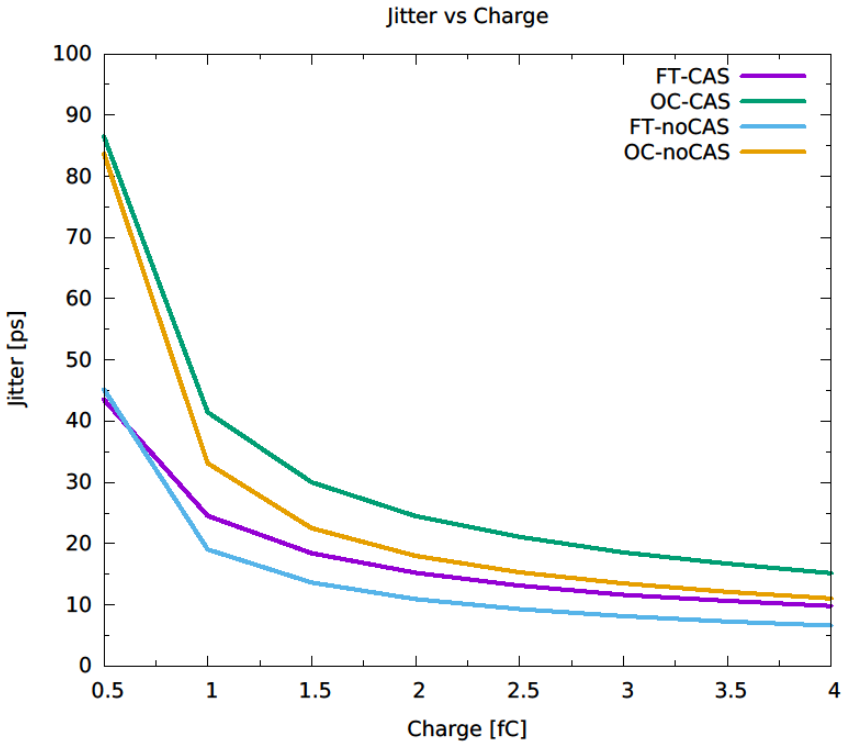


- The circuit autocorrect its offset while saving the desired baseline on a capacitor.
  - \+ Requires two global voltages.
  - \+ Works with local digital controls.
  - \+ Self calibrating.
  - \- The procedure must be strobed.
  - \- It must be repeated periodically, introducing some dead time.
  - \- Increases the jitter by a factor $\sqrt{2}$.
  - \- The parasitic of the capacitor loads the preamplifier.

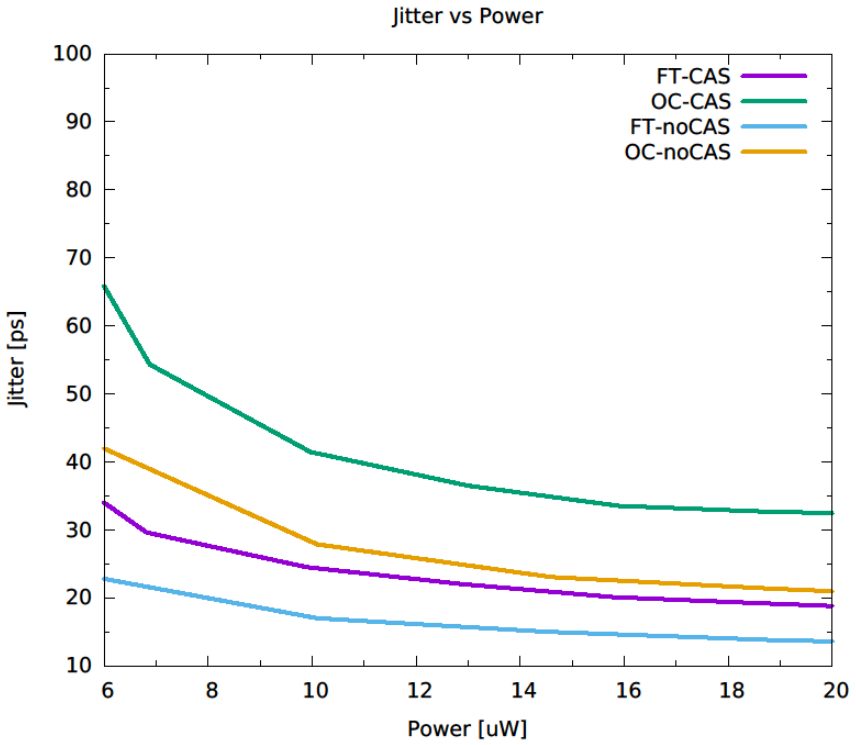


- The threshold is calibrated for each channel to compensate the offset.
  - \+ Requires: two global voltages, local digital code.
  - \+ The calibration is static.
  - \+ No added component to the jitter.
  - \+ No additional loading to the preamplifier.
  - \- Requires registers to save the calibration..
  - \- Requires a calibration procedure with error measurement.

IGNITE: AFE Jitter



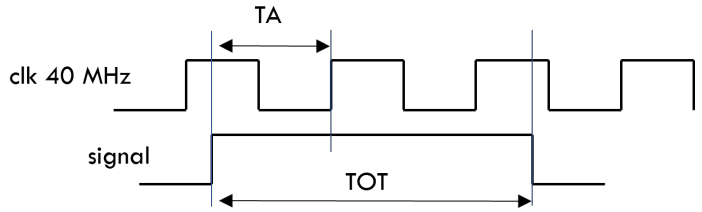
Post-Layout Simulations



- (Power = 10.8 µW, C_{in} = 100 fF).
- MIP 2 fC, lowest value 1 fC but charge sharing can decrease the MPV and the lowest value -> also it varies with sensor geometry.
- The OC has a "cost on power".
- The CAS core is sensitive to output loading.

- (q_{in} = 1 fC, C_{in} = 100 fF).
- Pre-Amp and Discriminator power varied to maintain performance.
- Nominal performance close to saturation. Can still be tuned-up.
- Some CSA exhibits good performance at sub-nominal power.

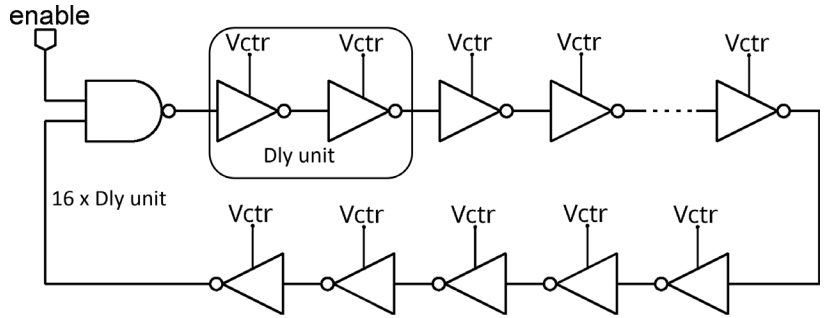
IGNITE: TDC overview



- TDC requirement
  - Time of Arrival (TA):
    - $\sigma_{overall} \approx 30$ ps overall (AFE + TDC)
    - $\sigma_{TDC} \leq 15$ ps
    - TDC LSB < 50 ps
  - Time Over Threshold:
    - LSB around 1ns or less
    - Max TOT < 200 ns
    - 8 bits

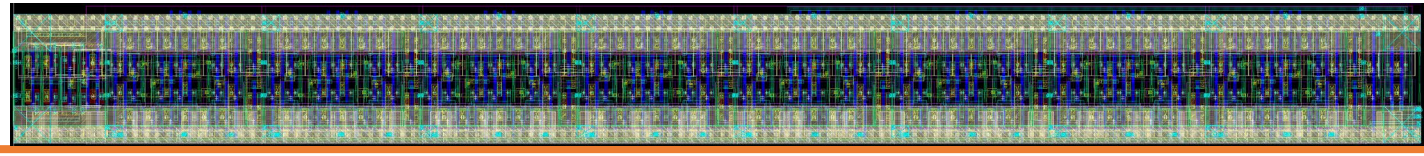
- Vernier Architecture (Evolution of Timespot TDC)
  - DCOs Frequency: ~ 1GHz
  - DCO's switched off after meas
  - The resolution does not depend on the periods but on their difference
  - Max conversion time depends on DCO Periods: Larger periods mean larger conversion time

DCO



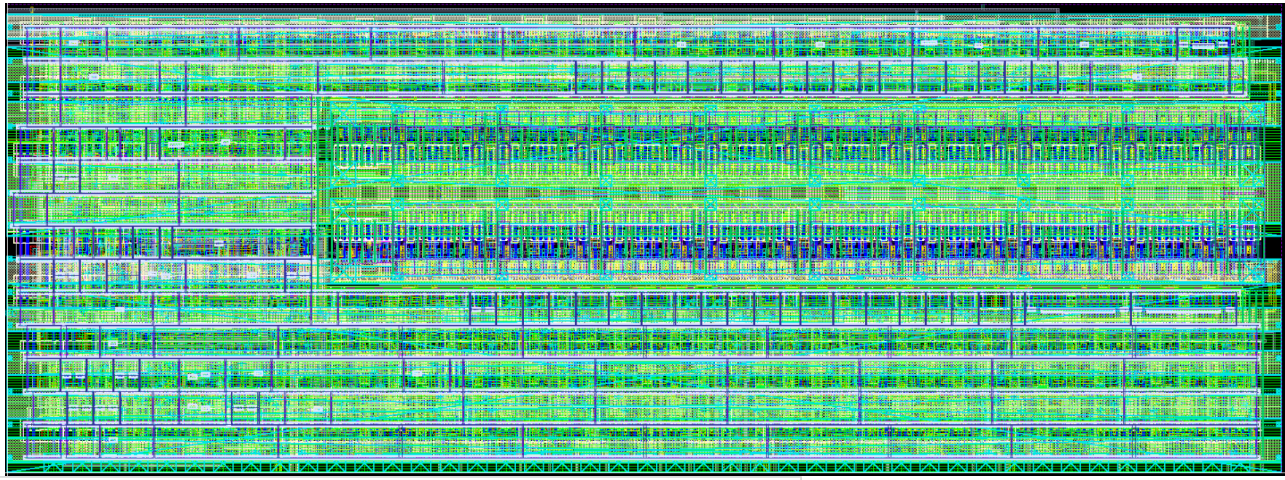
- **Size:** 19.78 x 1.94 um^2
- **Number of Steps:** 16 Delay Units
  - Single delay cell with starved architecture
  - Power on/off configuration – fine tuning – coarse tuning
  - Decoupling capacitors
- **Step controls:** Fine ≈ 3 ps – Coarse ≈ 50 ps
- **Period Range:** ~ 900 ps – 780 ps (Typ Post-Layout)
- **Power Cons.:** ~ 45 µA – 55 µA (Typ Post-Layout)
- **Jitter:** ~ 750 fs – 600 fs (Typ Post-Layout)

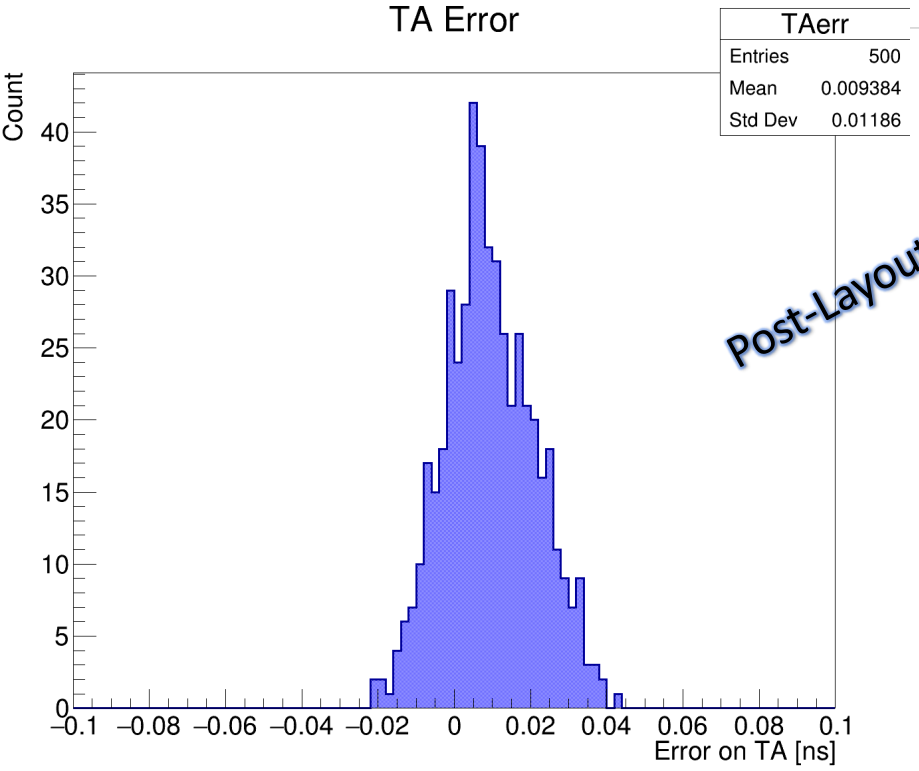
DCO layout: 19.78 x 1.94 um^2



IGNITE TDC: layout

- Particular care for power distribution as well as 40 MHz master clock distribution
- Size: 27 x 9.9 μm^2
- DCO Jitter < 1 ps
- TDC resolution from simulation: ~ 12 ps





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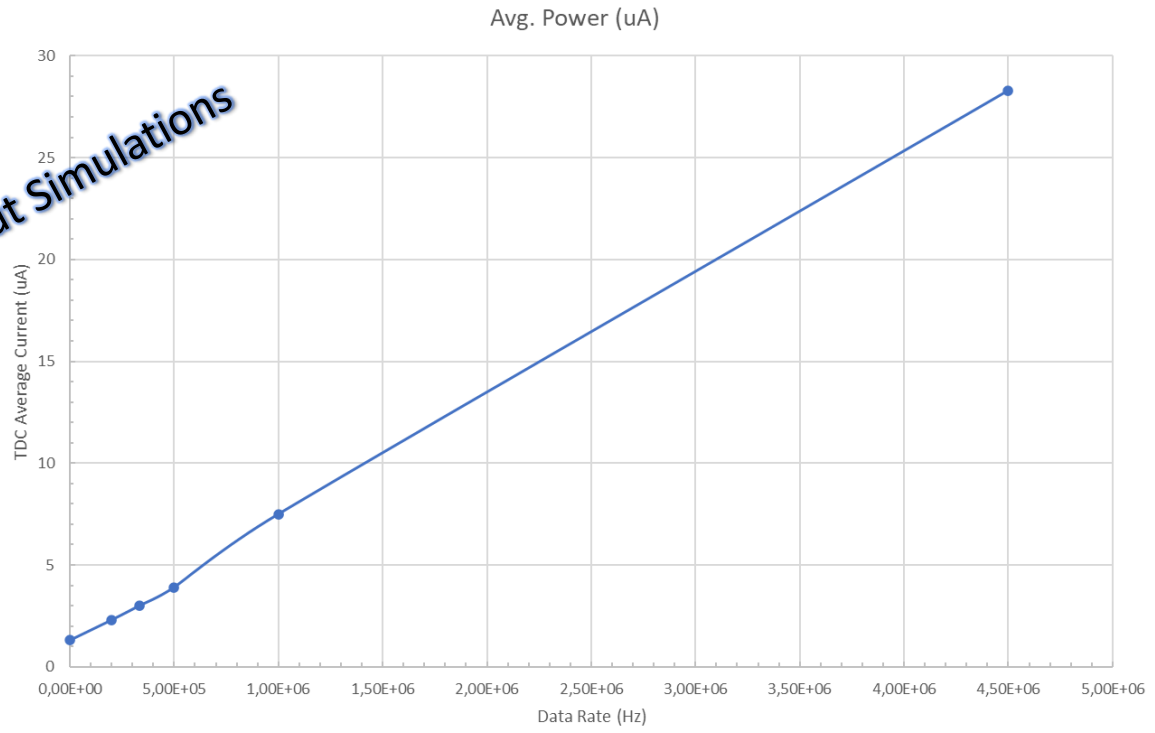


IGNITE TDC Power Cons.

TDC status	Current
OFF	0.5 µA
IDLE	1.3 µA
Calib. DCO {Istant. @1.12 GHz}	98 µA
RUN (4.5 MHz)	28.3 µA
RUN (1.0 MHz)	7.5 µA
RUN (500 kHz)	3.9 µA
RUN (333 kHz)	3.0 µA
RUN (200 kHz)	2.3 µA

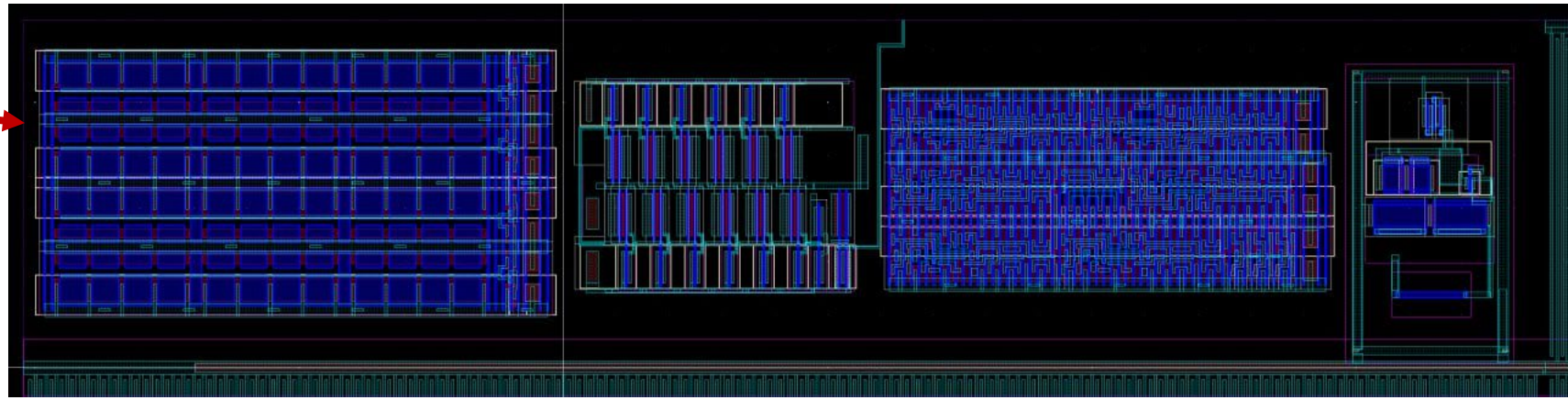
Timespot TDC Power Cons.

TDC power	µW
IDLE	20.7
Calibration	552
DAQ 3 MHz	175
DAQ 1 MHz	69.3
DAQ 500 kHz	45.5
DAQ 100 kHz	25.7

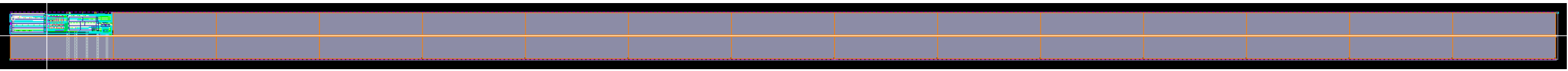
IGNITE PLL

- The PLL (Phase Locked Loop) has been designed to provide an internal reference clock with a locked phase with respect to an external one
- It can average the jitter on several edges of the input clock to produce a low-jitter reference
  - The average is done by means a large filter capacitor
- Based on a starved DCO
  - Three starving schemes: static, DAC and external
- Lock frequency 40MHz , power consumption ~50 µW, jitter filtering from 14 ps (input) to 1.6 -1.9 ps (output) depending on the starving scheme

- Core area: 30 x 6 μm^2



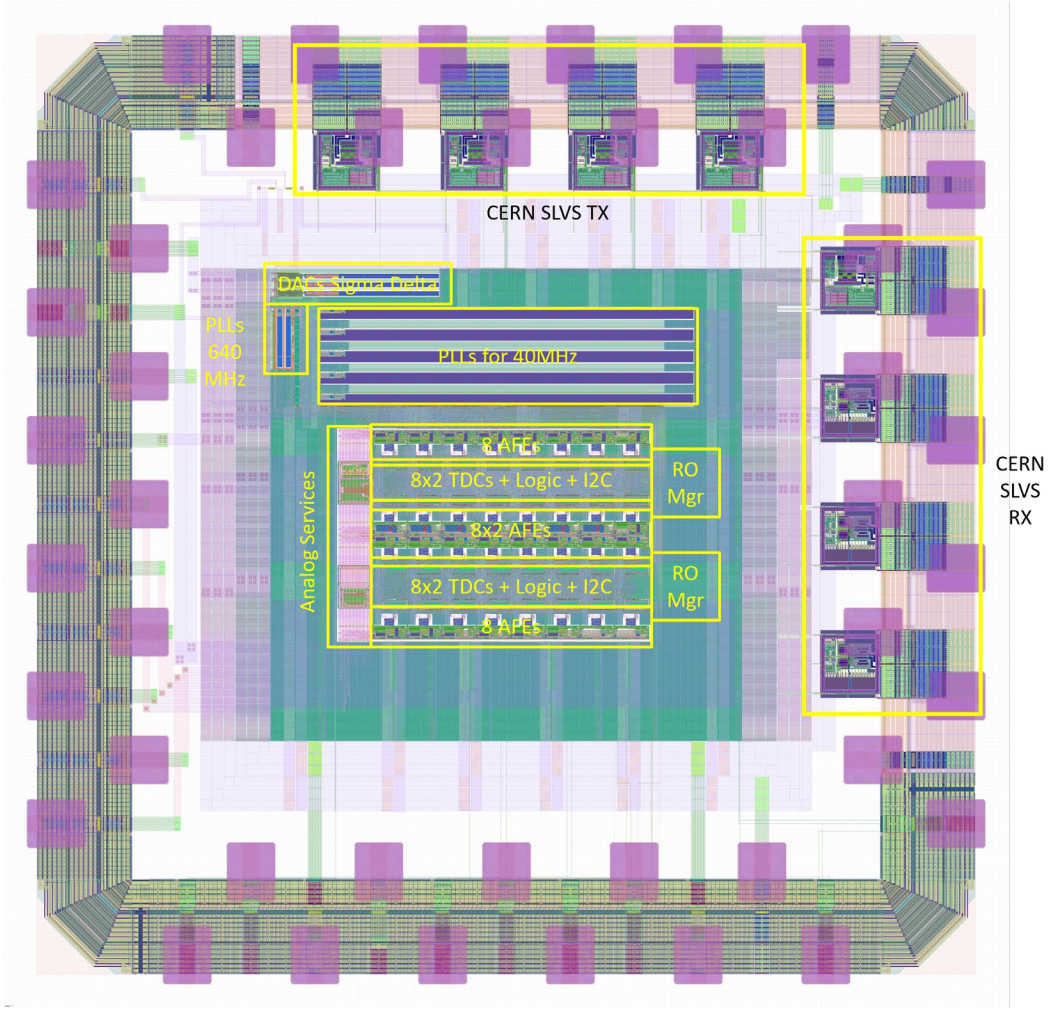
- With filter 433 x 15.6 μm^2
  - optimized for integration in the periphery



IGNITE: IGNITE0 mini@sic for testing

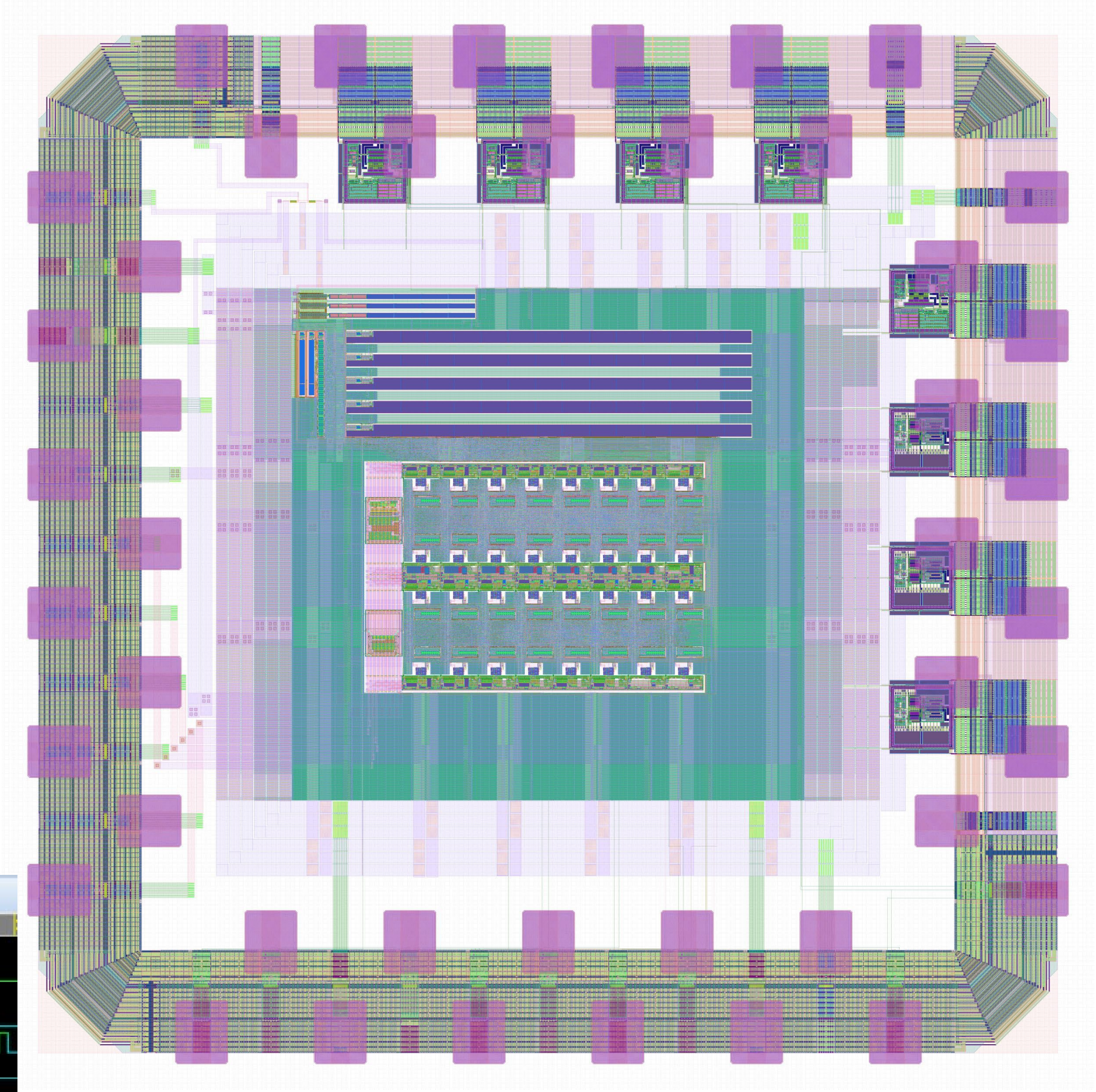
- IGNITE0 submitted in July ‘23 and expected in November ‘23.
  - An “half tile” 8x4 pixel (AFE + TDC)
    - Some extra spaces was added between TDC and AFE for extra test structures
  - 32 TDCs grouped in two 8x2 blocks
  - 32 AFE cells in different flavors
  - PLLs for clock generation/filtering (40 MHz and 640 MHz) with jitter lower than 4ps
  - DACs
  - Readout Managers
  - I2C interfaces for ECS controls and configurations

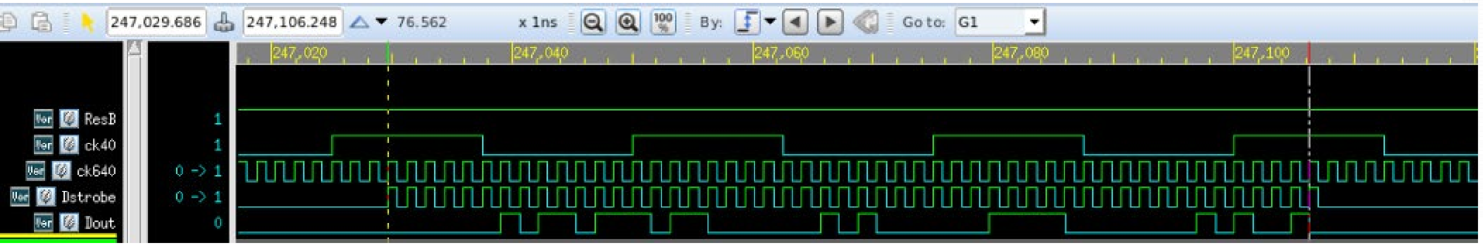
  - Several logic blocks that allow us to test each individual block in standalone mode as well as together with other connected functional blocks (e.g., AFE and TDC)



IGNITE: IGNITE0 mini@sic for testing

- Readout system
  - One 16-word depth FIFO for each block 8x2 (16 channels)
  - Each event is a 49-bit word and includes all the info (Vernier Counters, TOT, Coarse TimeStamp/Bxid, Event type, pixel Address, FIFO Status)
  - The data frame is not optimized for bandwidth
    - For Testing purpose, the output bit number is not minimized
  - Data out on two differential lines @ 640 Mb/s
    - Serialized data out
    - Data strobe @ 640 MHz
  - Max event rate per Output line/FIFO => ~12.5 MHz
  - Max event rate per pixel => ~780 kHz



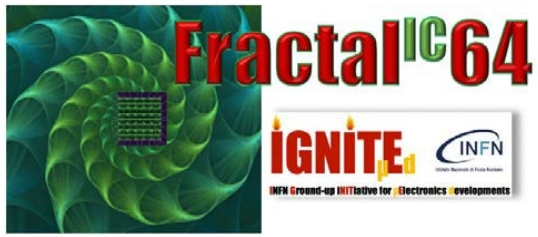


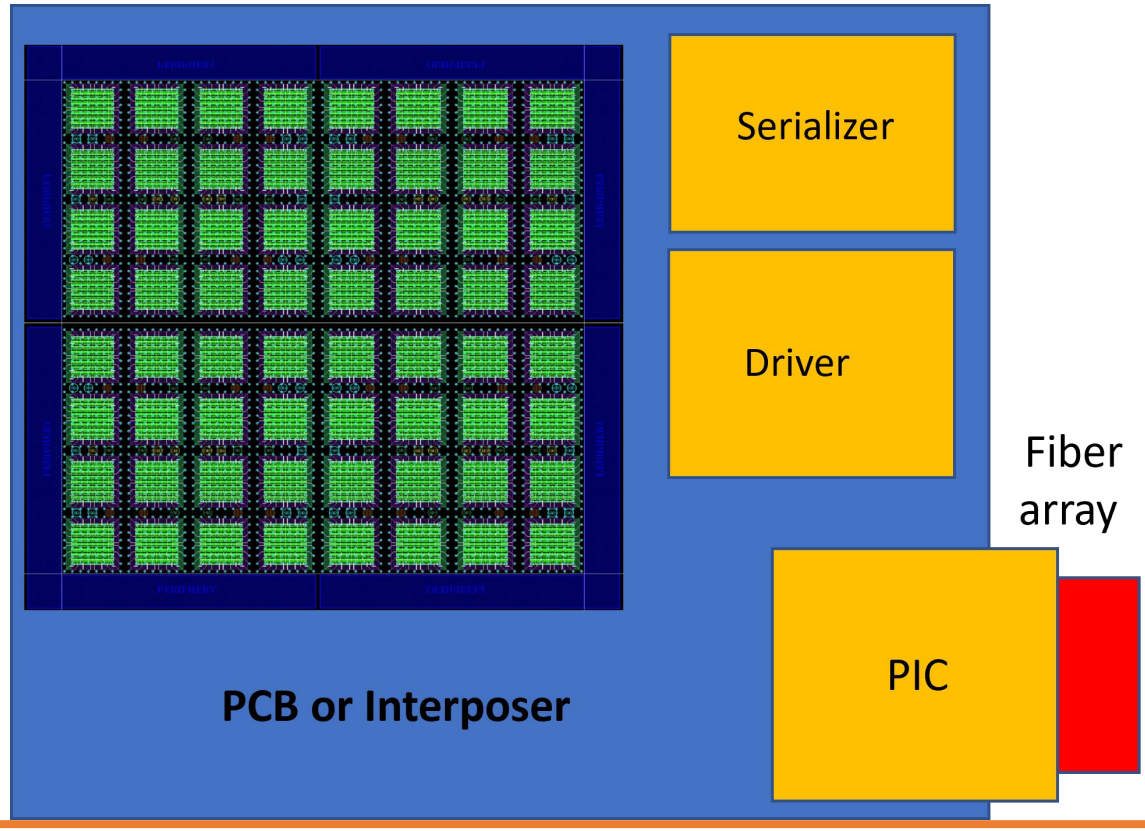
Bits																																																
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EF	HF	FF	Pix Addr[3:0]				EoC	Eota	TimeStamp[8:0]									cnt1[8:0]									cnt0[8:0]									tot[12:0]												

Conclusion

- IGNITE project aims to develop a 4D tracking system suitable for high-luminosity environments exploring innovative 3D integration technologies.
- We submitted a first prototype, "IGNITE0", in July '23 and expected in November '23.
  - It integrates 32 pixels, each one with its own AFE + TDC.
  - We include AFE cells in different flavors, Low Jitter PLL and other test structures.

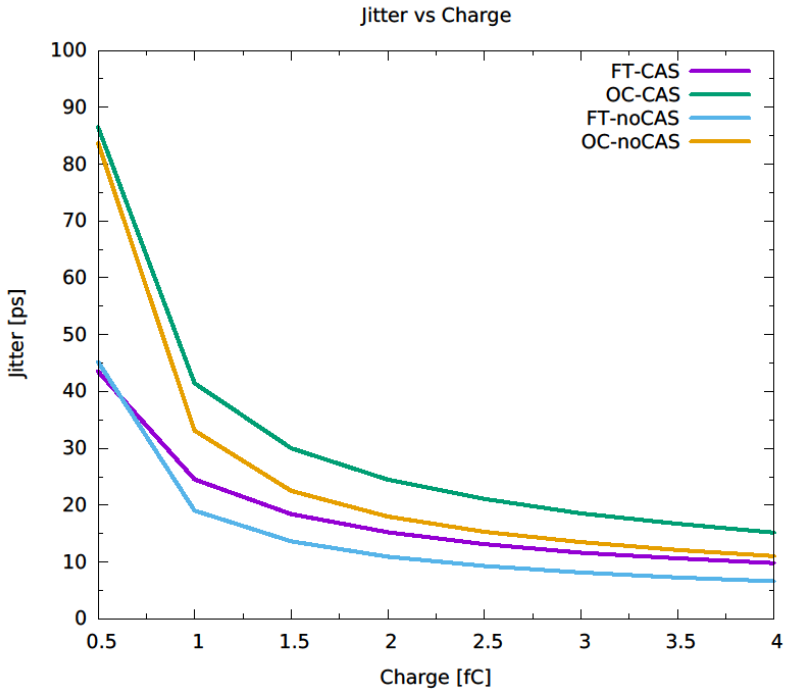
- Next ASIC, Fractalic64, will be submitted next year:
  - 64 x 64 pixels matrix.
  - It features an additional periphery for preliminary test with conventional wire-bond integration (dark blue area).
  - The ASIC can also be integrated with TSV.
- It will be first assembled with a regular PCB.
- Photonic Integrated Circuit (PIC) for optical data output.





Backup

IGNITE: AFE Jitter



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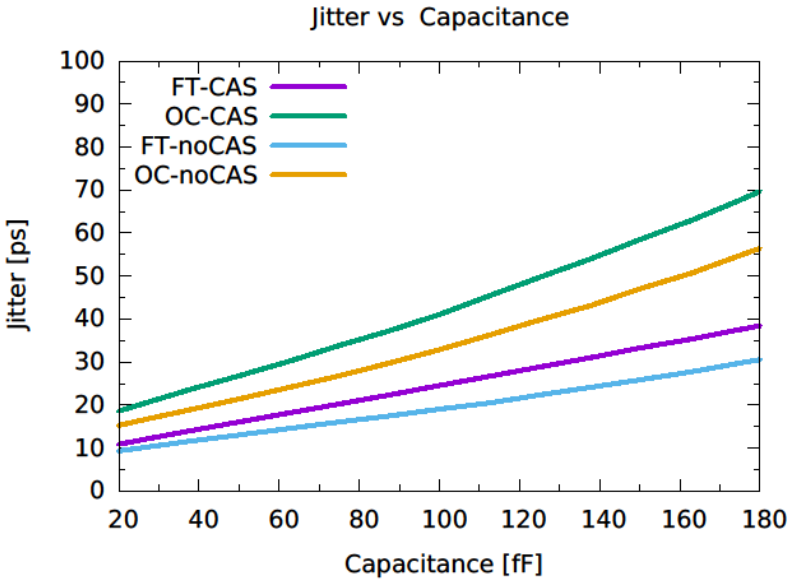
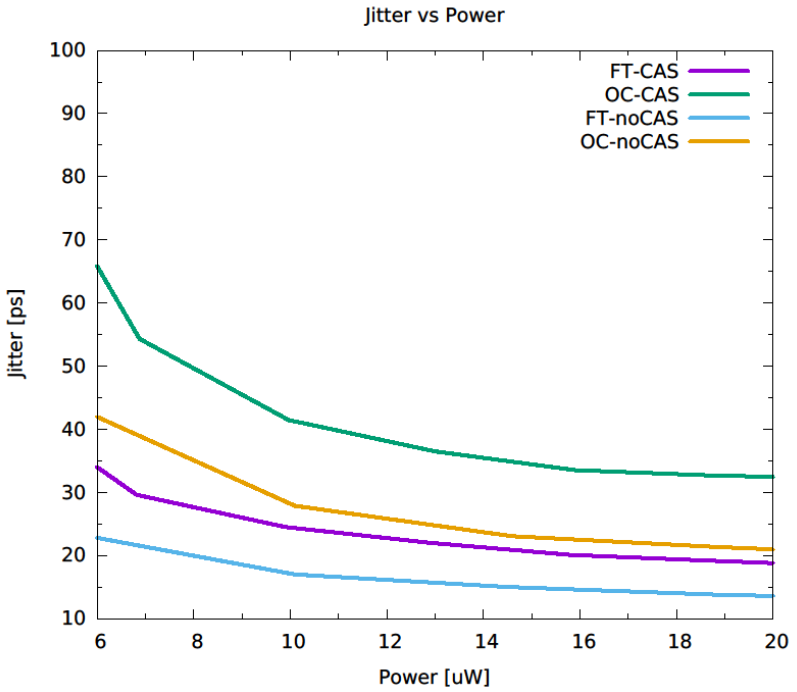


- (q_{in} = 1 fC, P =10.8 µW).
- Will be measured using on-chip programmable capacitors.
- Input capacitance depends on sensor geometry and coupling techniques.
- CSA: good linearity, adequate open loop-gain.



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- TDC requirement
  - Time of Arrival (TA):
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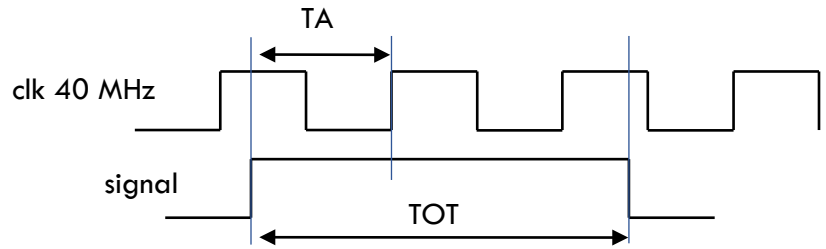
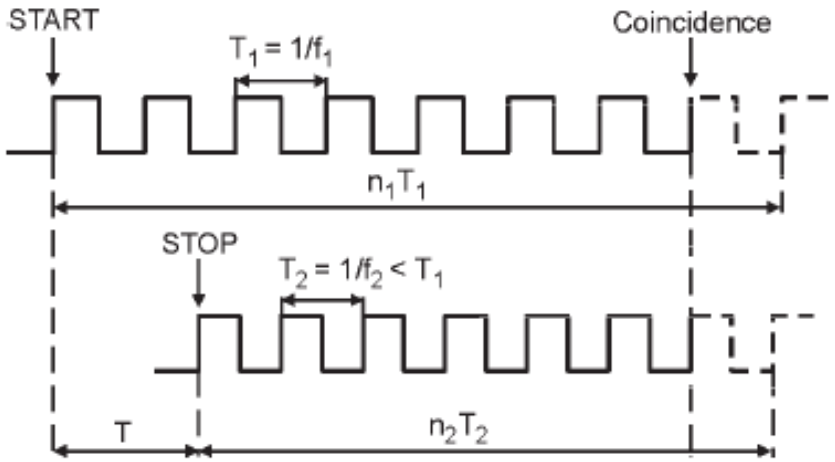


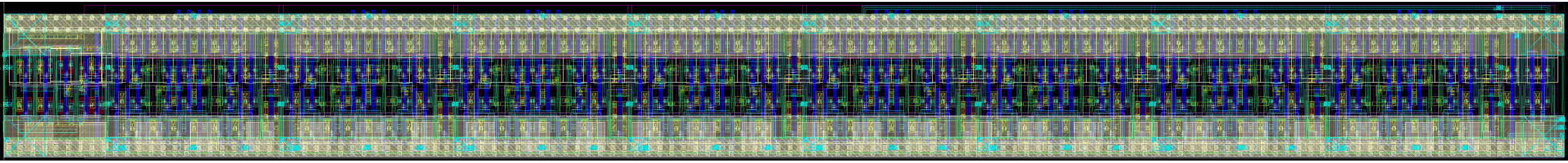


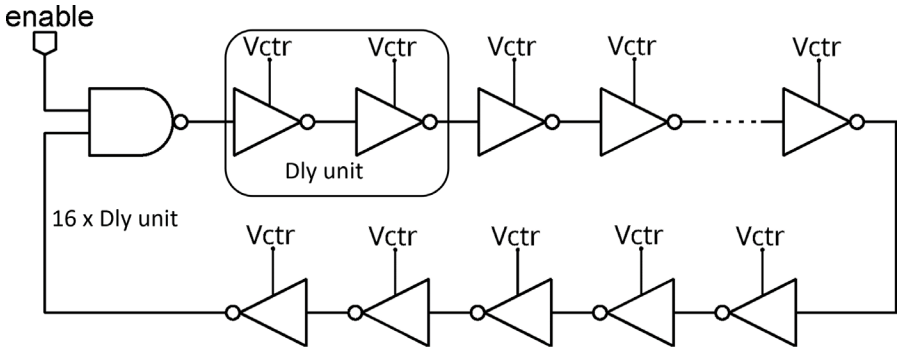
$$r = T_1 - T_2$$

$$TA = (cnt_1 - 1)T_1 - (cnt_2 - 1)T_2 = (cnt_1 - cnt_2)T_1 + cnt_2 r$$

$$T_{conv\_max} = \frac{T_1 \cdot T_2}{r(10ps)} \approx 100\ ns \qquad T_{conv\_max} = \frac{T_1 \cdot T_2}{r(30ps)} \approx 35\ ns$$

IGNITE TDC: the DCOs





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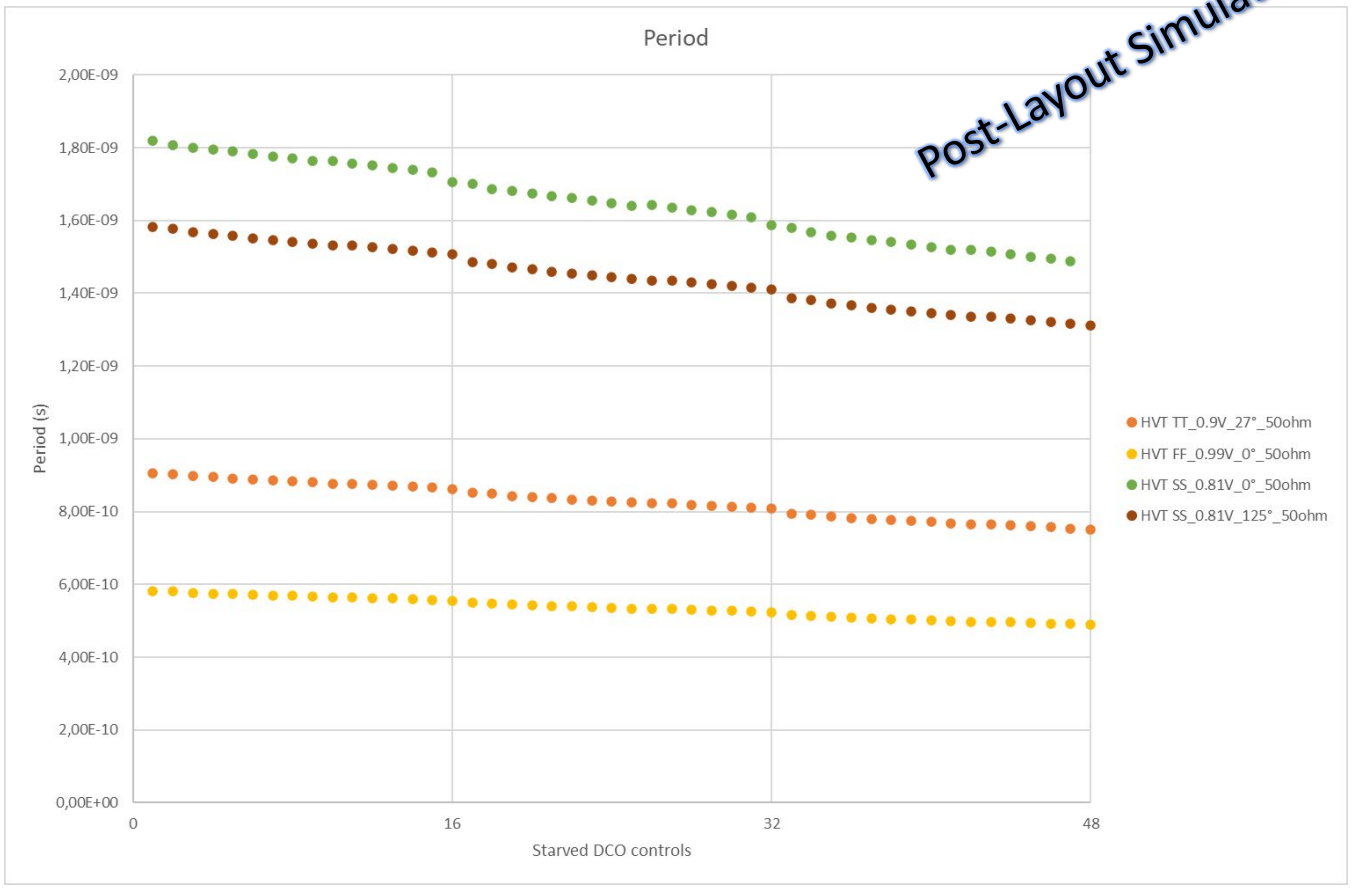

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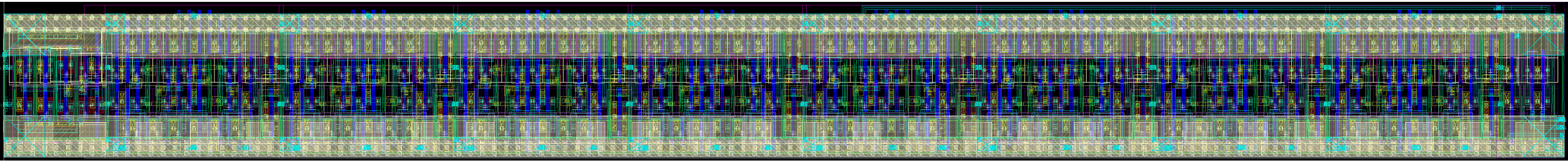

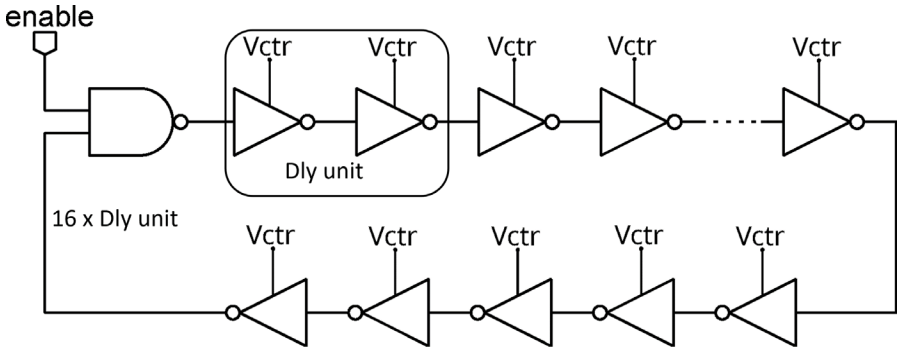

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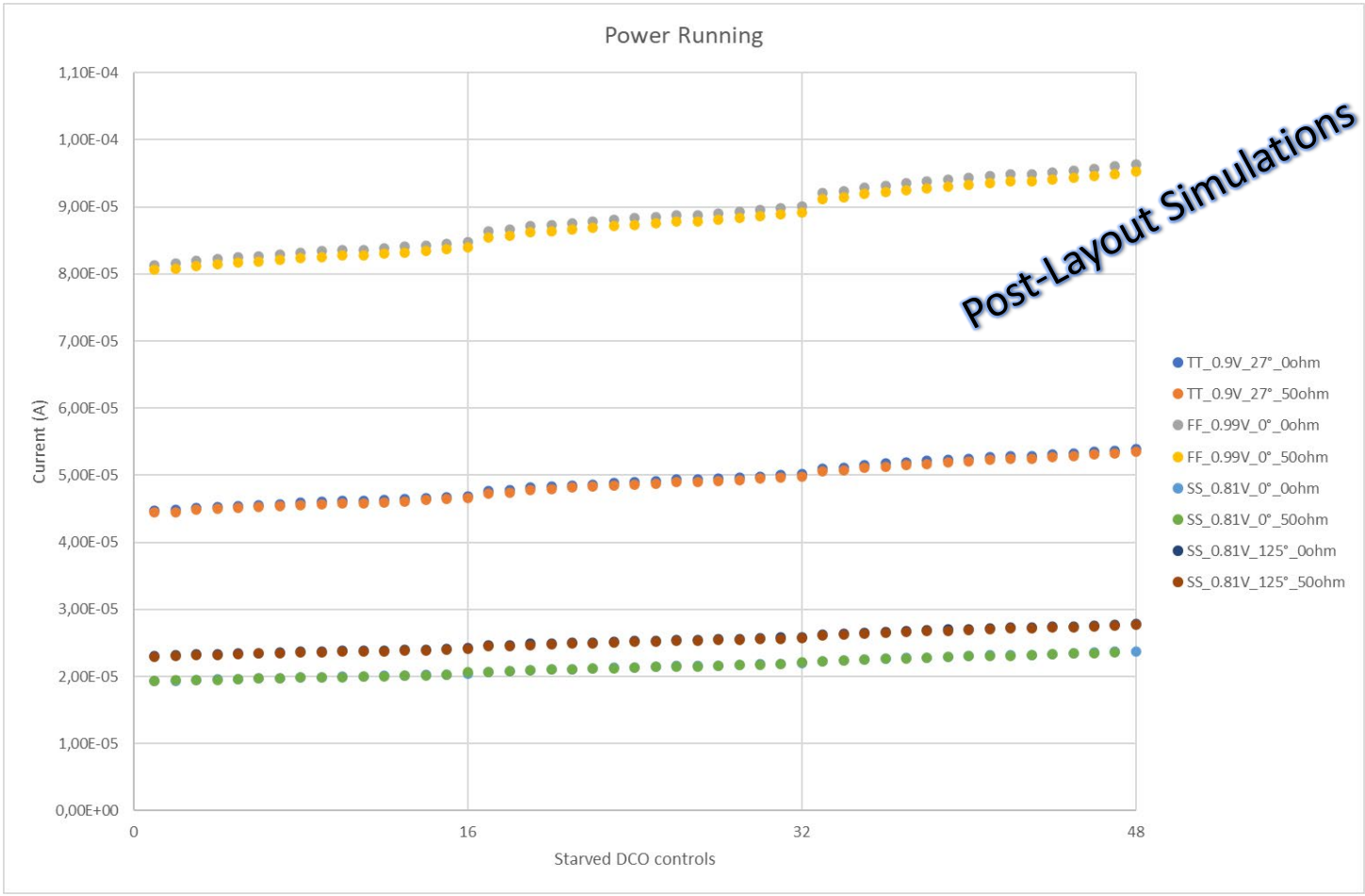
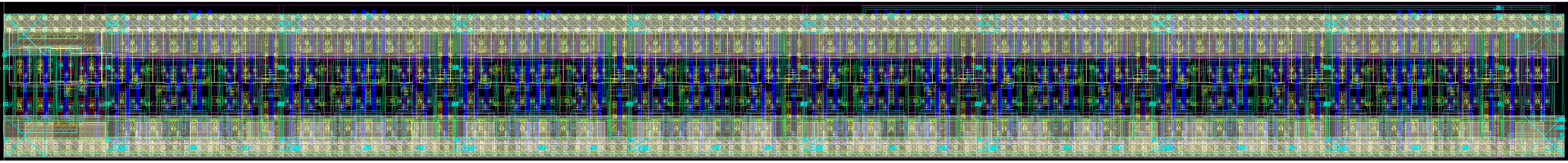
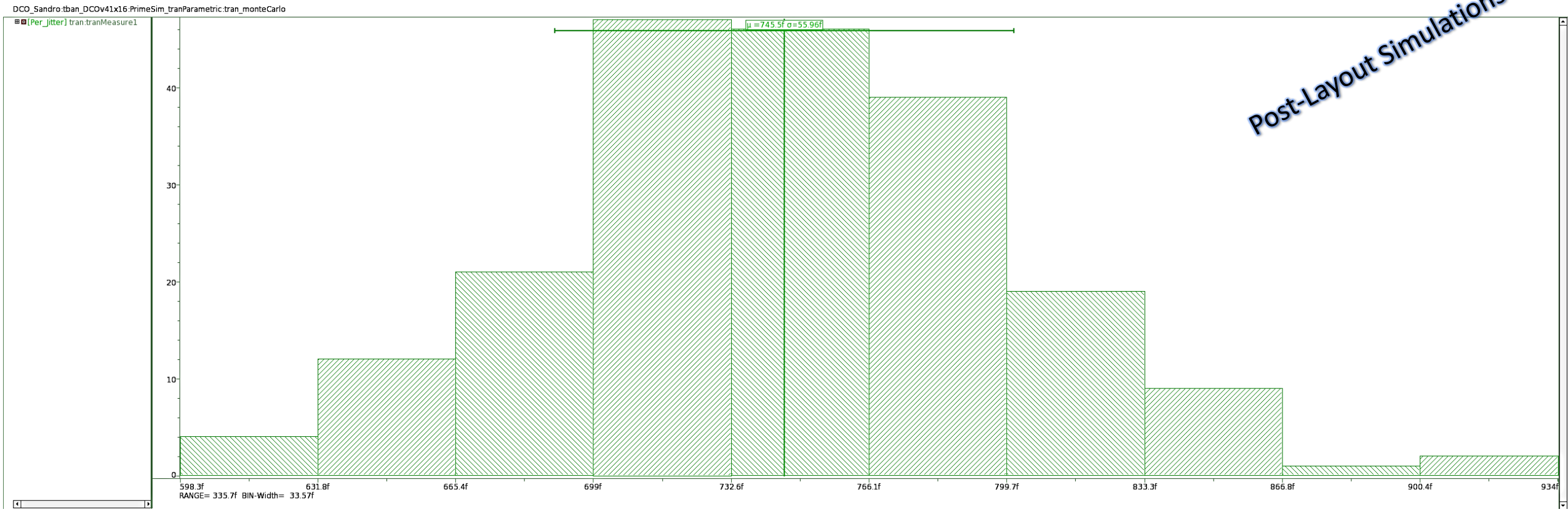
- **Number of Steps:** 16 Delay Units
  - Single delay cell with starved architecture
  - Power on/off configuration – fine tuning – coarse tuning
  - Decoupling capacitors
- **Step controls:** Fine ≈ 3ps - Coarse ≈ 50ps
- **Period Range:** ~ 900ps – 780ps (Typ)
- **Power Cons.:** ~ 45 µA – 55 µA (Typ)
- **Jitter:** ~ 750 fs – 600 fs (Typ)



IGNITE TDC: the DCOs





Post-Layout Simulations