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Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology

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The IGNITE project is developing solutions for the next generation of trackers at colliders. It plans to implement an integrated system module, comprising sensor, electronics, and fast readout, aimed at 4D-tracking. System pixels are required to have pitch around 50 μm and time resolution below 30 ps. In the present paper we present recent advancements on the design of a prototype ASIC, exploring several circuital solutions on the front-end side, in view of the first IGNITE ASIC, featuring a 64x64 pixel matrix, which is being completed in the coming months.

Summary (500 words)

The IGNITE project, funded by INFN, is developing solutions for the next generation of trackers at colliders, which may require high time resolution measurement at the pixel level, while keeping the pixel size and system power consumption substantially unaltered with respect to the present generation of inner tracking systems (e.g., CMS/ATLAS-phase2, LHCb Upgrade-1).

Following up and finalizing the developments of former INFN projects (TimeSPOT, Falaphel, Scaltech28), IGNITE plans to implement an integrated system module, comprising sensor, electronics, and fast readout, specifically aimed at 4D-tracking. System pixels are required to have pitch around 50 μm and time resolution below 30 ps. In the paper we present recent advancements on the design of a prototype ASIC (named Ignite_0), designed in CMOS 28-nm technology, which wants to explore several circuital solutions on the front-end side. The Ignite_0 development is preparatory to the design of the first IGNITE full-ASIC, featuring a 64x64 pixel matrix, being completed in the subsequent months.

The Ignite_0 ASIC is implemented as a mini-ASIC and contains new versions of the former TimeSPOT pixel, consisting of an Analog Front End (AFE) and a high-resolution Time-to-Digital-Converter.

The TimeSPOT-type AFE is a Charge Sensitive Amplifier with Krummenacher feedback and discrete-time Offset Compensation. Some imperfections, present in the TimeSPOT 32x32 matrix version, are here corrected and accurately simulated. New ideas on the AFE input stage and feedback circuit, aimed at obtaining a faster response to optimize the system performance in terms of time resolution, are here explored as well.

The TimeSPOT TDC, based on a Vernier-type architecture, have several improvements in terms of operational and SEU robustness. Furthermore, the front-end pixel size is also reduced from 55 μm (TimeSPOT) to the level of 40 μm, in order to make it possible the read-out of smaller pixel sensors.

The Ignite_0 ASIC integrates additional important service circuits, and in particular DACs and PLLS, to test them on silicon before their integration on the 64x64 pixel matrix, which has already started.

The explored solutions will be critically illustrated during the talk, highlighting their pro and cons.

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