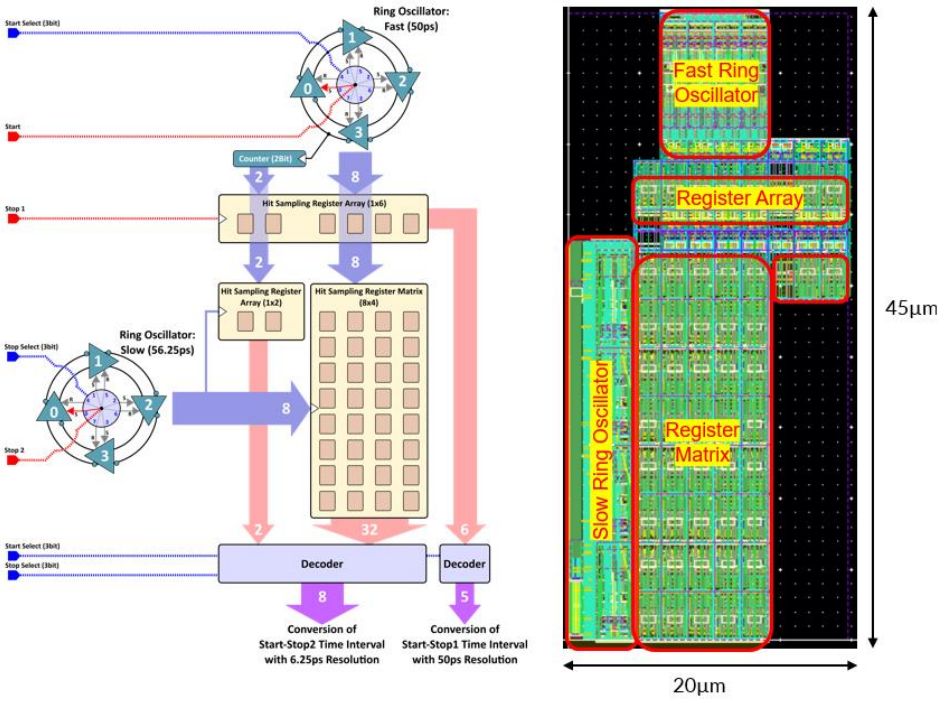
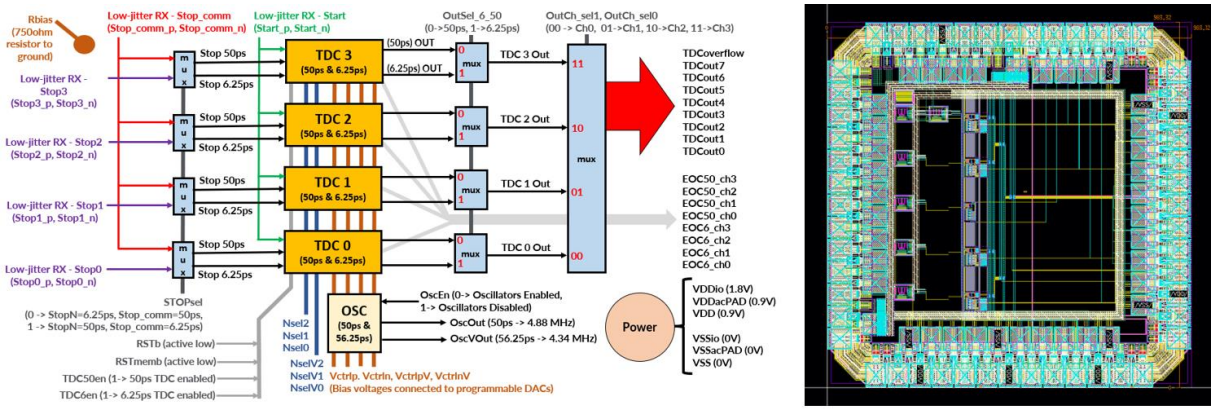


a) b)

Figure 1: TDC channel: a) block schematic, b) core layout.



a) b)

Figure 2: 28nm prototype ASIC: a) block schematic, b) layout. The ASIC includes 4 TDC channels, each capable of measuring time-intervals with 6.25ps and 50ps resolutions.