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Development of monolithic pixel sensor prototypes for the CEPC vertex detector

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The TaichuPix chip is a dedicated monolithic CMOS pixel sensor that is being developed for the first 6-layer silicon vertex detector prototype of the Circular Electron Positron Collider (CEPC) vertex detector R&D. Two small-scale demonstrator chips (25 mm^2) had been designed to optimize the in-pixel circuit and readout architecture, and to verify the radiation hardness. The positive results of the small-scale prototypes led to a submission of the first full-scale (2.6 cm × 1.6 cm) TaichuPix prototype in 2022. The design details and test results of TaichuPix prototypes and development of the readout electronics will be given.

Summary (500 words)

The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption. The TaichuPix chip need to provide a spatial resolution better than 5 μm, a power density lower than 200 mW/cm2, and a Total Ionizing Dose (TID) tolerance higher than 1 MRad. Fig.1 shows the architecture of a full-scale TaichuPix chip, including a matrix of 512 × 1024 pixels with a size of 25 × 25 μm2. Each pixel integrated a sensing diode, a front-end and a hit storage registers and logic for pixel mask and test. Pixels are arranged in double columns, with priority encoder within column and timestamp recorded at the end of double column (EOC). All the 512 double columns are read out in parallel, in order to minimize the dead time. For each double column, a fast-or busy signal delivers to the EOC when any pixel generates a hit signal. The timestamp with a resolution of 25 ns is generated whenever a new fast-or busy signal is received. Fired pixels in the same cluster share a common timestamp as the Trigger ID. The pixel addresses of the fired pixels are temporarily stored in a column level FIFO (FIFO1). The 512 double columns and the corresponding EOC logics are divided to 4 blocks, and each one integrating a chip level FIFO (FIFO2). There are four groups in each block with each group including 32 double columns. The 32 FIFO1 inside each group are read out according the address priority, while the 4 groups are read out sequentially to the FIFO2. The four FIFO2 are read out through a hierarchical data multiplier. The readout of TaichuPix chip is compatible to both trigger and trigger-less modes.

Two small-scale prototypes have been developed and characterized to address the chip architecture and major functionalities. The test results show the average pixel noise is 10-29 e- and the threshold dispersion is 25-58 e-, depending on the pixel variants. One of the two parallel in-pixel digital designs is properly operating at a 40 MHz clock. The tests with X-ray and 90Sr sources proved the functionality of the pixel array and digital periphery. The highest serial data transmission rate is tested to be 3.36 Gbps. The positive results of the small-scale prototypes led to a submission of the first full-scale (2.6 cm × 1.6 cm) TaichuPix-3 prototype in 2022.

To verify the spatial resolution of the sensor prototype, a beam telescope based on TaichuPix-3 chips was built. The readout electronics for both the single sensor and the telescope have been developed (see Fig.2). The full-scale sensor chip was characterized at the DESY test beam facility. The preliminary results indicate that the best spatial resolution of the individual TaichuPix-3 sensor is better than 5 μm combined with a detection resolution of around 99% (see Fig.3). The TaichuPix-3 also fulfill the power consumption and TID tolerance requirements.

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