The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results

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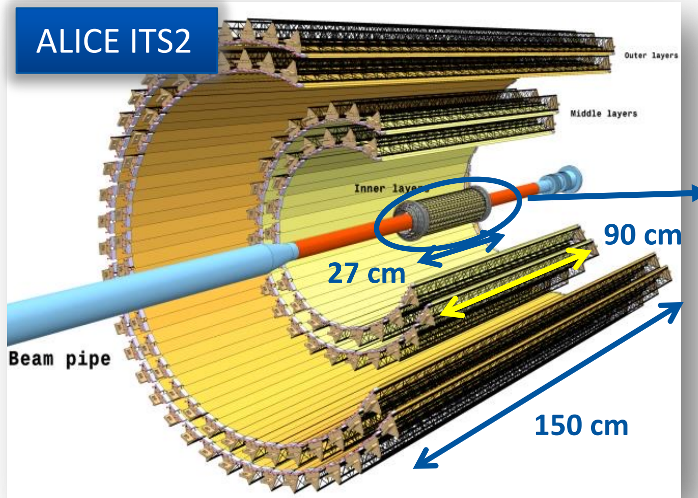
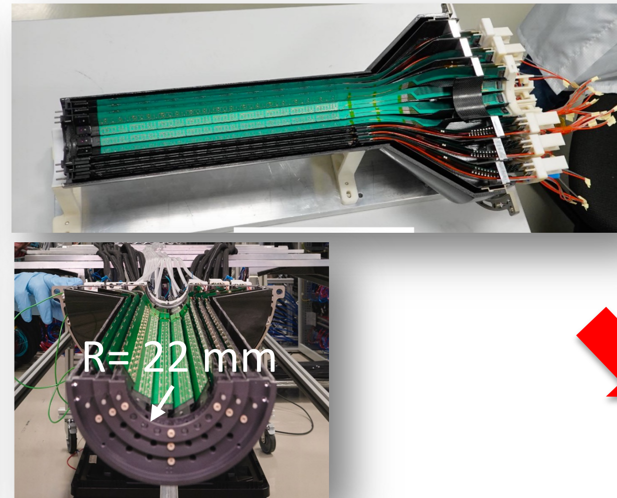
On behalf of the ALICE Collaboration

Outline

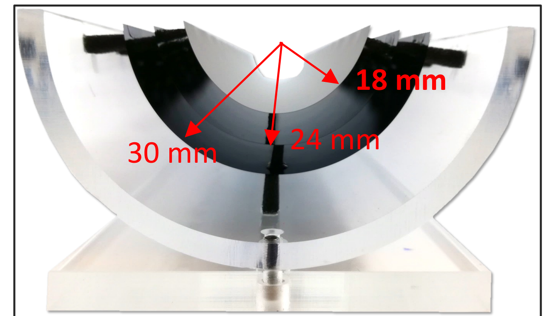
1. Context and motivation
2. MOSS Chip
3. Test System for MOSS
4. Glance at first Test Results

ALICE ITS3 Upgrade





~12.5 Gpixels, 10 m^2 sensitive area
24120 **ALPIDE** Pixel Sensors (CMOS 180 nm)



Replace inner barrels by real half-cylinders of **bent thin** silicon

Minimize **material budget** and **radial distance** from interactions

Improve vertexing and physics yield

Rely on **wafer-scale MAPS sensors**

← How to design and build these?

ER1 Submission

Aim at learning and proving **stitching**, submitted in December 2022

65 nm CMOS Imaging Technology

Design activities framed within **CERN EP R&D WP1.2**

- Large effort of several teams and institutes

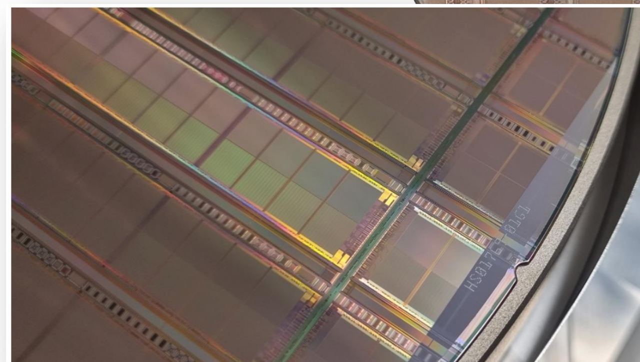
Two wafer scale stitched sensor chips (MOSS, MOST)

- Different design approaches for resilience to manufacturing faults

MOSS (1 of 6)

MOST (1 of 6)

300 mm wafer

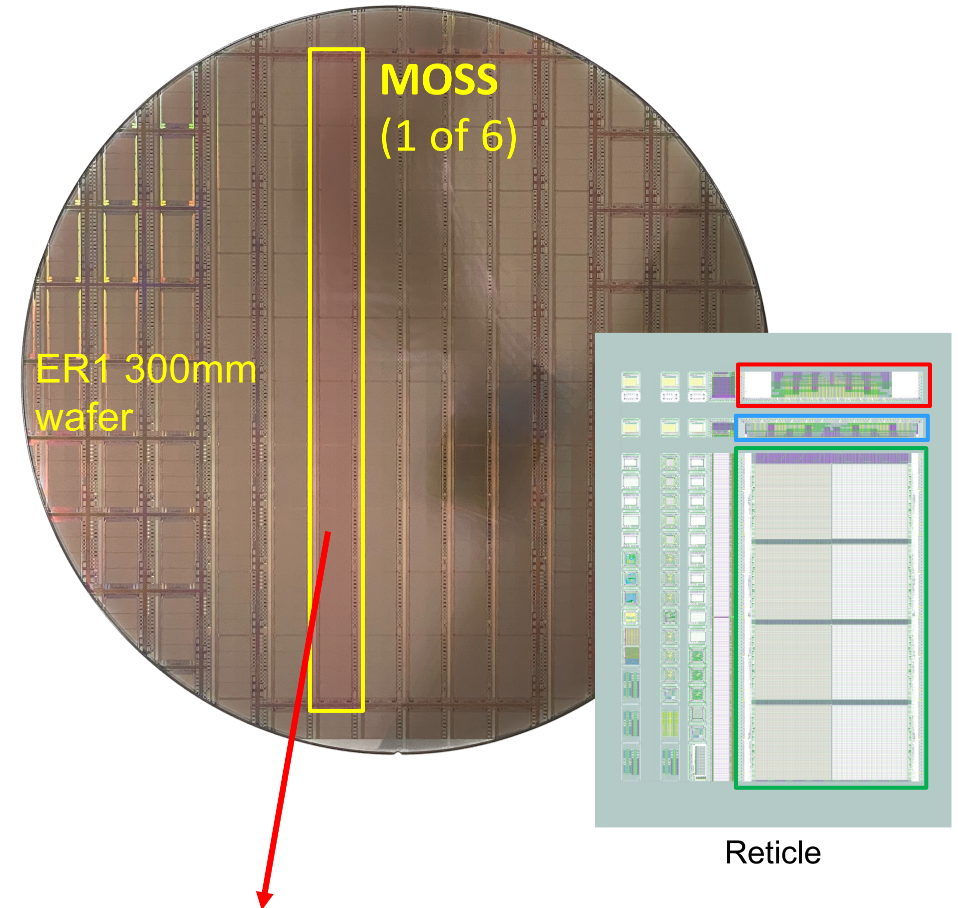


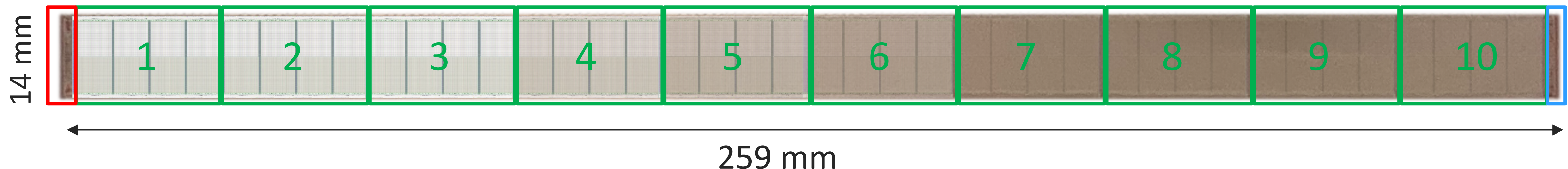
MOSS Monolithic Stitched Sensor Prototype

Primary Objectives
Learn design with stitching to build wafer scale particle detectors
Distribute power and signals on wafer scale chip
Study manufacturing yield and constraints
Study power, leakage, noise, spread

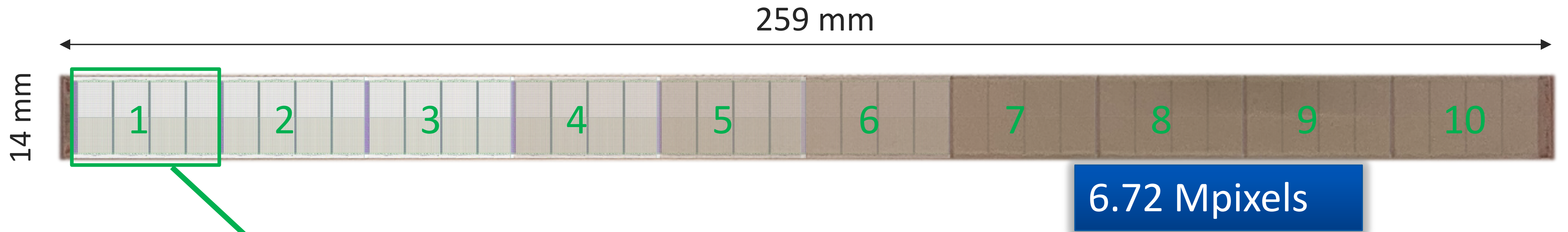
Repeated units abutting on short edges

- Repeated Sensor Unit, Endcap Left, Endcap Right
- Functionally independent designs
- Metal traces cross stitching boundaries for power distribution and long range on-chip control and data transfer
- Module integration on wafer scale die for the first time

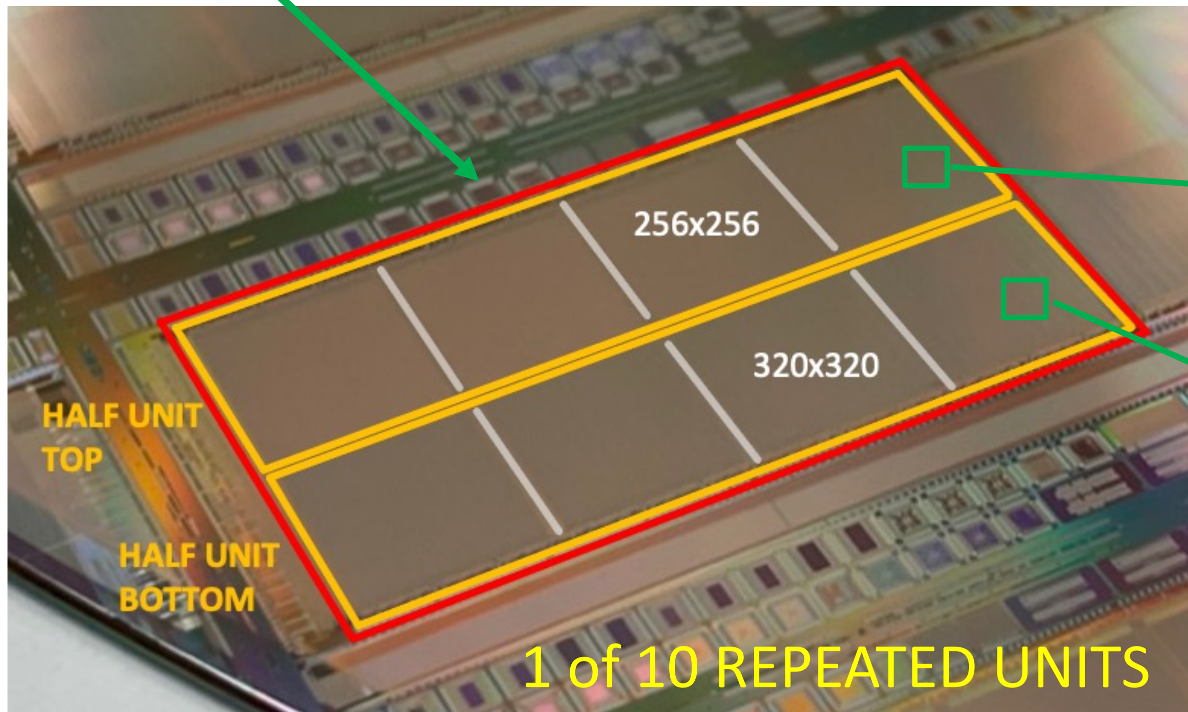




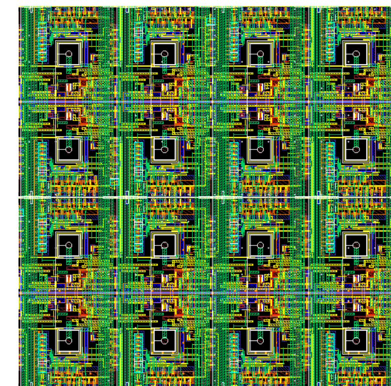
MOSS Layout



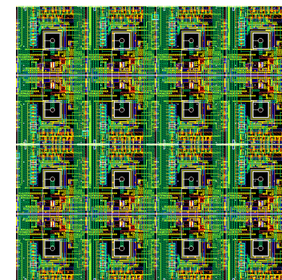
6.72 Mpixels



Large Pixel Pitch
22.5 μm

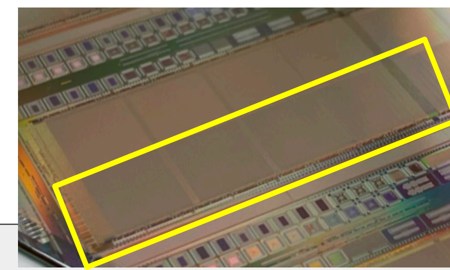


Fine Pixel Pitch
18 μm

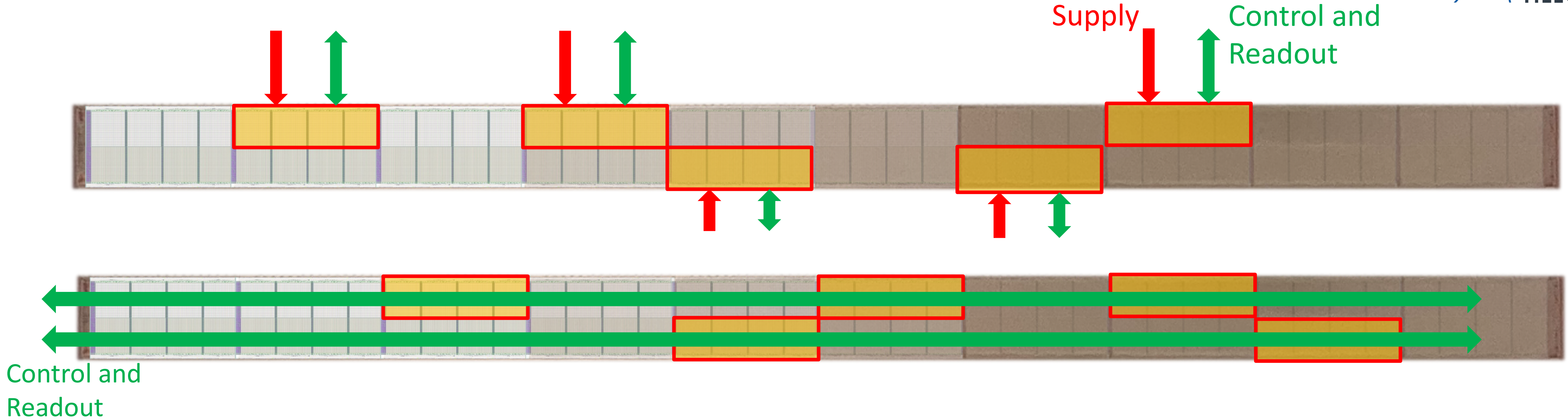


Investigate effects of layout density

MOSS - Half Unit



MOSS Testing



Power and test half units

Test one by one first and then in parallel from the left endcap

Validate long range transmission of signals

Learn and improve manufacturability

Yield at half unit, block, column/row/pixel level granularity

Study sensing performance with large arrays

64 Power Domains + Substrate
107 Supply Nets
2192 bonding pads
390 Digital I/Os, 480 Analog I/Os

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3. Test System for MOSS
4. First Glance at Test Results

MOSS Test System

MOSS Carrier

Proximity Board

Power regulation and analog services for 5 MOSS half-units

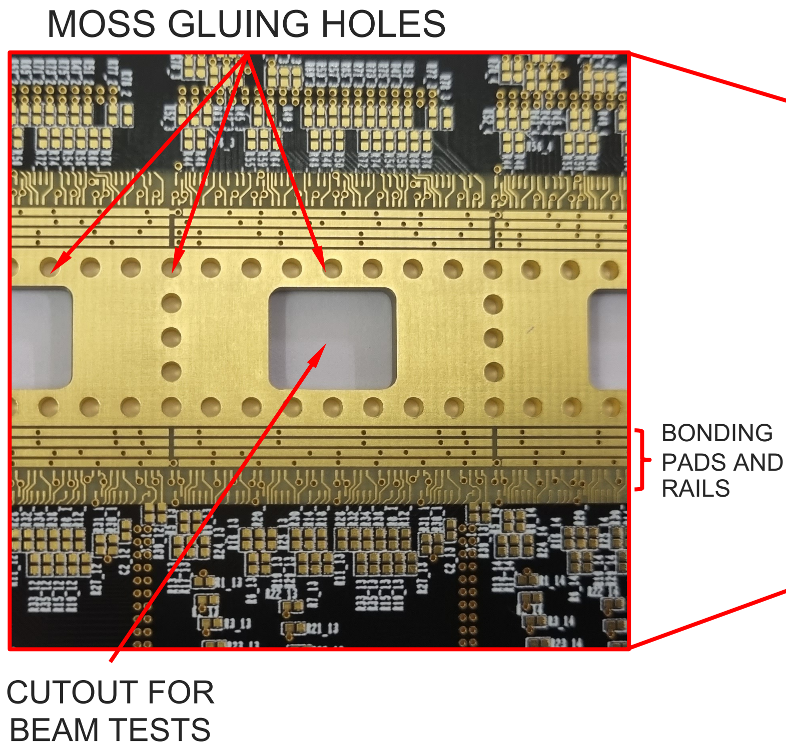
Automation and readout module

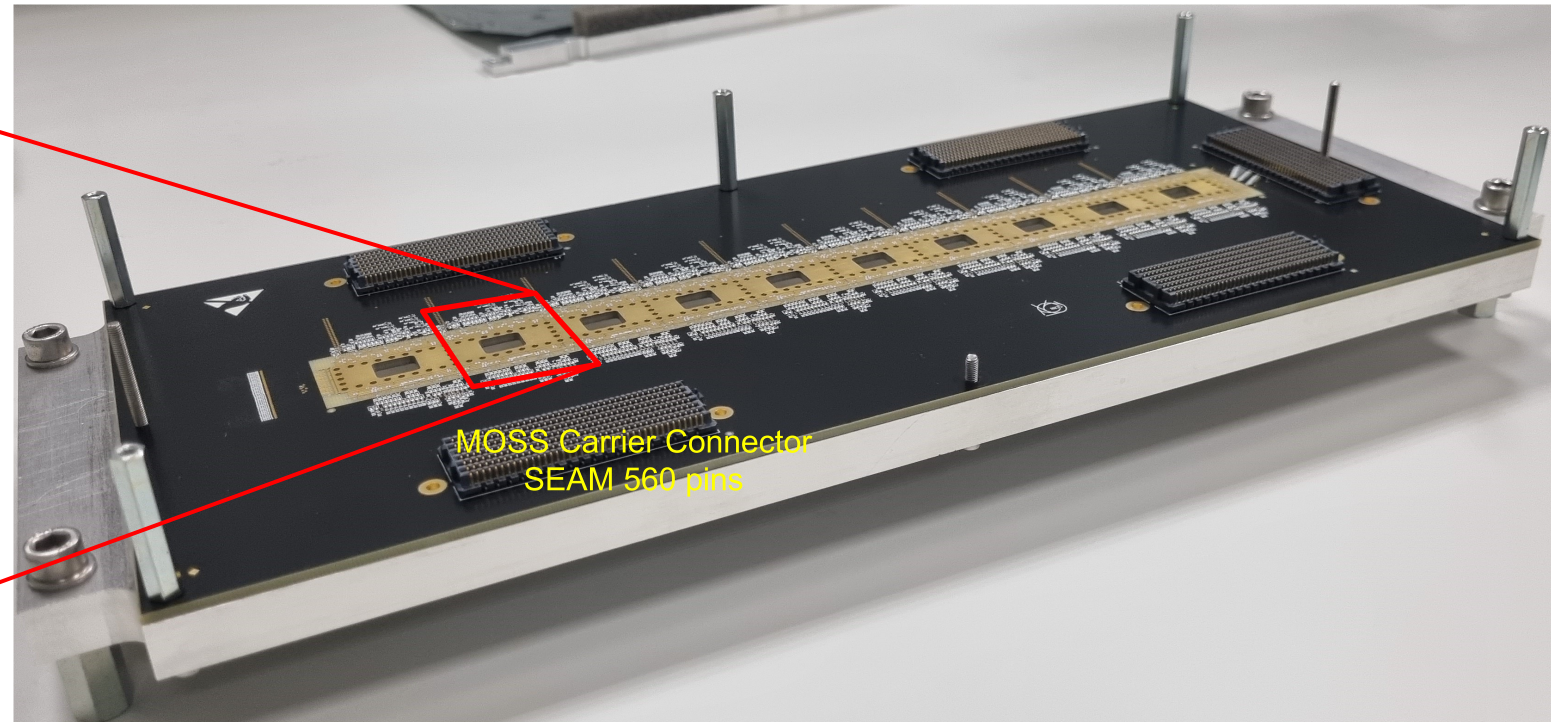
Steers the proximity boards

Interfaces with MOSS and with the host computer

Proximity Board
Proximity Board
Proximity Board
26 cm
MOSS Chip Carrier
Proximity Board
Proximity Board
73 cm
Automation and Readout
65 cm

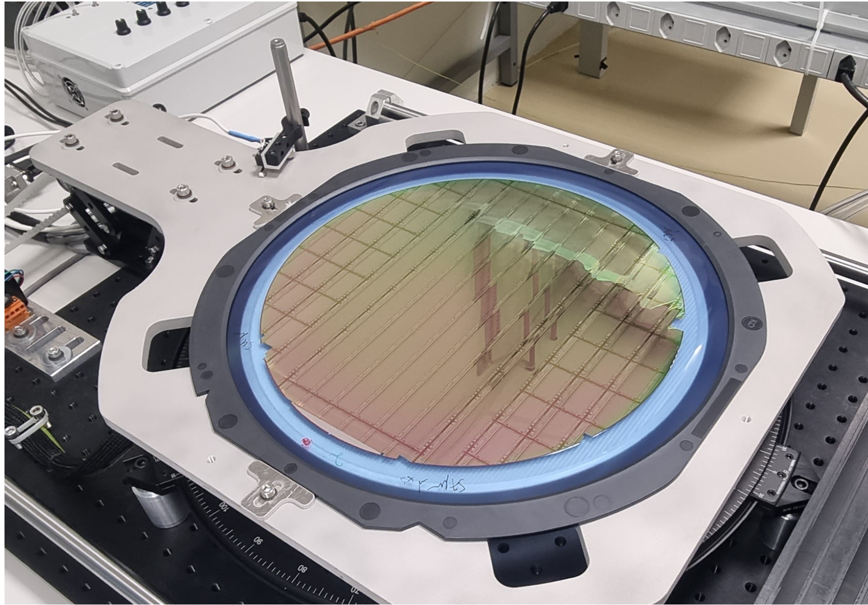
MOSS Carrier Board

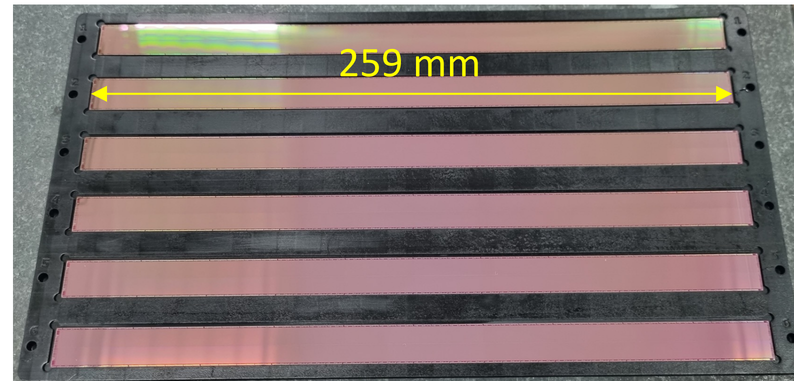


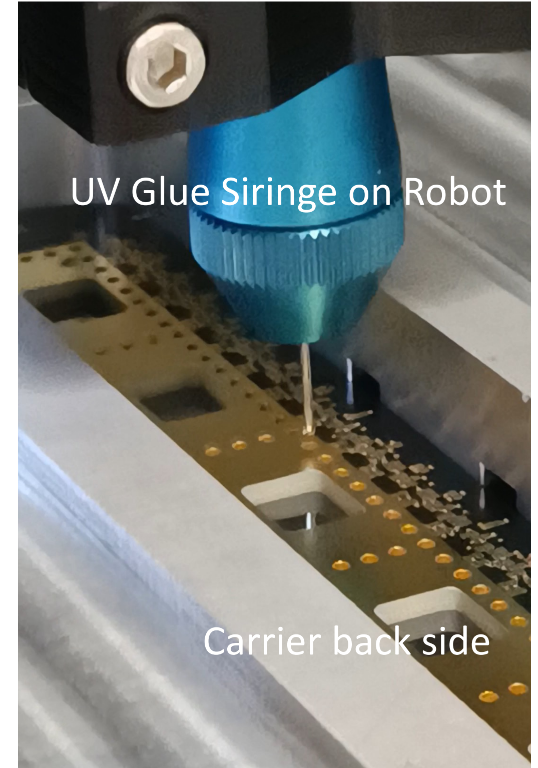


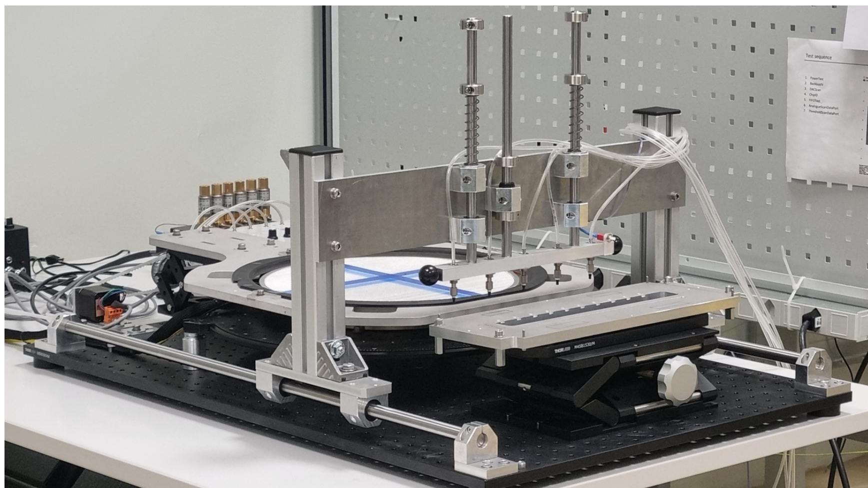
12 layers PCB, passive board, interconnects and decoupling
Very high routing density near chip and connectors
Features for placing, aligning and gluing the MOSS chip

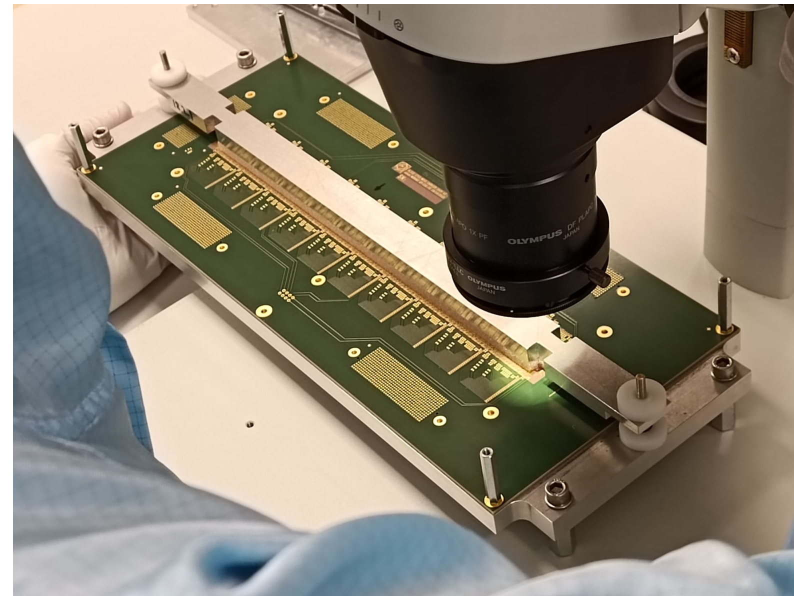
Pick, Align, Glue MOSS on Carrier

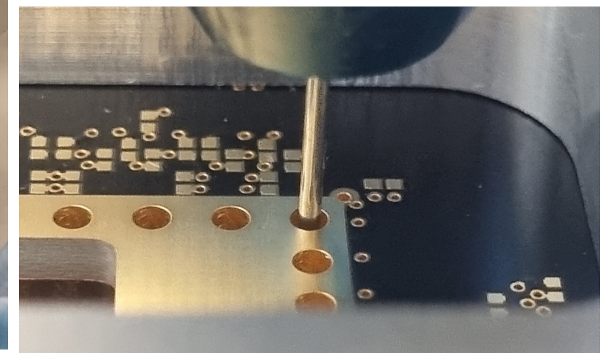




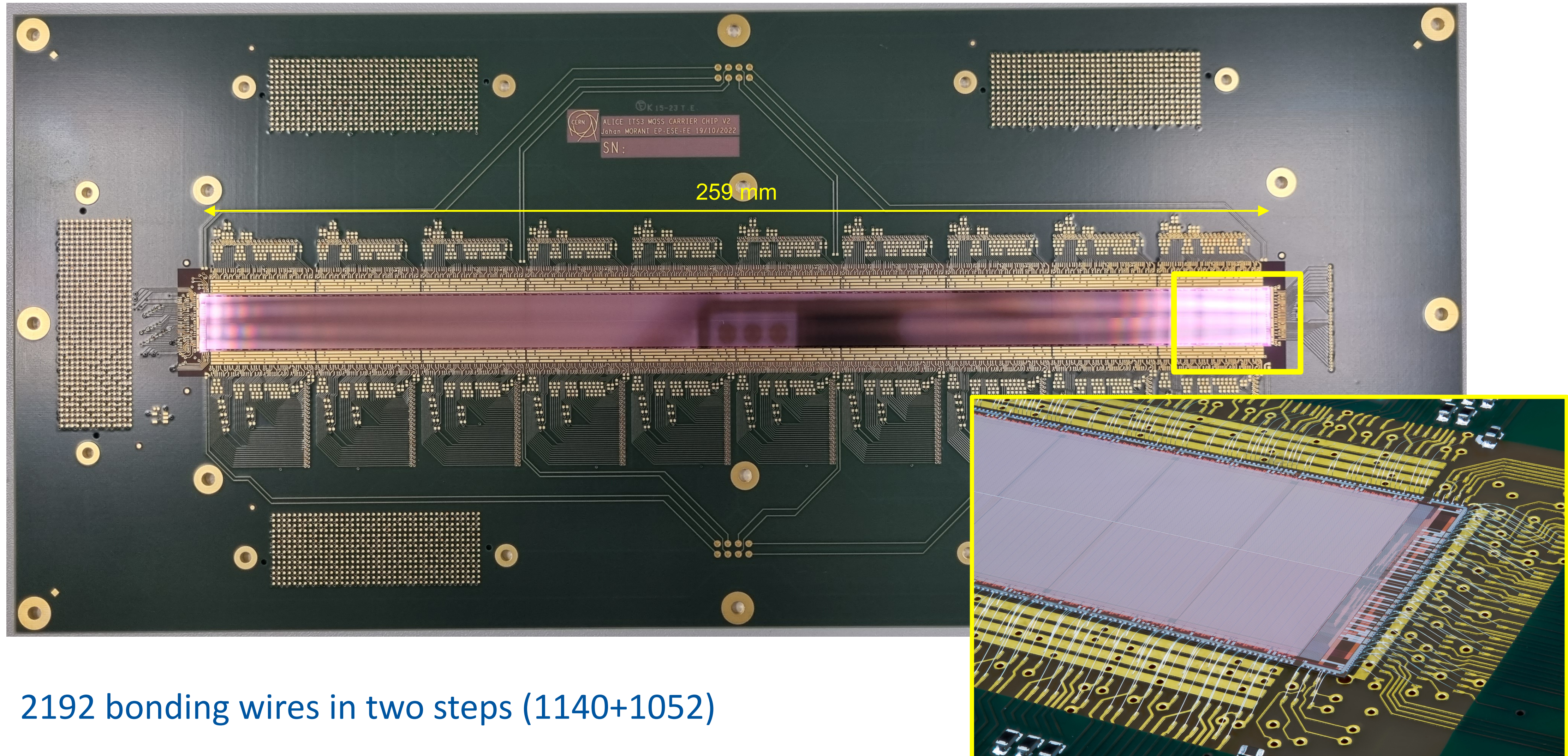








Wire Bonding MOSS on Carrier



2192 bonding wires in two steps (1140+1052)

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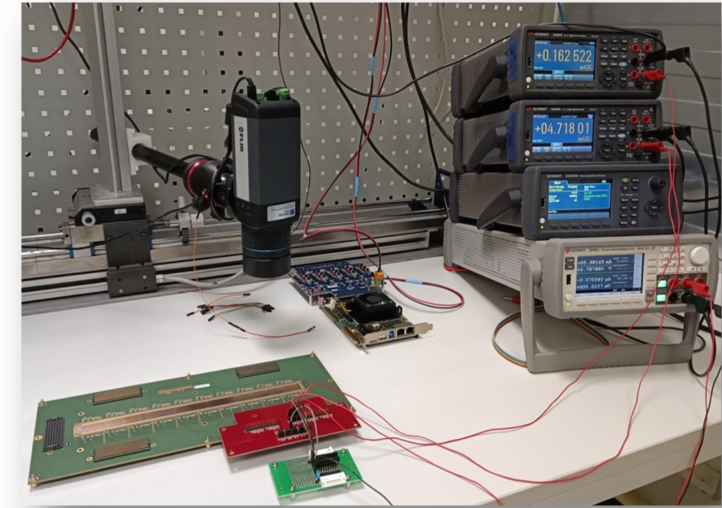
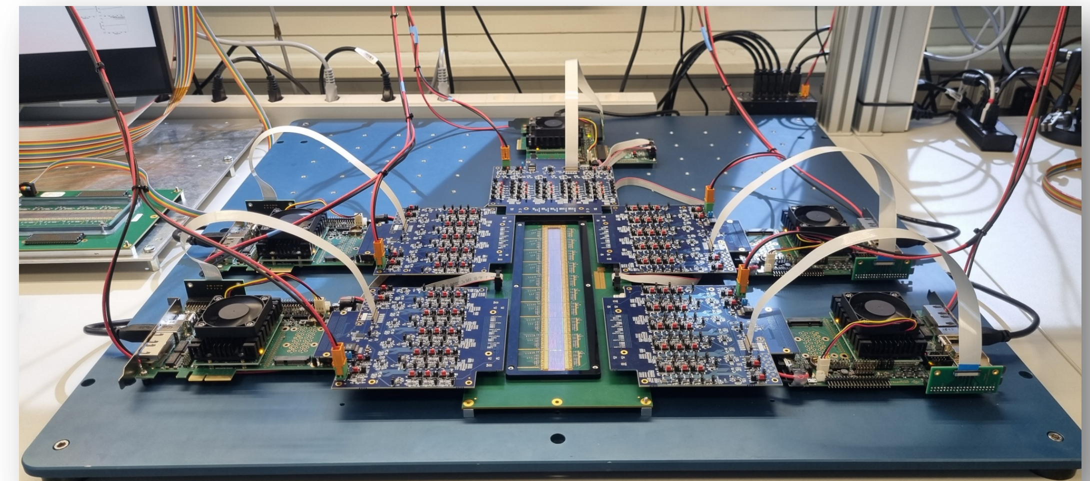
4. **First Glance at Test Results**

Testing Procedures with MOSS on Carriers

Shorts or anomalies?	Impedance Tests	MOSS Carrier + Lab Equipment
I-V characteristic?	Power Ramps	
Changes in impedance?	Impedance Tests	
Full powering Initialization Registers Scan DACs Scan Threshold scans Fe55	Full Powering Scans + Functional Tests	MOSS Test System
	Beam Tests	





Power Ramp Tests

Power Ramps

Ramp supplies slowly and monitor currents

- OK -> all supplies ramped to full voltage and currents less than compliance limit
- Wafer maps reconstructed from power ramps data of MOSS on carriers
- *Preliminary results.* Refining current thresholds, grounding, ramp rates

Wafer to wafer differences

- First results with MOST chip consistent with MOSS data

WAFER 17

Power Ramp - 36/100=36.00% HUs OK

	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10	
1-TOP	nOK	OK	OK	nOK	nOK	nOK	nOK	OK	OK	OK	50.0% OK
1-BOT	OK	OK	nOK	OK	nOK	nOK	nOK	nOK	OK	OK	
2-TOP	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	
2-BOT	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	
3-TOP	nOK	nOK	nOK	nOK	nOK	nOK	nOK	nOK	OK	OK	15.0% OK
3-BOT	nOK	nOK	nOK	nOK	nOK	nOK	nOK	nOK	OK	nOK	
4-TOP	OK	OK	OK	nOK	nOK	nOK	nOK	OK	OK	OK	45.0% OK
4-BOT	OK	nOK	OK	nOK	nOK	nOK	nOK	nOK	OK	nOK	
5-TOP	OK	nOK	OK	nOK	nOK	nOK	nOK	nOK	OK	nOK	30.0% OK
5-BOT	nOK	OK	nOK	nOK	nOK	nOK	nOK	OK	OK	nOK	
6-TOP	OK	nOK	OK	nOK	nOK	nOK	nOK	nOK	OK	OK	40.0% OK
6-BOT	OK	OK	OK	nOK	nOK	nOK	nOK	nOK	nOK	OK	

WAFER 23

Power Ramp - 90/120=75.00% HUs OK

	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10	
1-TOP	OK	OK	OK	nOK	OK	OK	OK	nOK	nOK	OK	80.0% OK
1-BOT	OK	OK	OK	OK	OK	nOK	OK	OK	OK	OK	
2-TOP	OK	OK	nOK	nOK	nOK	nOK	OK	OK	OK	OK	75.0% OK
2-BOT	OK	OK	OK	OK	OK	nOK	OK	OK	OK	OK	
3-TOP	OK	OK	nOK	nOK	nOK	nOK	nOK	OK	OK	nOK	60.0% OK
3-BOT	OK	OK	OK	OK	OK	nOK	OK	OK	nOK	OK	
4-TOP	OK	nOK	nOK	nOK	OK	OK	OK	OK	OK	OK	75.0% OK
4-BOT	OK	OK	OK	OK	OK	OK	nOK	nOK	OK	OK	
5-TOP	OK	OK	OK	nOK	OK	OK	OK	OK	OK	OK	75.0% OK
5-BOT	nOK	OK	nOK	OK	nOK	nOK	OK	OK	OK	OK	
6-TOP	OK	OK	OK	OK	nOK	OK	OK	OK	OK	OK	85.0% OK
6-BOT	OK	OK	OK	OK	OK	nOK	OK	OK	nOK	OK	

WAFER 24

Power Ramp - 90/96=93.75% HUs OK

	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10	
1-TOP	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**Full MOSS**
1-BOT	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	
2-TOP	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	95.0% OK
2-BOT	nOK	OK	OK	OK	OK	OK	OK	OK	OK	OK	
3-TOP	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	
3-BOT	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.	
4-TOP	OK	nOK	OK	OK	n.c.	OK	OK	OK	OK	n.c.	81.2% OK
4-BOT	n.c.	OK	nOK	OK	OK	n.c.	OK	OK	nOK	OK	
5-TOP	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	**Full MOSS**
5-BOT	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	
6-TOP	nOK	OK	nOK	OK	OK	OK	OK	OK	OK	OK	90.0% OK
6-BOT	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	

Fully Functional MOSS Units

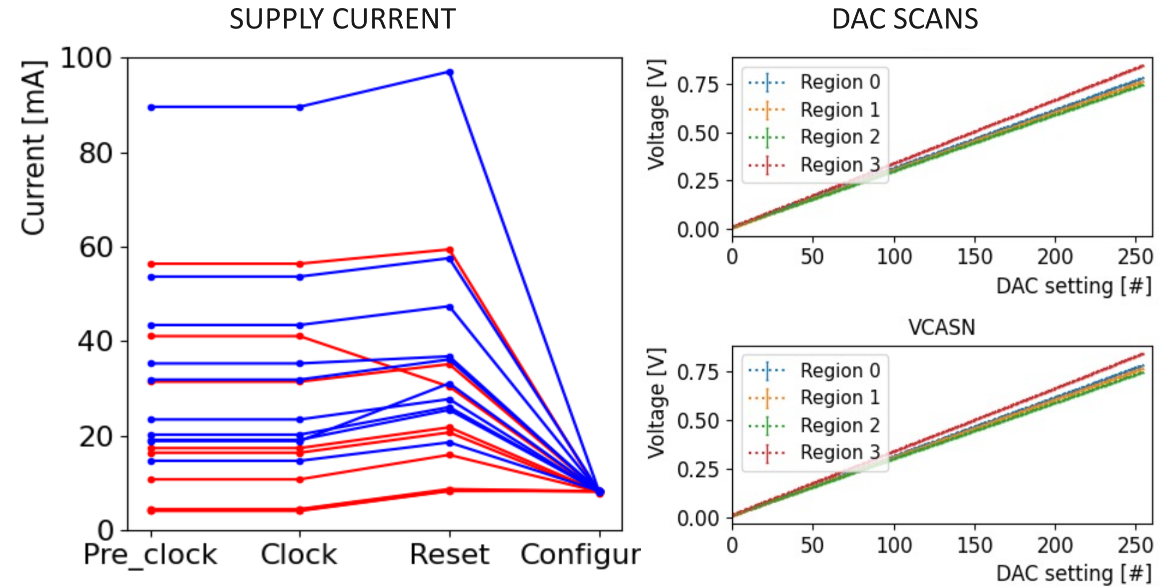
Full Powering Scans + Functional Tests

MOSS Unit passing Power Ramps Test pass Full Powering and Register Scan

- Initialization and then read/write all registers
- Using the I/Os distributed on the long edges

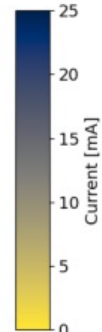
Biasing DAC Scans

- Internal bandgaps and DACs are functional
- Characterizing linearity and spreads



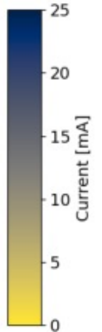
W24 - ANALOG CURRENTS

	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10
1-TOP	6.8	6.9	7.0	7.0	6.9	7.1	7.1	6.9	7.2	7.0
1-BOT	8.2	8.2	8.4	8.4	8.3	8.2	8.5	8.3	8.8	8.9
2-TOP	9.6	6.8	6.7	6.8	7.0	6.8	7.1	7.1	7.0	5.7
2-BOT	n.c	8.2	8.4	8.2	8.4	8.3	8.4	8.3	9.1	8.2
3-TOP	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
3-BOT	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
4-TOP	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
4-BOT	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
5-TOP	6.8	6.9	7.0	7.1	6.9	7.2	7.3	7.1	7.2	7.0
5-BOT	8.4	8.5	8.6	9.0	8.3	8.6	8.6	8.9	8.4	8.7
6-TOP	n.c	7.2	n.c	7.2	11.2	7.3	7.2	7.1	7.1	7.0
6-BOT	11.2	8.4	11.2	8.7	8.7	8.9	9.0	8.5	8.4	8.7

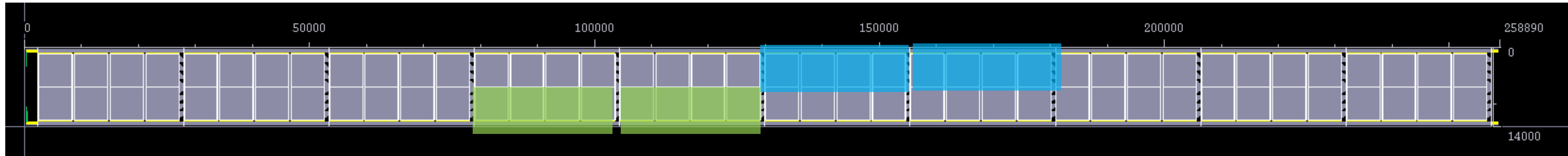


W24 - DIGITAL CURRENTS

	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10
1-TOP	6.0	6.2	6.2	6.3	6.4	6.4	6.3	6.3	6.2	6.1
1-BOT	6.4	6.6	6.6	6.7	6.8	6.7	6.7	6.6	6.6	6.6
2-TOP	6.1	6.2	6.1	6.3	6.3	6.3	6.3	6.3	6.3	7.3
2-BOT	n.c	6.5	6.6	6.7	6.8	6.7	6.7	6.6	6.6	6.5
3-TOP	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
3-BOT	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
4-TOP	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
4-BOT	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c	n.c
5-TOP	6.1	6.2	6.2	6.3	6.4	6.5	6.4	6.3	6.2	6.2
5-BOT	6.5	6.6	6.6	6.7	6.8	6.8	6.7	6.7	6.6	6.6
6-TOP	n.c	6.5	n.c	6.5	6.5	6.6	6.5	6.5	6.3	6.2
6-BOT	6.5	6.6	6.7	6.7	6.8	6.8	6.7	6.7	6.7	6.6



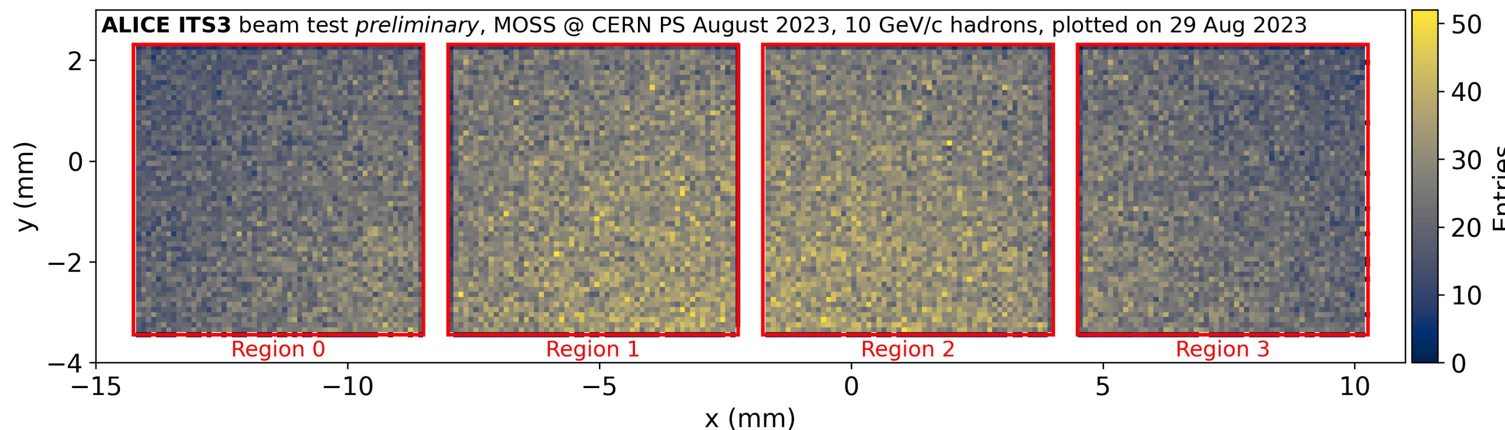
MOSS at Beam Test



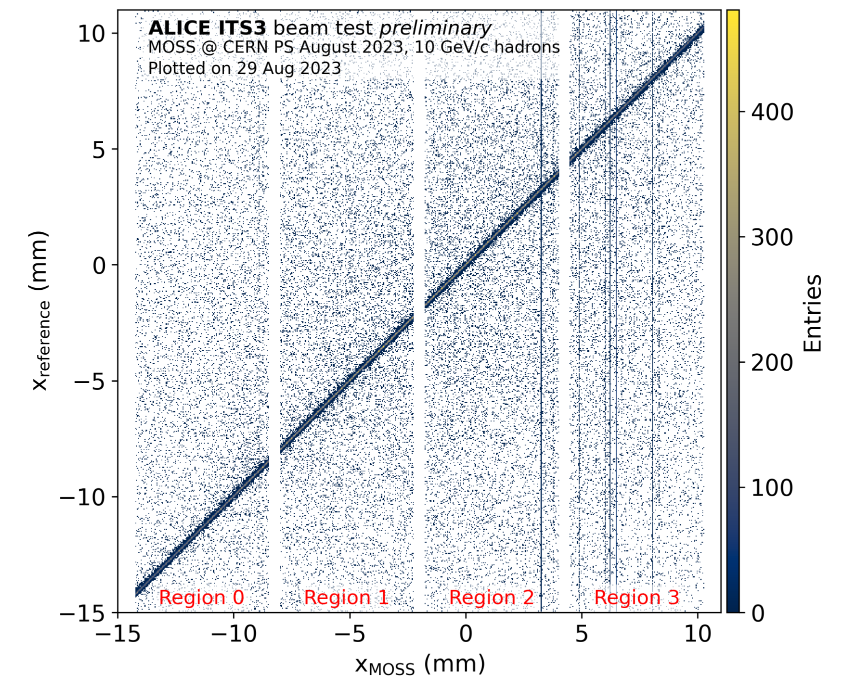
1 MOSS on Beam

- 2 Top Half Units
- 2 Bottom Half Units
- 16 Pixel Arrays

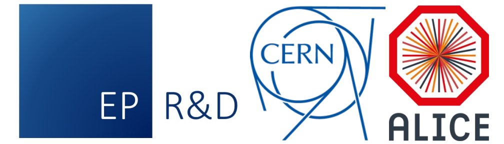
Hit Map (1 HRSU, 4 regions)



Hit x-coordinate correlation between MOSS and reference ALPIDE telescope



Summary



MOSS Monolithic Sensor Chip

Learned methodology, challenges and constraints

MOSS Test System

Complex test system. Developed dedicated hardware and procedures

Know-how on handling and testing wafer scale chips

Testing ongoing

MOSS design is functional

- Operation of full MOSS chips achieved
- Particles seen in beam tests

Studying powering, yield and wafer to wafer variations

Producing knowledge on design and handling of stitched MAPS

Tuesday

121. Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3
Chiara Ferrero (Universita e INFN T...
03/10/2023, 09:20

93. Model and analysis of the data readout architecture for the ITS3 ALICE Inner Tracker System
Manuel Viqueira Rodriguez (Universidad Politec...
03/10/2023, 12:00

99. Prototype of a 10.24Gbps Data Serializer and Wireline Transmitter for the readout of the ALICE ITS3 detector.
Arseniy Vitkovskiy (Nikhef National inst... , Dr Arseniy Vitkovskiy (Nikhef (the Dutch N..., Mr Marcel Rossewij (Utrecht University), Vladimir Gromov (Nikhef National inst...
03/10/2023, 13:40

Thursday

26. ALICE ITS3: a bent stitched MAPS-based vertex detector ← ITS3 Overview
Ola Slettevoll Groettvik (CERN)
05/10/2023, 11:20

89. Development of the data transmission architecture of the stitched sensor prototype towards the ALICE ITS3 upgrade
Piotr Andrzej Dorosz (CERN)
05/10/2023, 17:40

SPARE SLIDES

ITS3 LoI Layout and Requirements

3 Cylindrical layers

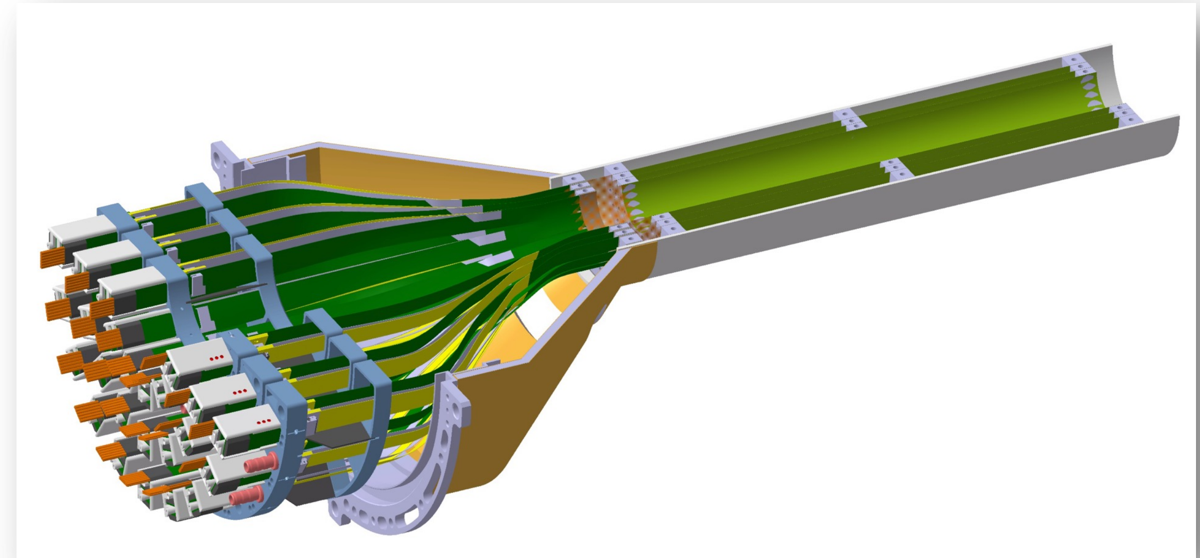
Made with **6 curved wafer-scale single-die** Monolithic Active Pixel Sensors

Radii 18/24/30 mm, length **27 cm**

Thinned down to **<50 µm**

Position resolution ~5 µm

-> Pixels **Θ(20 µm)**



Electro-mechanical integration

No flexible circuits in the active area

-> Distribute supply and transfer data on chip to the short edge

Cooling by air flow

-> Dissipate less than *20 mW/cm²* (in sensitive area)

Pb-Pb Interaction Rate	50 kHz
Particle Flux	$3.3\ \mathrm{MHz/cm^2}$
Integration time	< 10 µs
TID	<10 kGy
NIEL	1×10^{13} 1 MeV $n_{eq}\ cm^{-2}$

ALICE ITS3 LoI CERN-LHCC-2019-018 / LHCC-I-034

ER2 Stitched Sensor

Layer 0: 12 x 3 repeated units+endcaps

Layer 1: 12 x 4 repeated units+endcaps

Layer 2: 12 x 5 repeated units+endcaps

SEGMENT

97,82

78,256

58,692

19,564

21,666

259,992

Sensitive z-length

4,5

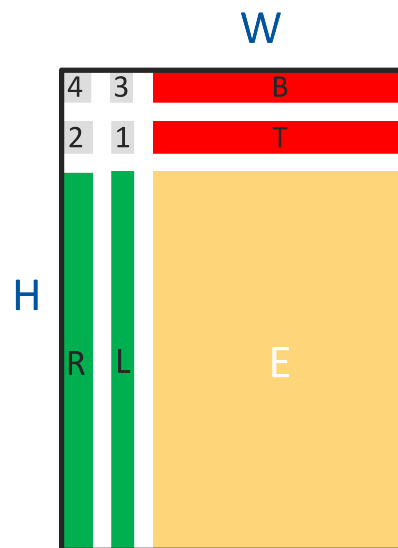
1,5

265,992

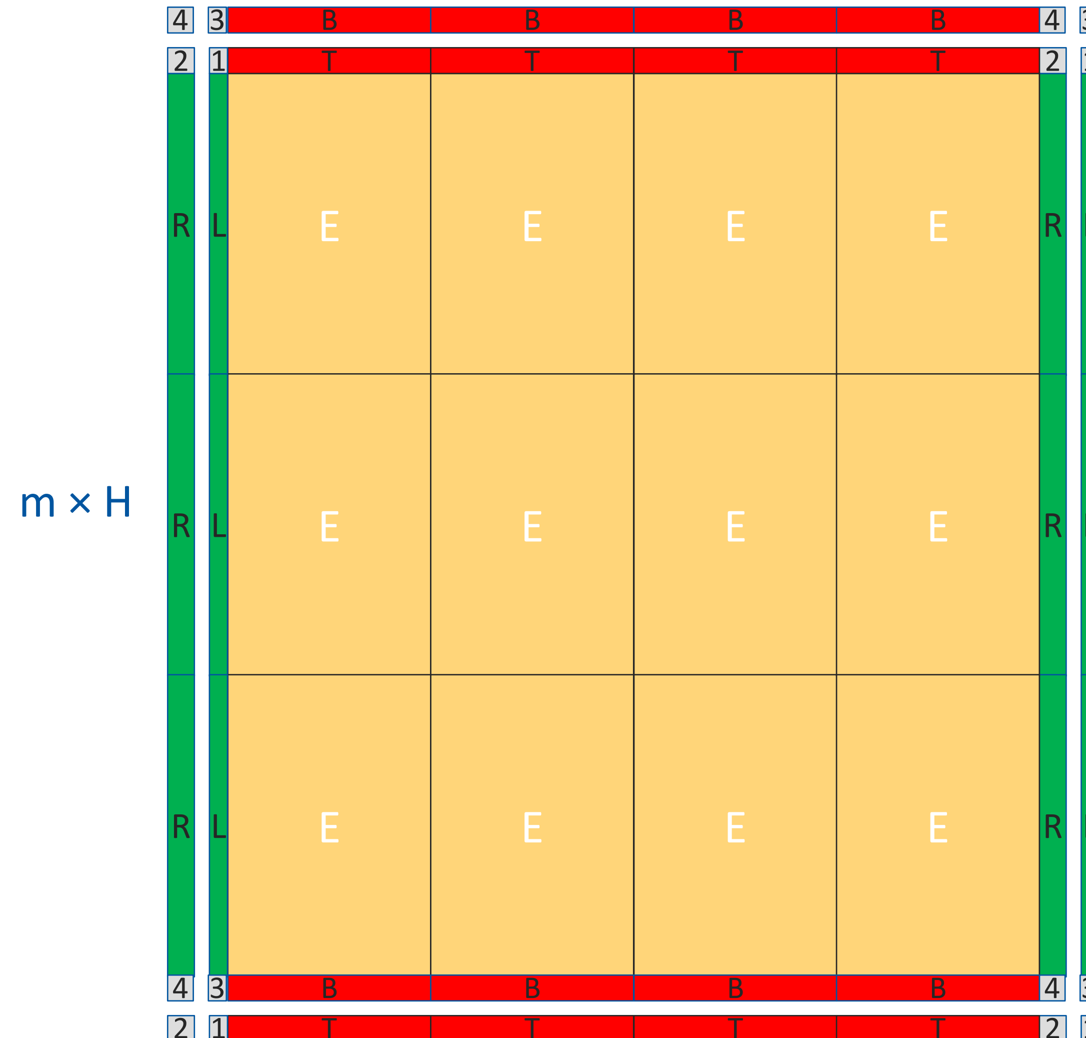
Physical z-length

Stitching

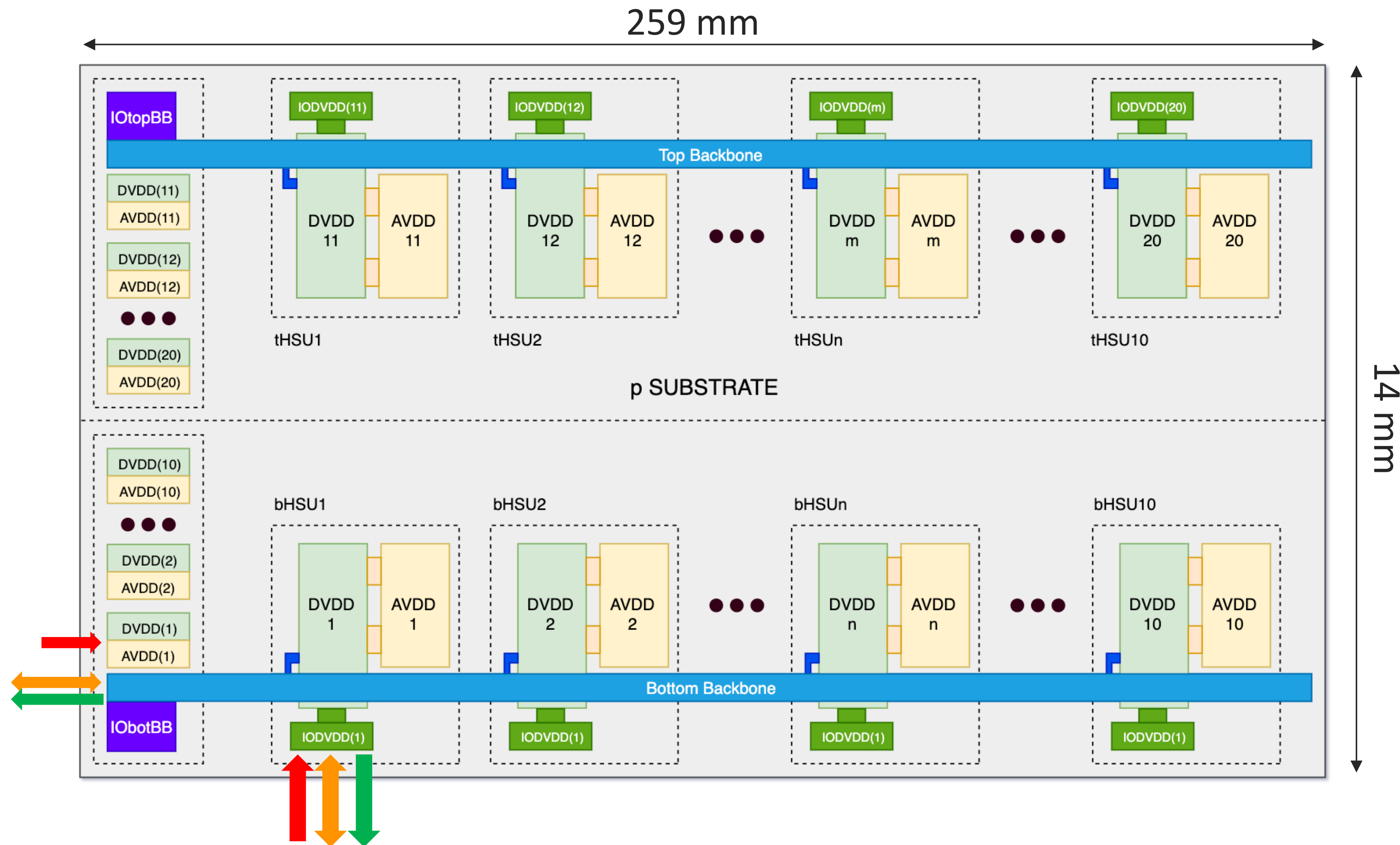
Design Reticle (typ. 2×3 cm)



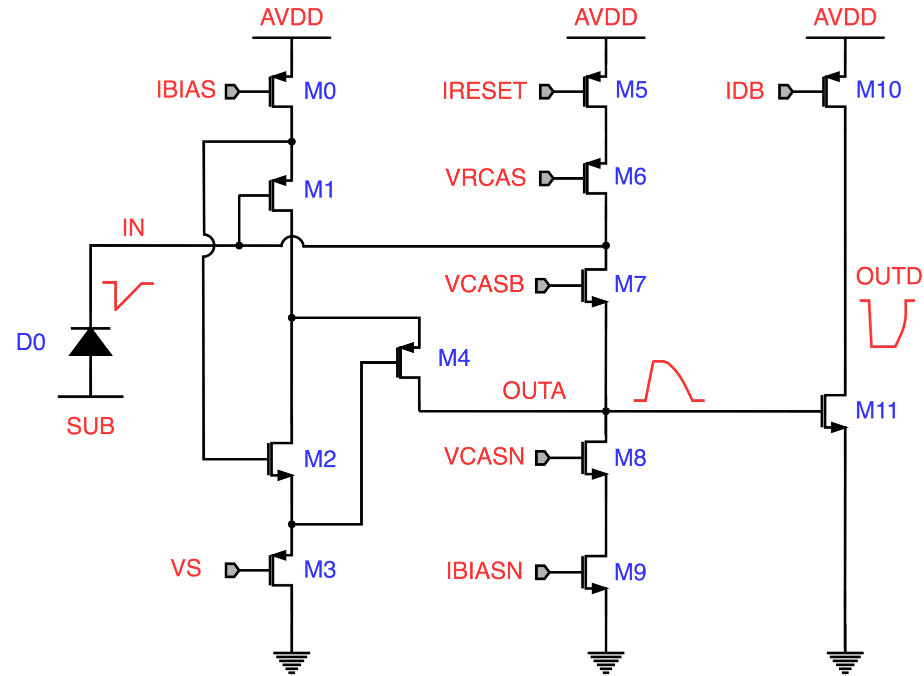
Circuits on wafer

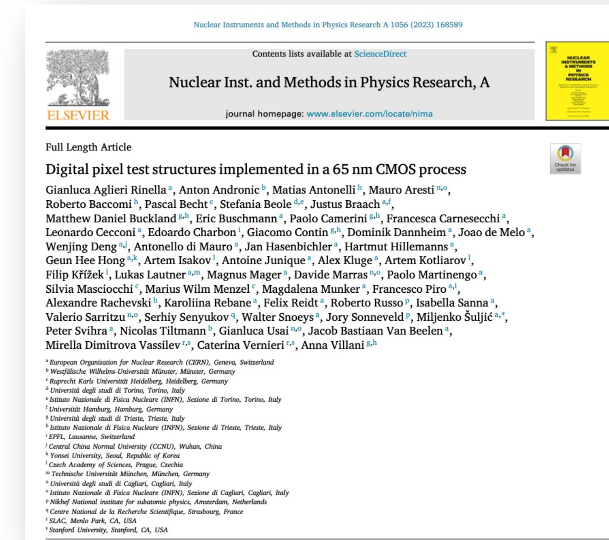


MOSS Power Domains and I/Os



MOSS Front-End





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Full Length Article

Digital pixel test structures implemented in a 65 nm CMOS process

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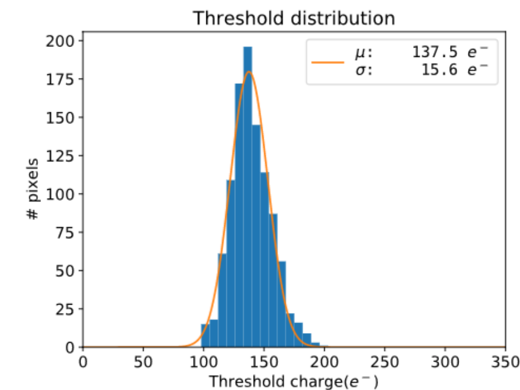
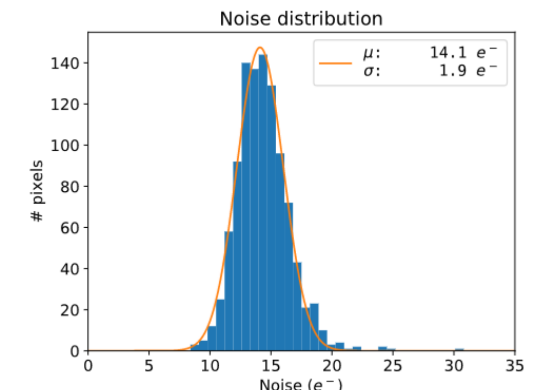
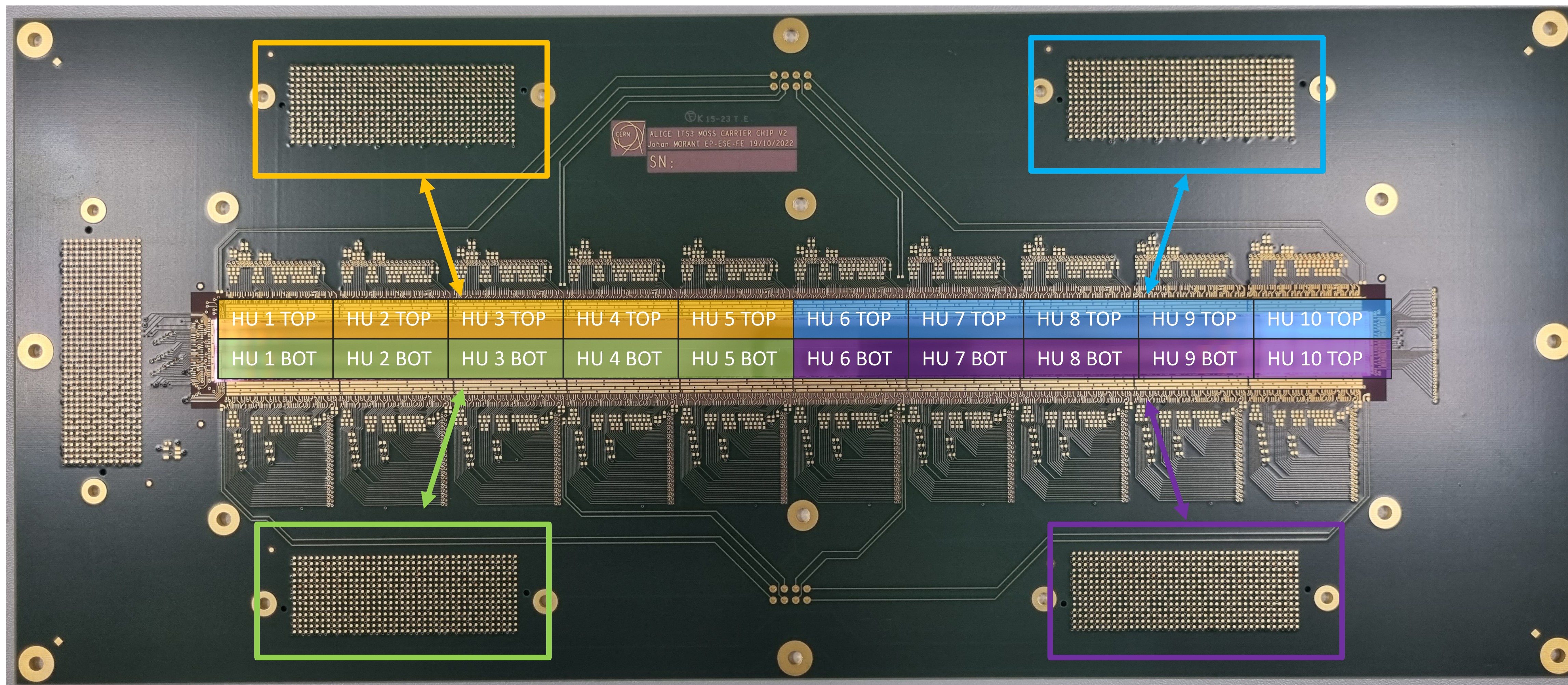
"Digital pixel test structures implemented in a 65 nm CMOS process", https://doi.org/10.1016/j.nima.2023.168589

Analog FE Area	60	μm^2
Nominal FE Power	30	nW
Analog Power Density	10	mW/cm^2
FHR	$<10^{-2}$	s^{-1} $pixel^{-1}$






ALICE ITS3 MOSS CARRIER CHIP V2
Johan MORANT EP-ESE-FE 19/10/2022
SN:
HU 1 TOP
HU 2 TOP
HU 3 TOP
HU 4 TOP
HU 5 TOP
HU 6 TOP
HU 7 TOP
HU 8 TOP
HU 9 TOP
HU 10 TOP
HU 1 BOT
HU 2 BOT
HU 3 BOT
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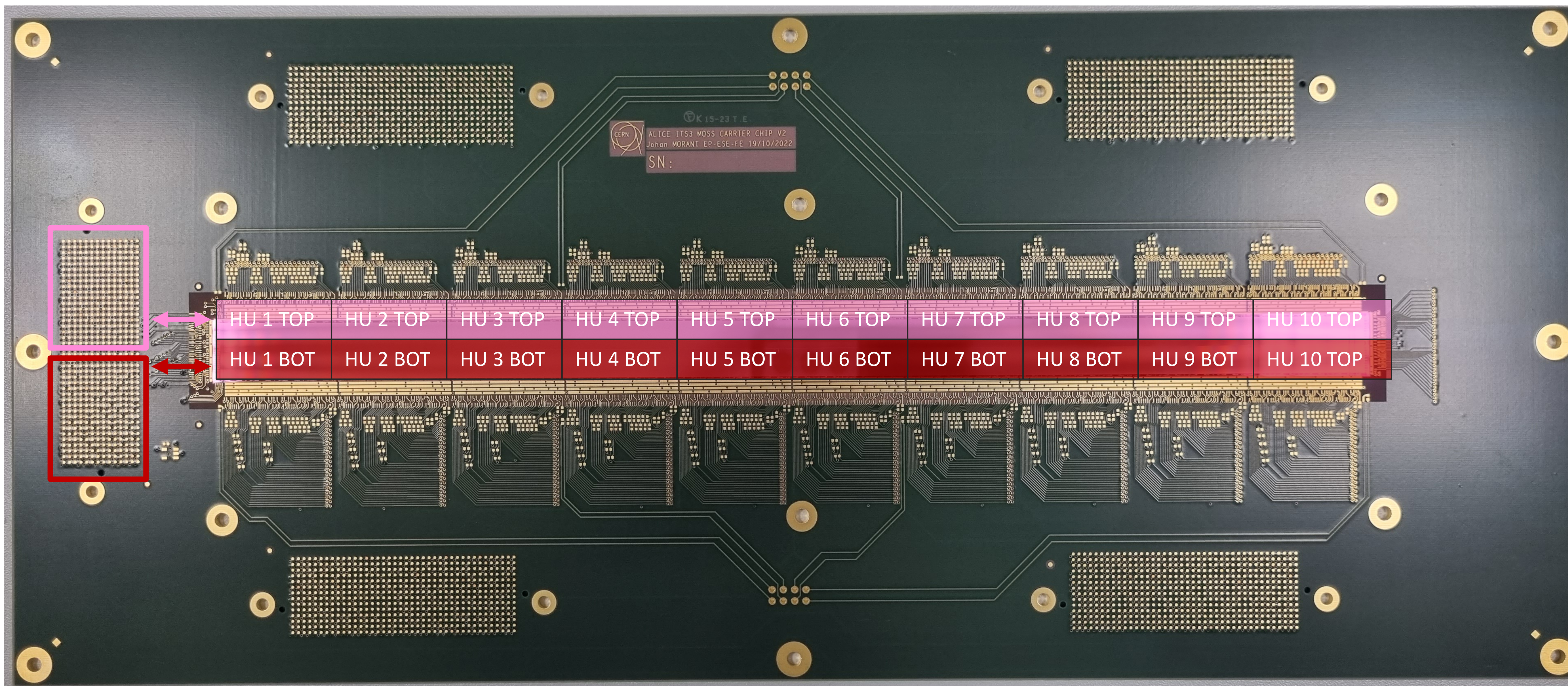
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HU 6 BOT
HU 7 BOT
HU 8 BOT
HU 9 BOT
HU 10 TOP
ALICE ITS3 MOSS CARRIER CHIP V2
Johan MORANT EP-ESE-FE 19/10/2022
SN:

ER1 Wafers and MOSS testing

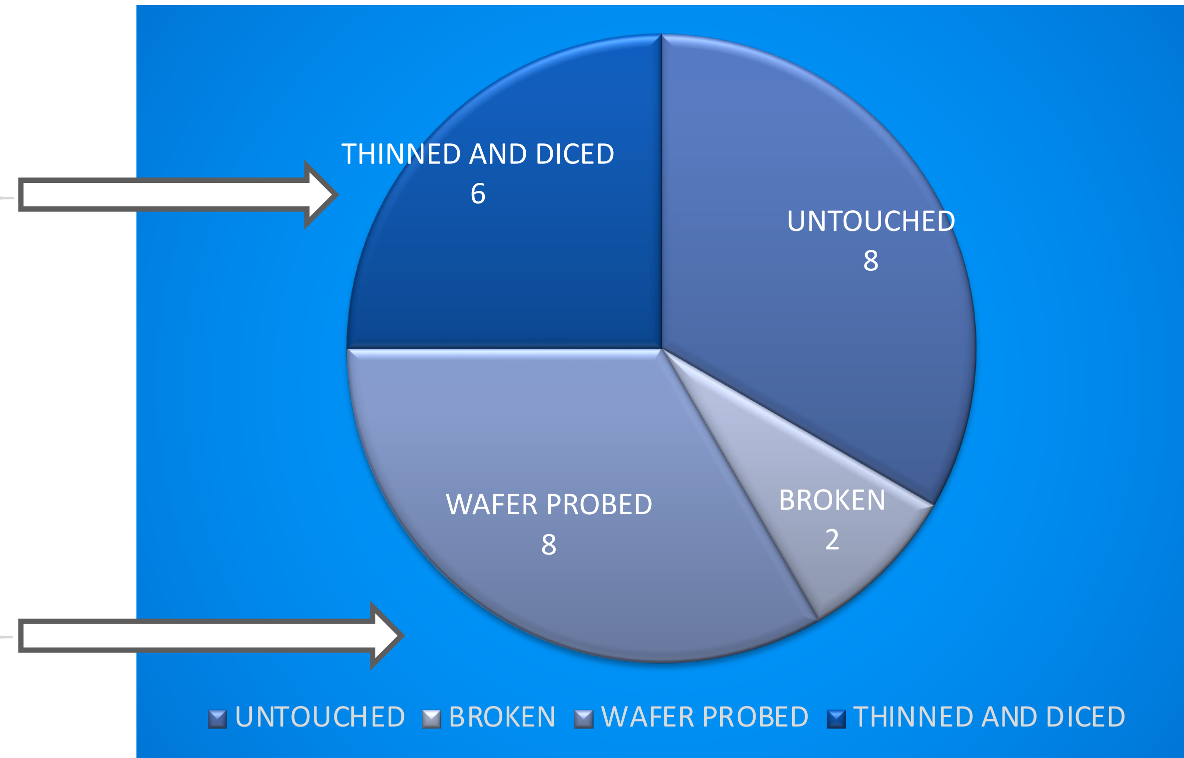
6 Wafers Thinned and Diced

- 3 Wafers Picked
- 16 MOSS on Carriers under test
  - +1 not bonded yet, +1 broken
- 3 Wafers On Hold (18 MOSS)

8 Wafers probed with Wafer Prober

- 48 MOSS + Single MOSS
- Impedance Tests

2 Wafers broke at Thinning and Dicing



Lot of 24 Wafers. Status September 2023

Sequential Power Scans Currents - Wafer 17