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The Monolithic Stitched Sensor (MOSS) Prototype for the ALICE ITS3 and First Test Results

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The MOSS (Monolithic Stitched Sensor) chip is a monolithic pixel prototype chip measuring \(\qty{25.9}{cm}\times\qty{1.4}{cm}\). It was designed to explore the stitching technique, to investigate the achievable yield and as a proof of concepts for the sensors for the ALICE ITS3 upgrade. It was manufactured in early 2023.

This submission will focus on the MOSS chip and on its testing. It will give an overview of the chip and describe the system developed to characterize it. It will report on the early experience of testing in the laboratory and include the first experimental results.

Summary (500 words)

The ALICE ITS3 upgrade project aims at replacing the three innermost layers of the current ALICE tracker during the LHC Long Shutdown 3. The new layers will be made with single die sensors implemented in a 65 nm CMOS Imaging Process and with dimensions up to \(\qty{266}{\milli m}\times\qty{92}{\milli m}\). This can be achieved using stitching, a technique to manufacture modular chips that are much larger than the design reticle. The sensors will be thinned below \qty{50}{\micro m} and bent as true half-cylinders.

The MOSS (Monolithic Stitched Sensor) chip is a monolithic pixel prototype chip measuring \(\qty{25.9}{\centi m}\times \qty{1.4}{\centi m}\) (fig. 1). It was designed in 2022 to explore stitching, to investigate the yield and as proof of concepts for the ALICE ITS3 sensor developments. Its manufacturing was completed in April 2023.

The MOSS chip is made abutting ten Repeated Sensor Units (RSU) of \(\qty{25.5}{\milli m}\times\qty{14}{\milli m}\) and two small end-cap regions at the two sides of the abutted RSUs. Each RSU is subdivided in two half-units. The top one contains four pixel arrays of \(256\times256\) pixels with a pitch of \(\qty{22.5}{\micro m}\) while the bottom unit contains four arrays of \(320\times320\) pixels with a pitch of \(\qty{18}{\micro m}\). The two halves differ for the densities of circuits and interconnects, in order to investigate the potential impact on yield of layout density. The MOSS chip contains 20 half units and 6.72 million pixels. It has 107 supply or biasing nets, 2192 bonding pads, 390 digital and 480 analog I/Os. The design contains interconnects crossing the stitching boundaries to transfer data over distances reaching

\qty{26}{cm}, entirely on die. Metal stripes of every power domain also traverse the stitching boundaries.

The testing of such a complex chip presented several challenges. There was no previous experience with the handling and bonding on carriers of chips of such dimensions. The supply domains, I/Os and internal blocks are remarkably numerous. At least few tens of samples need to be tested accurately to address questions related to yield quantitatively.

An electronic system was developed to enable the semi-automated testing of MOSS chips. This system consists of one large Carrier, 5 Proximity Boards and 5 Automation boards (fig. 2). The Carrier is a custom board with features to facilitate gluing and bonding of the chip. Die picking and wire bonding required adapting techniques and developing tools. The Proximity Board is a custom PCBA with many programmable components providing supplies, biasing and analog monitoring. The Automation board is a commercial FPGA based board. It interfaces to the lab host computer, to the Proximity Board and to the MOSS chip through it.

This submission will focus on the MOSS chip design, testing and the related challenges. It will describe the chip and the hardware system developed to characterize it. It will present the test plans and the first experience from testing in the laboratory. The first test results are expected to become available by the time of the workshop and will be included in the contribution.

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