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Design and Characterization of a precision tunable time delay integrated circuit.

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We present a design of a time delay circuit that we have developed for future applications in particle physics experiments. Our circuit has a dynamic range of 250 ps achieved in steps of 270 fs. The chip was fabricated in TSMC's 65 nm LP process and consists of an array of planar waveguides for fine control and LC lumped circuits for large scale delays. We will report on detailed characterization of the device including some recent results from radiation tests.

Summary (500 words)

Precision timing measurements is and will be a major tool at the HL-LHC and at future high energy facilities. The requirement of precision clock distribution and stabilization will be a major challenge as we extend our physics requirements to the picosecond or sub-picosecond levels. We have developed an integrated dual channel digitally controlled phase shifter circuit with a step size of ˜270 fs and a dynamic range of ˜250 picoseconds. The concept we use in this design is based on tunable delay-line phase shifters first used for developing accurate beam control in large scale arrays for 5G mm-wave base stations. In this work we have adopted this core technique and transformed it into an architecture that fits the needs of precision time delay. Fine delay precision and large dynamic range are typically at odds as one requires fine unit cells and stacking a large number of them for dynamic range comes at the cost of unbearable signal attenuation and area. To address this trade-off we incorporate a two-tier tuning mechanism that enables both high precision and large dynamic range. First, a coarse set of delay cells biases the delay within the range close to the target delay value. Next, a set of transmission line-based delay lines fine-tune this delay with sub-picosecond delay steps and produces the target delay within <270 fs of accuracy. We designed and fabricated a prototype of this tunable delay line in the TSMC 65nm LP process. The chip area is 1mm × 1.9mm and consists of two tunable delay lines and a radiation tolerant I2C interface for digital control of the delay cells. The passive construction of the delay line creates delay values that primarily depend on the physical distances between metal structures on chip. Such distances can be accurately fabricated with nano-scale accuracy resulting in reliable and accurate delay values. The passive nature of this delay line also has the benefit of zero DC power. There is good agreement between EM simulation results of the delays and board level delay measurements of the fabricated chip. We will report on results obtained with this device, that include linearity, signal quality, dispersion, and radiation tolerance. The attached image shows our measurements of the fine delay steps.

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