Test results of ECON-D and ECON-T, the concentrator ASICs for the HGCAL front-end readout

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Fermilab

CMS Compact Muon Solenoid

ECON team and contributors

The ECON design team

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CERN: Gianmario Bergamin, Davide Ceresa, Szymon Kulis, Matteo Lupi, Simone Scarfi'

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Thanks to the lpGBT team

eRX: Di Guo (SMU), Datao Gong (SMU), Jingbo Ye (SMU),Paulo Moreira (CERN)

ePortRxGroup (phaseAligner, ePortRx): Dongxu Yang (SMU), Szymon Kulis (CERN), Datao Gong (SMU), Jingbo Ye (SMU), Paulo Moreira (CERN)

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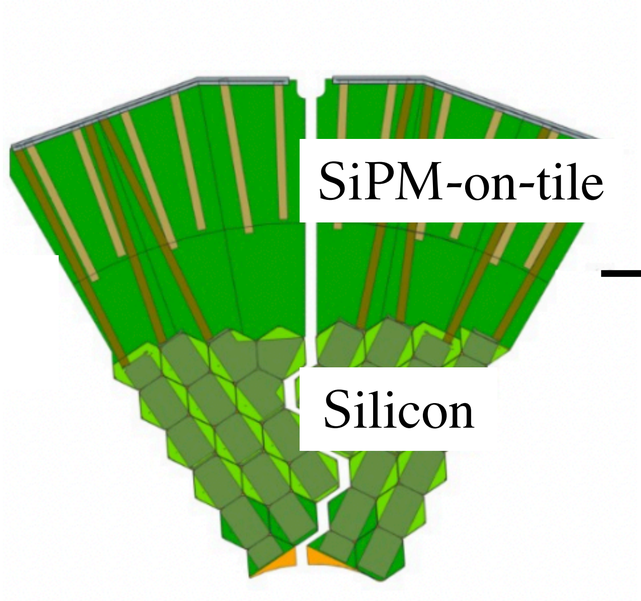
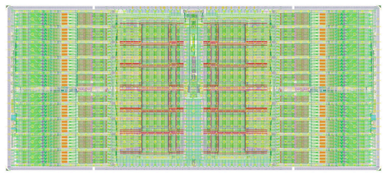
eTX: Paul Jozef Leroux (KUL), Bram Feas (KUL), Paulo Moreira (CERN)

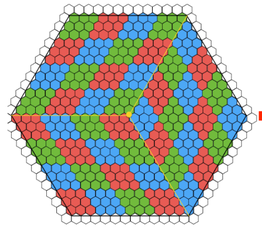
Thanks to the hls4ml team

Concentrating readout data in the HGCAL front-end readout





HGCROC
readout ASIC

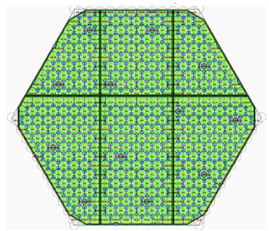


ECON-T

To L1Trigger

Trigger
Decision
< 15us

Trigger Data
charge sums



Accept

Discard

DAQ Data
charge, time

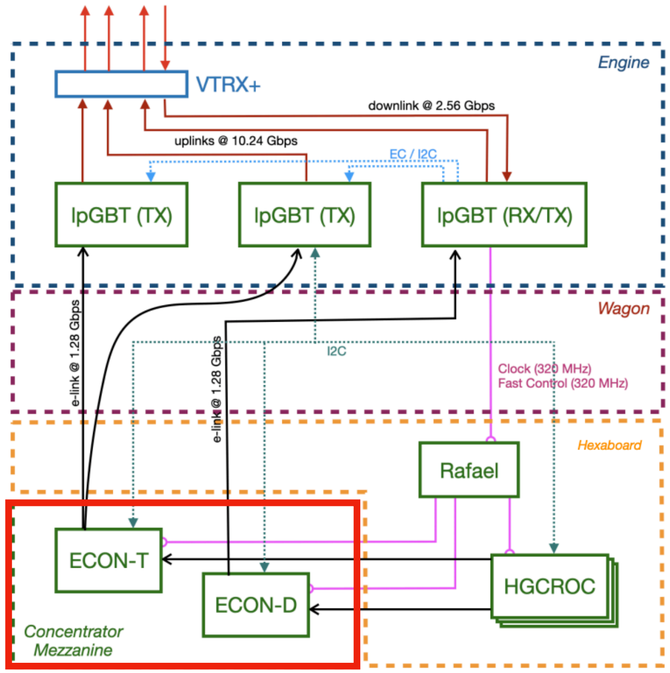
ECON-D

To DAQ

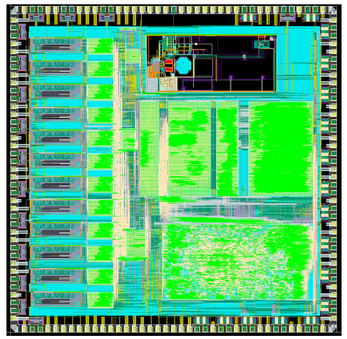
Trigger Path Stage	# channels	bits/ch	Compression	Rate	# links*
Raw data	6M	20	×1	5 Pb/s	1M
HGCROC (hardware)	1M	7	×1	300 Tb/s	60k
Threshold (ECON selection)	1M	7	×7	40 Tb/s	9k

*Assumes 40MHz rate and 50% link packing efficiency (7 used on each lpGBT => 10.24 Gbps)

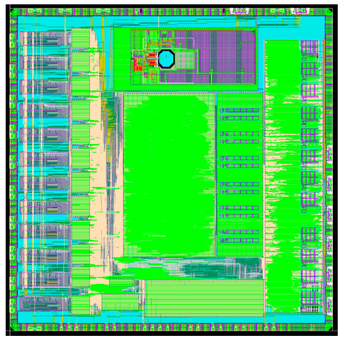
ECON requirements in the front-end



Example: front-end architecture for LD silicon



ECON-T-P1
5.19 x 5.19 mm^2



ECON-D-P1
5.315 x 5.315 mm^2

Parameter	Specification
ECON-T Latency	$\leq$0.4 µs
Power Consumption	$\leq$ 2.5 mW/channel (each)
Voltage range	1.2 V $\pm$ 10%
Number of input/outputs	12 inputs, 6-13 outputs @ 1.28 Gbps
Total Ionization Dose	200 Mrad
SEE tolerance	Hadron fluence ($E > 20$ MeV) of 1×10^{14} cm^{-2}*

ECON-T

Reduces # of links by selecting charge data @ 40 MHz

Physics performance of compression algorithms is key!

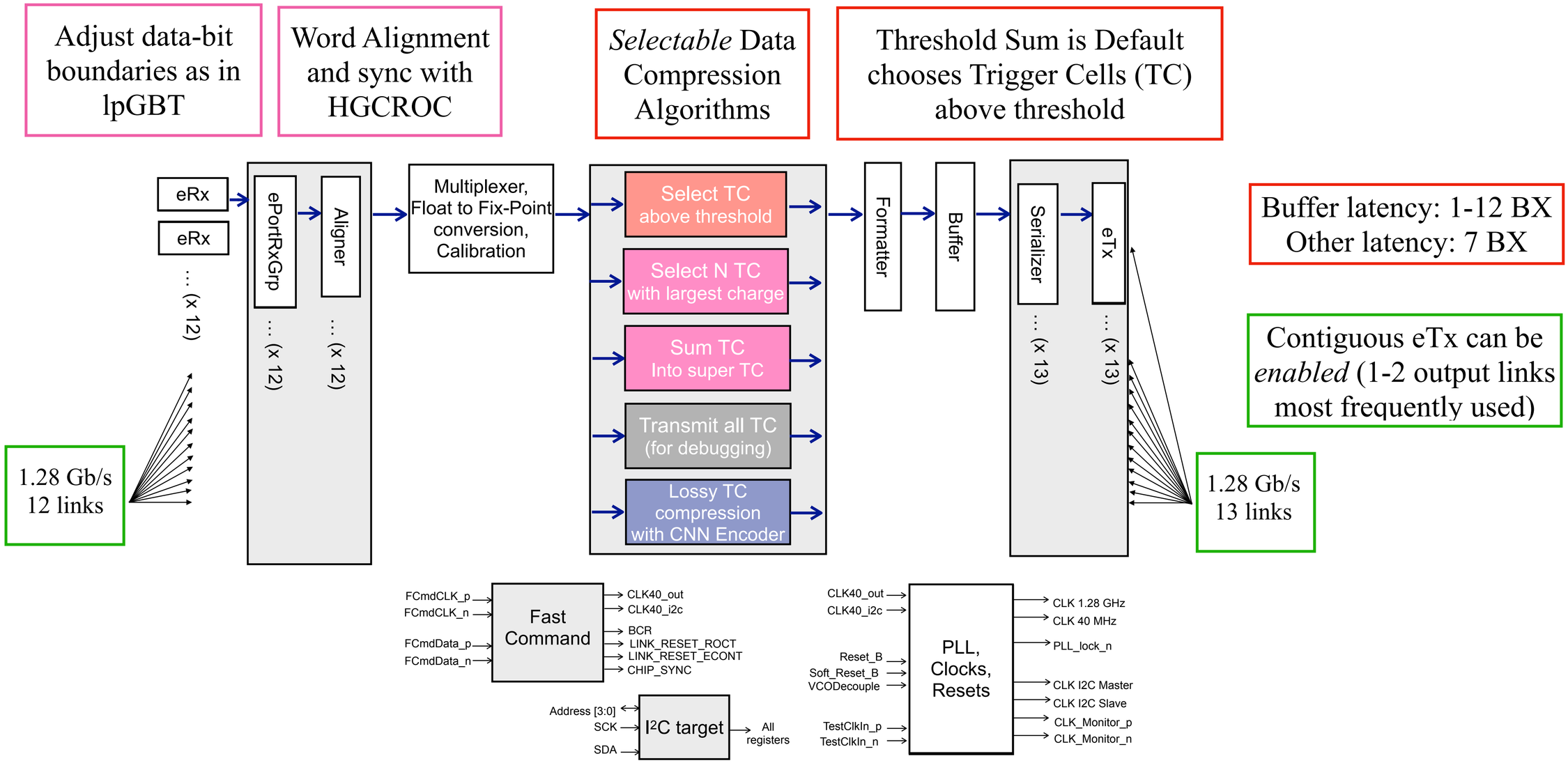
ECON-D

Zero-suppression, time-analysis of error conditions, data-packet building @ 750kHz

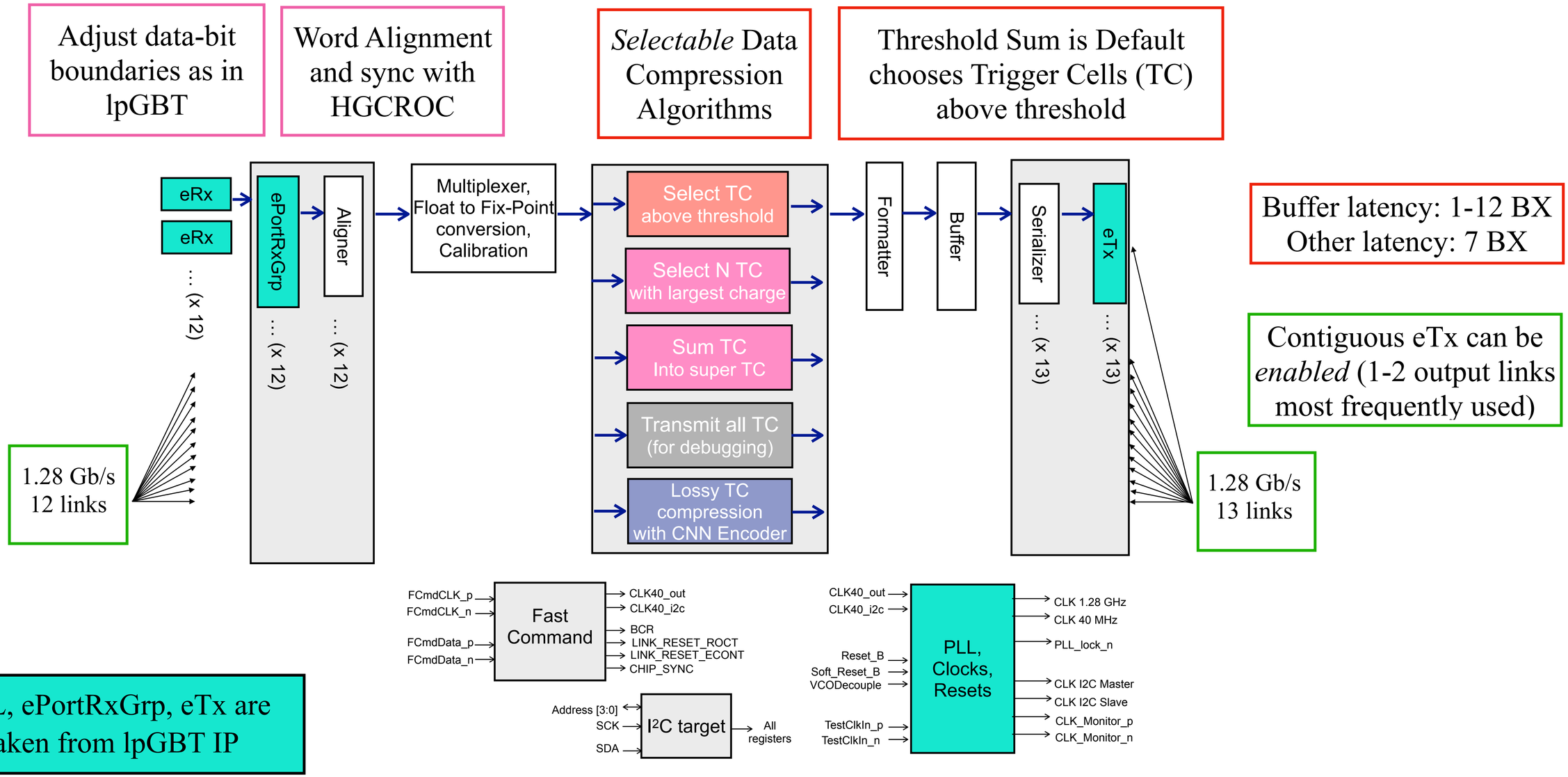
More susceptible to loss of sync (e.g. via SEE)

*average over entire detector

ECON-T block architecture



ECON-T block architecture

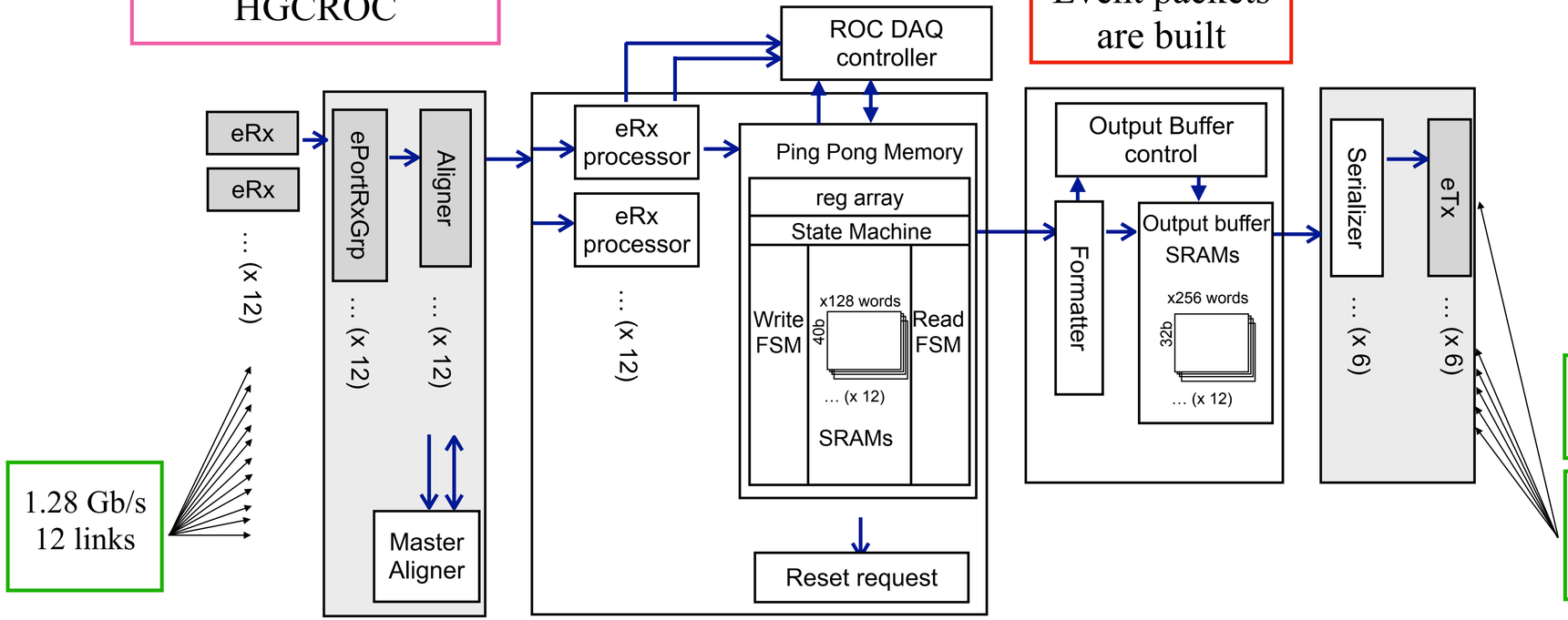


ECON-D block architecture

Each input handles data from one-half of HGCROC

All active eRx streams are synchronized

Event packets are built



1.28 Gb/s
12 links

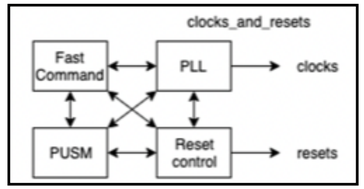
Any inputs/outputs can be active or inactive

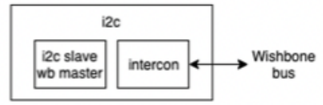
1.28 Gb/s
6 links

Channel data is processed *(and zero-suppressed)* and stored in a pingpong SRAM

Reset Requests if systematic problems are found

Staggered writing/reading to 12 channel SRAMs



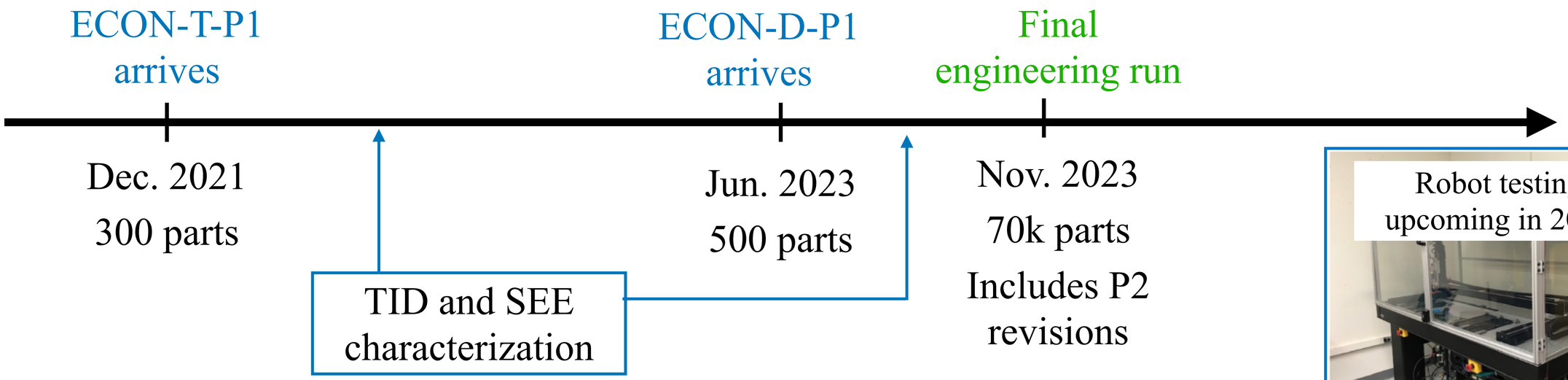


Single 40 MHz clock: core logic uses only clocks produced by PLL

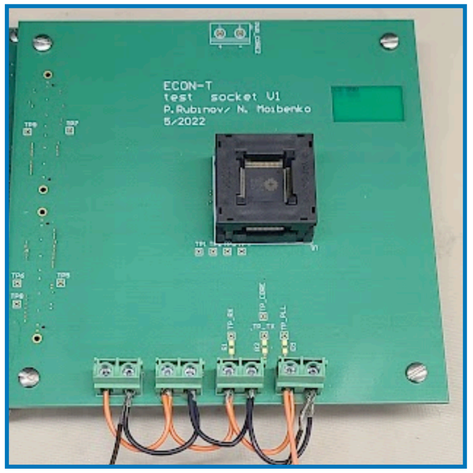
PUSM and serializer improved design

Shared blocks between ECON-T and ECON-D

Testing Overview



- Focus on results from ECON-D-P1:
  - External IP remains the same as in ECON-T-P1
  - Common blocks are updated and will be used in final ECON-D and -T.
- **Comprehensive bench testing of both chips reveals no major issues**
  - Tested in radiation environment, voltage range and low temperature (-20°C)
  - Tested unpackaged and packaged chips (128 pin LQFP packaging)



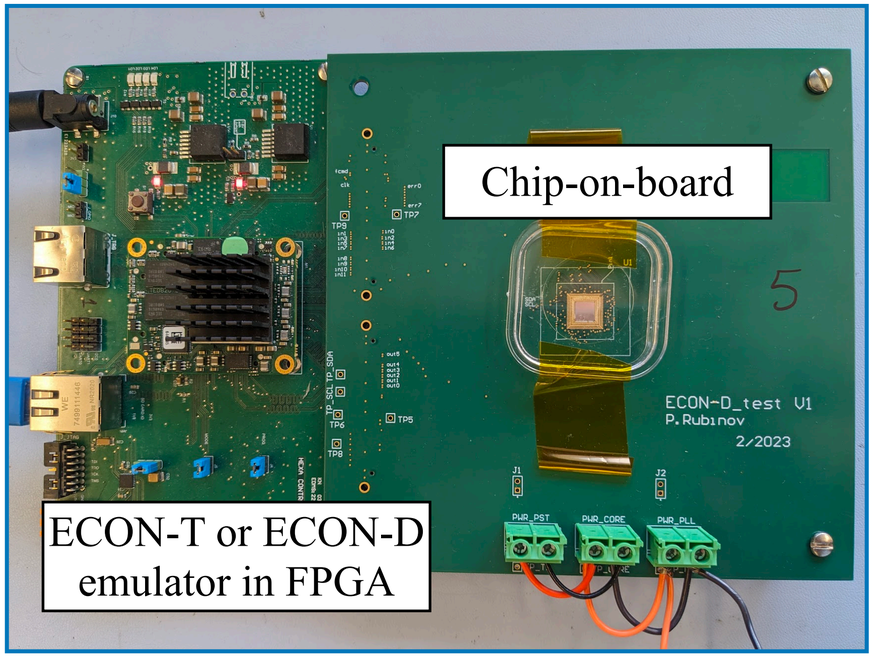
Emulator-based testing

Validate main functionality via **data stream comparison**:

- ASIC output compared bit-for-bit in real time to emulator output
- emulator validated against spec. and independent python-based emulation of behavior

Drives inputs to ECON chips (with HGCROC format)

Fast commands, slow control and input clock provided by FPGA



ECON powered at 1.2V with external power supply

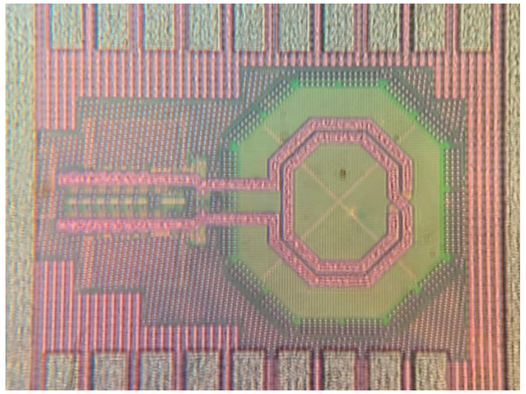
Block	Functionality test
I^2C	Write and readback registers
PUSM	PLL locking
	DLL locking
Fast control	Fast command response
ePortRxGrp	Bit alignment
Aligner	Synchronization with HGCROC
	Stability over time
ECON-T-P1 main functionality	Compression algorithms for many configurations (e.g. # of links)
ECON-D-P1 main functionality	Event packet building
	L1A response

PLL performance

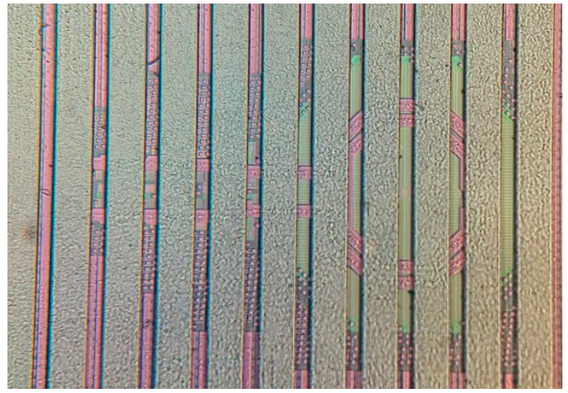
ECON uses **lpGBTv1 PLL based on LC-tank VCO with adaptations** for ECON's 9-layer metal stack

ECON-D-P1: Extra AP metal layer over PLL reduces magnetic flux through VCO's inductor and increases the frequency of the VCO

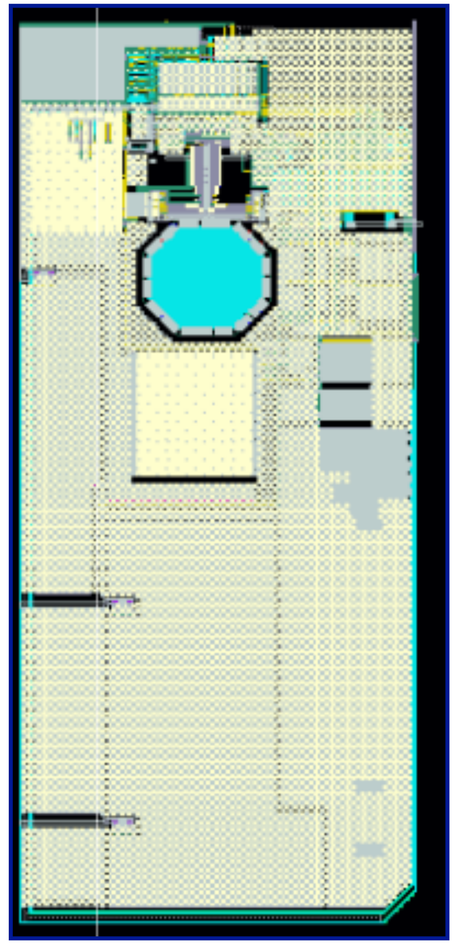
- PLL locking range ~ 41.5-49 MHz (does not lock at 40 MHz)



ECON-T-P1



ECON-D-P1



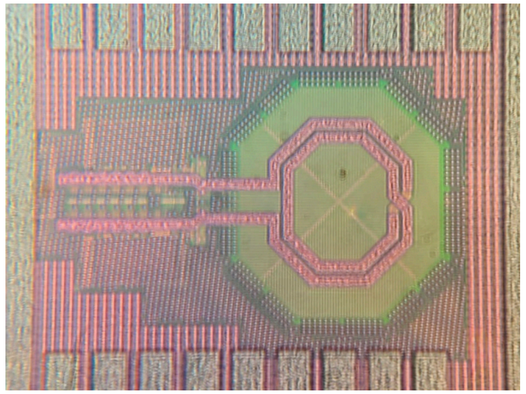
PLL design for ECON-D-P1 and ECON-T-P1

PLL performance

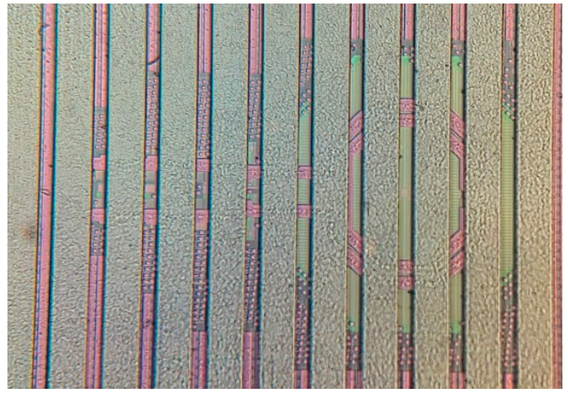
ECON uses **lpGBTv1 PLL based on LC-tank VCO with adaptations** for ECON's 9-layer metal stack

ECON-D-P1: Extra AP metal layer over PLL reduces magnetic flux through VCO's inductor and increases the frequency of the VCO

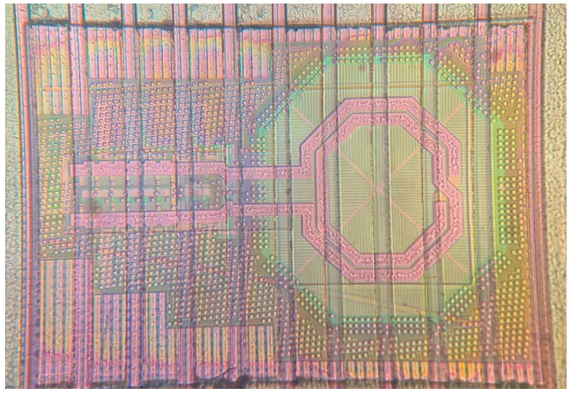
- PLL locking range ~ 41.5-49 MHz (does not lock at 40 MHz)
- Removal of extra layer (e.g. via focused ion beam FIB) recovers locking range (at 40 MHz)



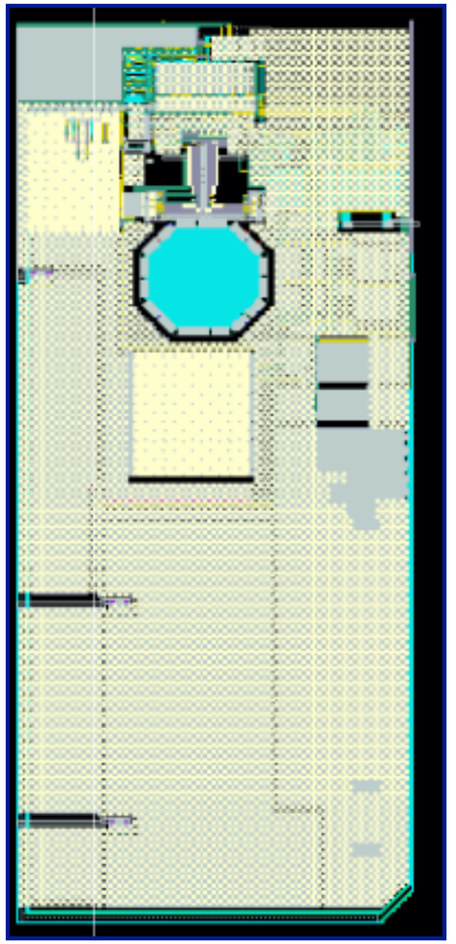
ECON-T-P1



ECON-D-P1



ECON-D-P1 FIB

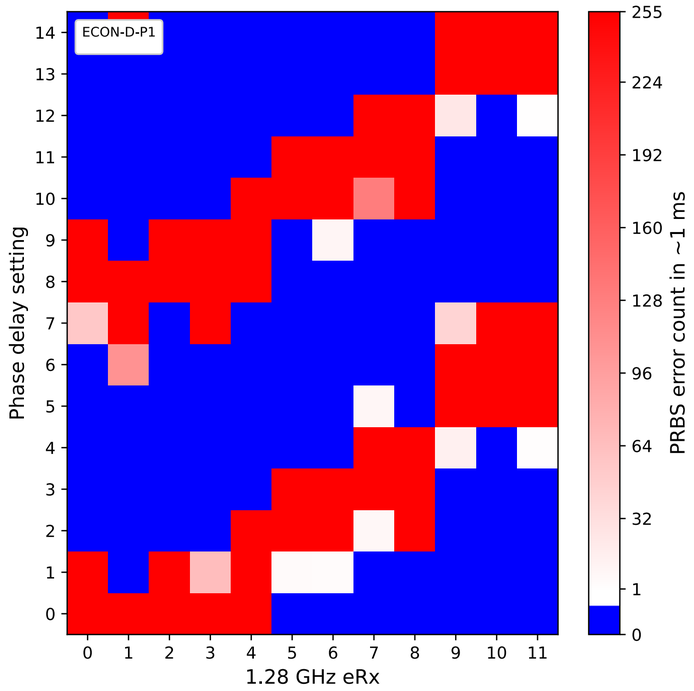


PLL design for ECON-D-P1 and ECON-T-P1

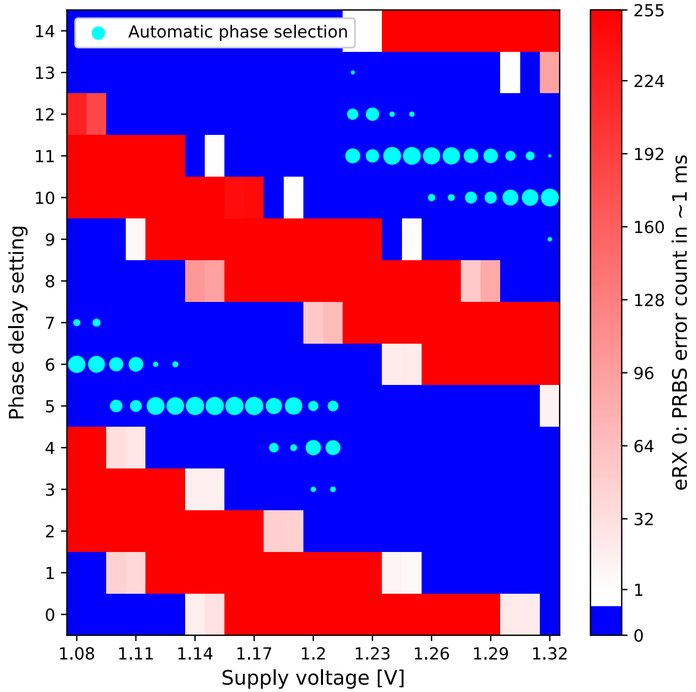
Phase alignment in ePortRx

- ePortRx: Internal check of PRBS 32-bit word errors as the phase delay setting* changes manually.
  - FPGA-related jitter reduces width of good phase region
  - Similar results obtained for ECON-T-P1 and ECON-D-P1
- **Automatic modes of phase selection** (e.g. continuous phase tracking) **select in the error-free region.**

Wide error-free region



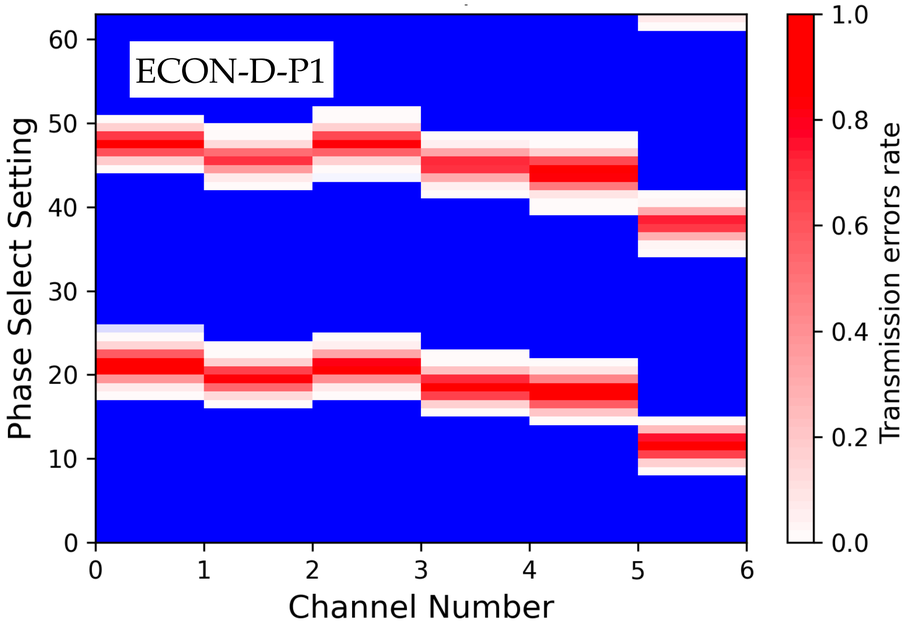
Good automatic phase selection over supply voltage

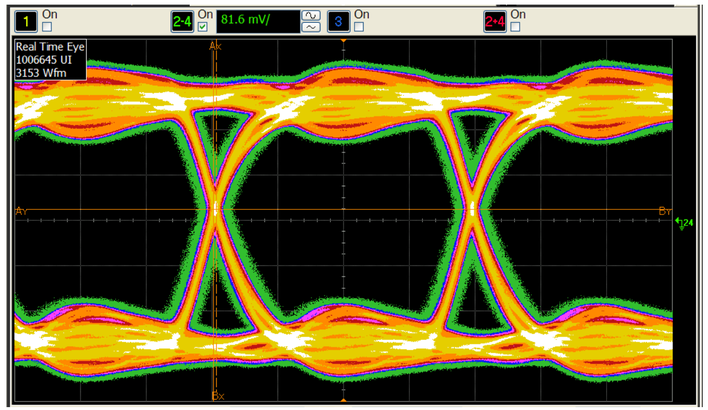


* Each phase setting adds a delay of 97.7 ps

Data output and jitter measurements

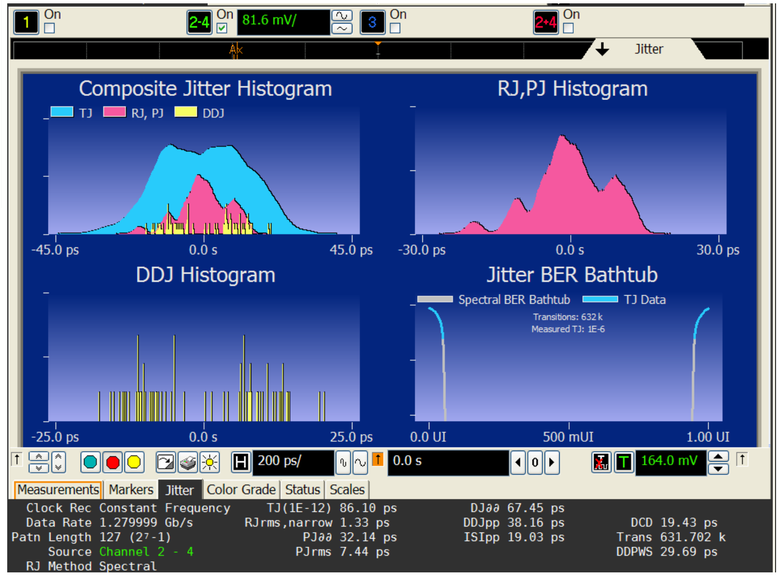
- QC characterization: each eTx routed to the test board via 2 programmable delay lines in the FPGA: scan over output delay settings.
  - Test also allows to detect issues in FPGA links in the test system.
- Jitter meets specification requirements (<15 ps)





Eye diagram @ 1.28 Gbps, eTx=1 ECON-D-P1

Random jitter: ~ 1.3 ps (RMS)

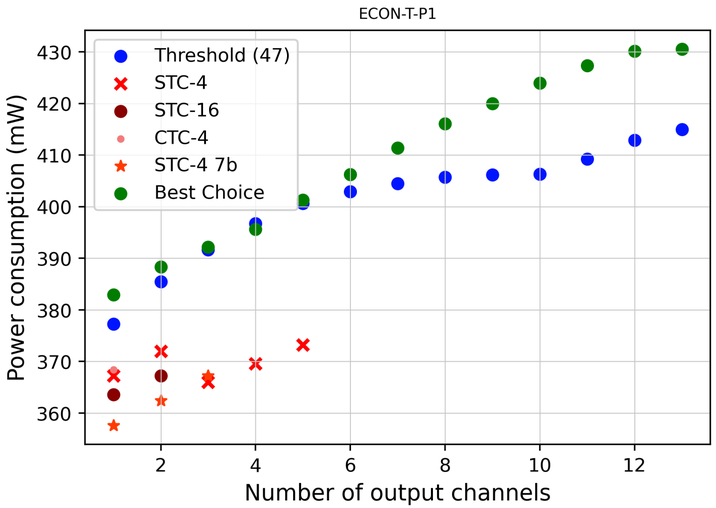


Cleaner jitter measurement obtained with external reference clock (not FPGA)

Early QC testing the ECON ASICs

Power consumption @ 1.2 V

Varies with number of output channels, algorithm (ECON-T), L1A rate (ECON-D) and buffer occupancy



- ECON-T-P1: Nominal 380 mW, Max 450 mW
- ECON-D-P1: Max 400 mW
- Adheres to specification: < 2.5 mW per channel

Early QC testing the ECON ASICs

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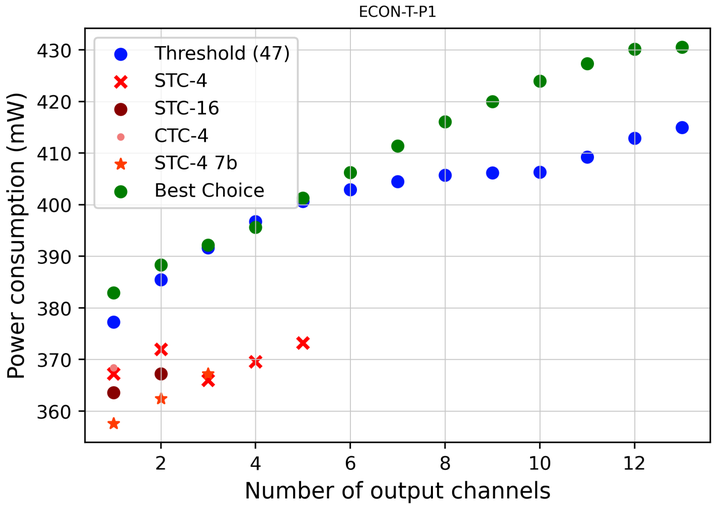

First QC tests for ECON-T-P1

O(200 packaged parts)

Test	# Failed	Yield
Power draw	0	100%
I^2C Read and write	1	$> 99\%$
PLL locks	3	$> 97\%$
eRx/eTx eye width, test-bench issues*	4-11	$91 - 96\%$

ECON-T-P1 QC test (180 parts)
*characterization in progress

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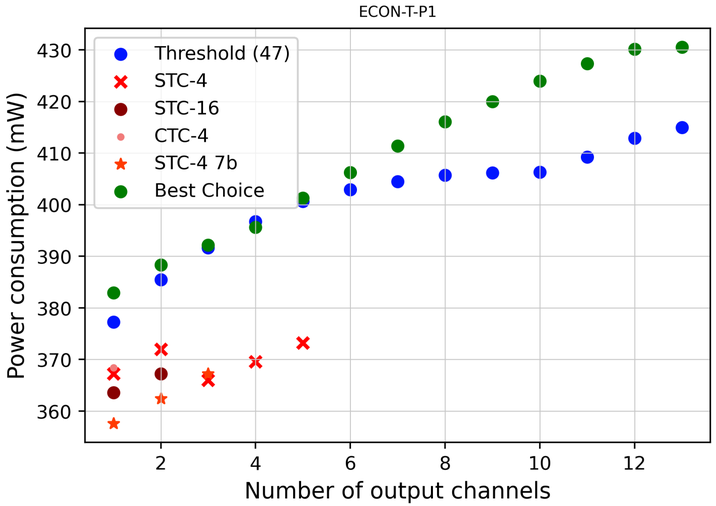

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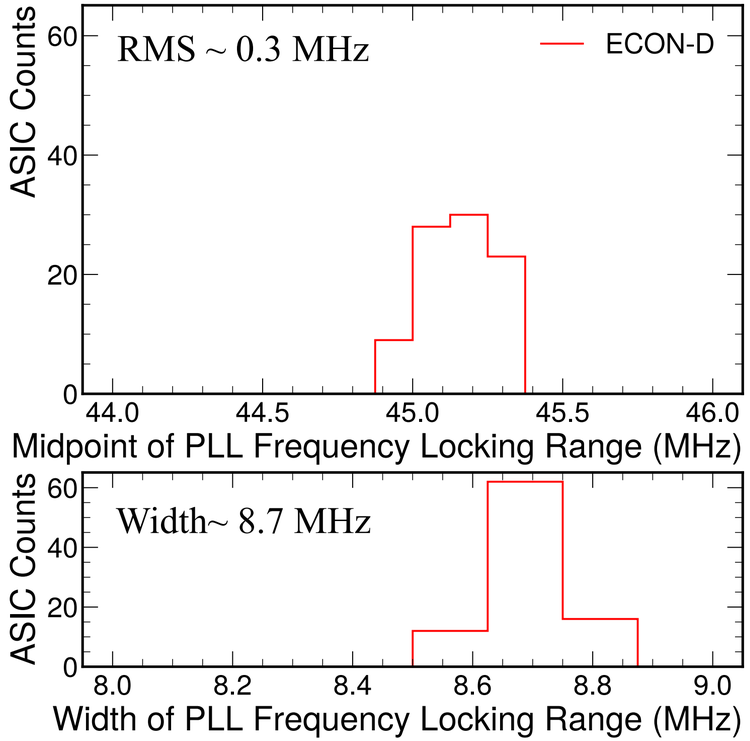
ECON-T-P1 QC test (180 parts)
*characterization in progress

PLL locking range for ECON-D-P1 (non-FIB)

O(100 packaged parts)



- ECON-T-P1: Nominal 380 mW, Max 450 mW
- ECON-D-P1: Max 400 mW
- Adheres to specification: < 2.5 mW per channel

Radiation hardness and SEE protection

- 65 nm LP process.
- ECON-D-P1:
  - All blocks (except SRAMs) are fully triplicated (registers, voters, clocks)
  - Use hamming code to protect byte 0 in SRAMs (determines output frame size)
- ECON-T2 and ECON-D2 will have identical periphery and TMR (following ECON-D-P1)

	Total Bytes	TMR	Auto-Correct	ECC
ECON-T-P1				
Data		FF	No	No
I^2C peripheral	675 bytes	FF	Yes*	Yes
I^2C (NN Encoder)	1608 bytes	FF, logic, clock	Yes*	No
ECON-D-P1				
All blocks (except SRAM)		FF, logic, clock	Yes	No
I^2C	8292 bytes	FF, logic, clock	Yes	No

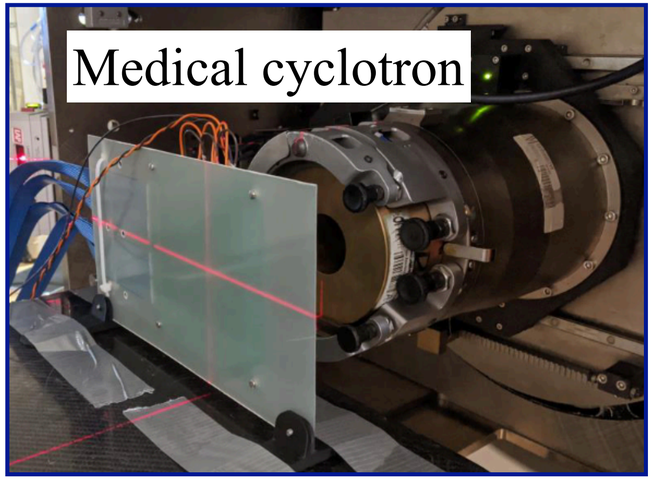
Error-Correction-Codes (ECC) only included for ECON-T-P1

TMRG-based flow for ECON-D-P1

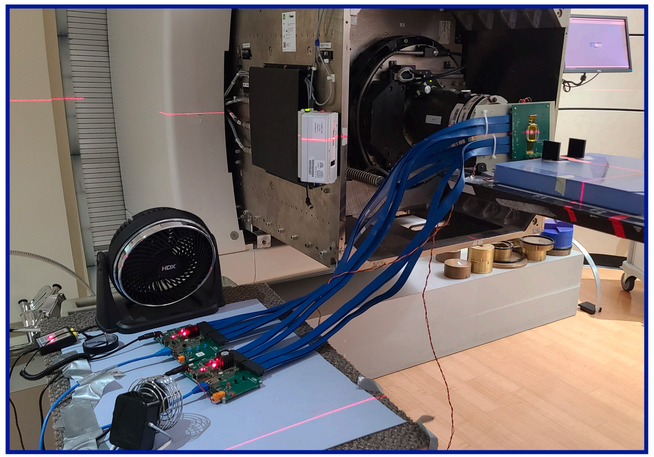
https://tmrg.web.cern.ch/tmrg/

*TMR refresh runs at 156kHz which is one correction every 6.4 us, or once per spill

Single Event Effect testing



1 ECON-T-P1 tested May 2022



2 ECON-D-P1 tested Aug 2023

2 separate campaigns for ECON-T/ECON-D:

- Beam: 217 MeV **protons**
- HGCAL requirement: 1e14/cm^2 high energy hadrons
- Observations:
  - No misbehavior requiring reset and no SEU in I^{2}C registers, for both ECON-T and ECON-D.
  - Set upper limit on cross section of errors requiring reset.

	Flux (/cm^2/s)	Fluence (/cm^2)	σ_{reset} (cm^2/ECON) 95% CL limit	Period$^{**}_{\text{reset}}$ (min./error) 95% CL limit
HL-LHC expected*	3×10^6	1×10^{14}		
ECON-T-P1 (May. 2022)	5×10^9	4×10^{12}	$< 7.45 \times 10^{-13}$	> 0.8
ECON-D-P1 (2 × Aug. 2023)	3×10^{10}	1×10^{14}	$< 3 \times 10^{-14}$	> 13
		5×10^{13} (per chip)		

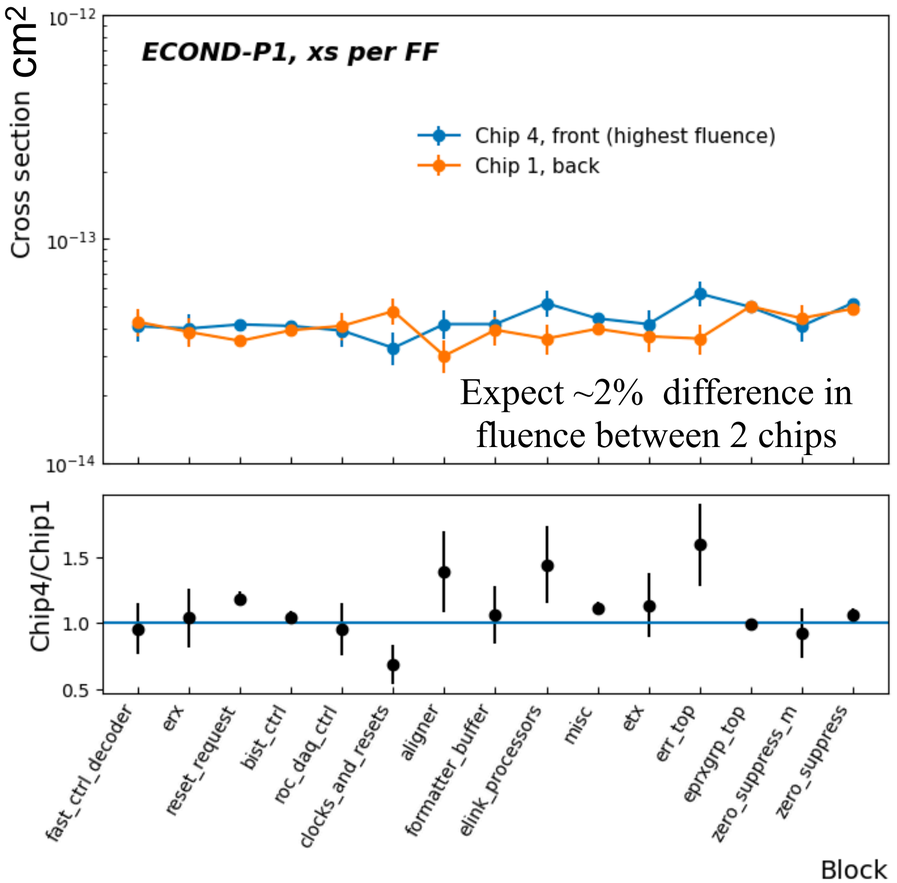
* averaged over all HGCAL
** for entire HGCAL : 27k ECON-D, 20k ECON-D

Limit on period between errors requiring reset: better for ECON-D-P1 because of larger test fluence.

Single Event Effect testing

- ECON-D-P1: estimated bit error cross section from internal monitoring of TMR counters

Cross section per bit for pre-voted FF
$\sim 3 \times 10^{-14}$cm^2/FF

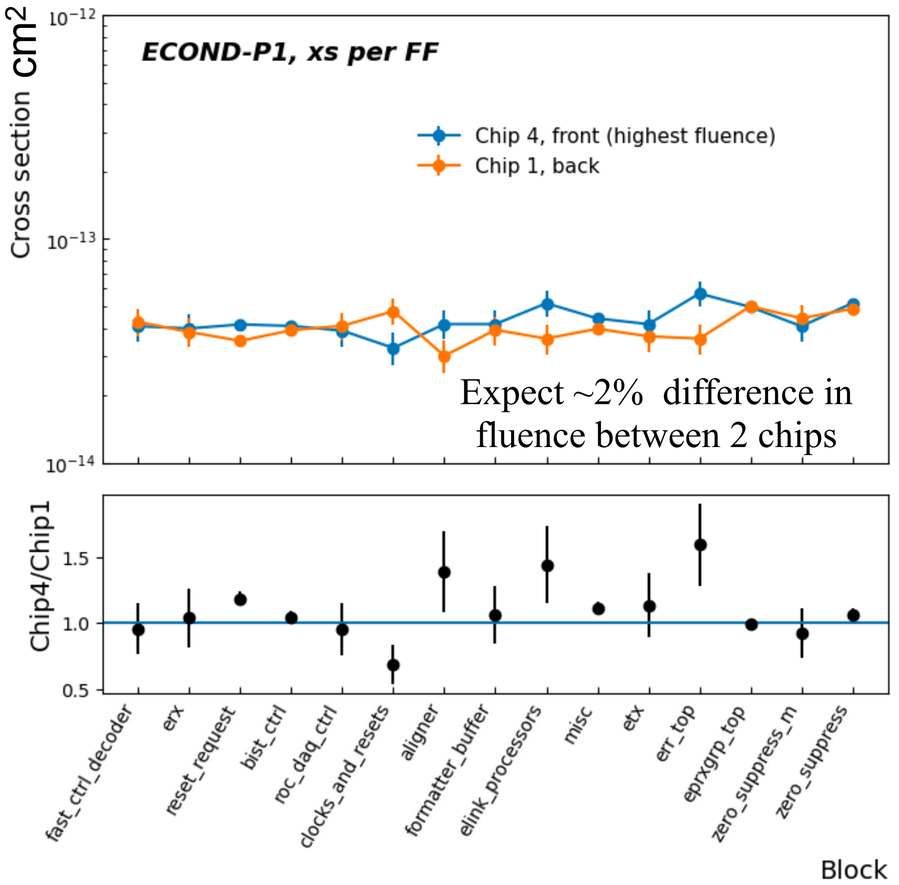


Each pre-voted FF will only see 3 errors in the lifetime of HGCAL

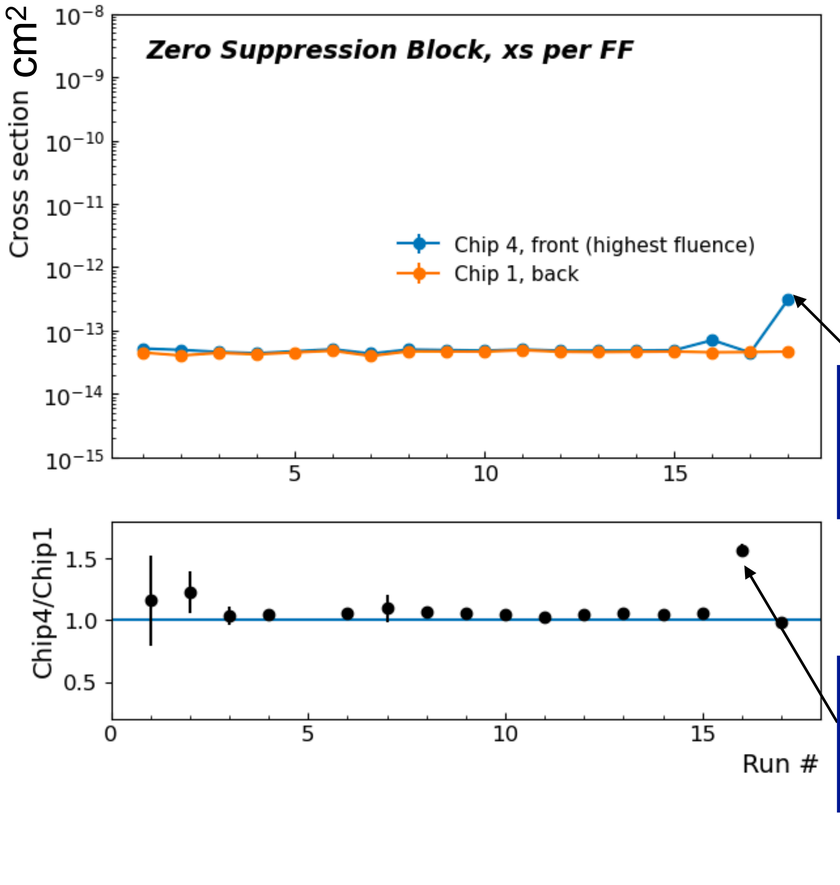
Single Event Effect testing

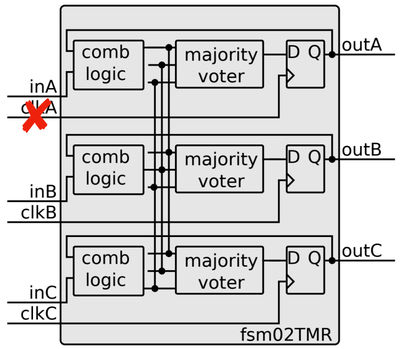
- ECON-D-P1: estimated bit error cross section from internal monitoring of TMR counters

Cross section per bit for pre-voted FF
$\sim 3 \times 10^{-14}$cm^2/FF



Special runs (ZS block)





Special test run turning off one triplicated clock (cross section value not meaningful)

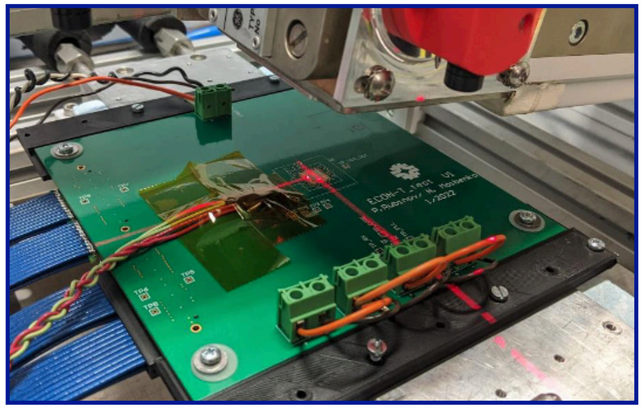
Special test run (chip 4) starting from FF values = 0 (different probability of flip 1→0, 0→1)

Each pre-voted FF will only see 3 errors in the lifetime of HGCAL

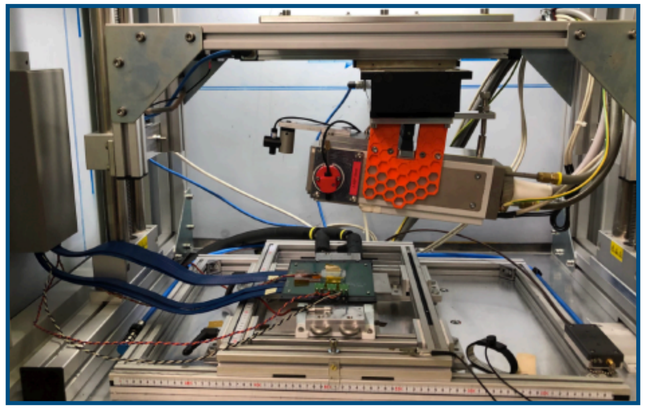
TID testing

Dose: ~ 9.2 Mrad/hour
Temperature: -20°C

ECON-T-P1 Oct 2022
2 chips irradiated



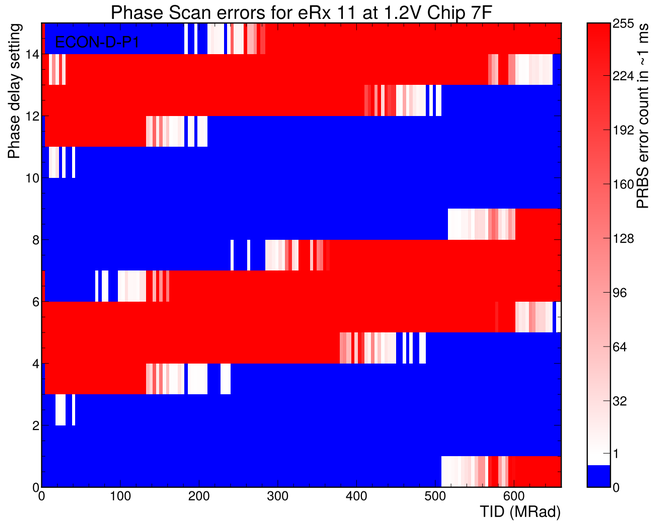
ECON-D-P1 Aug 2023
3 chips irradiated (1 with FIB modification)



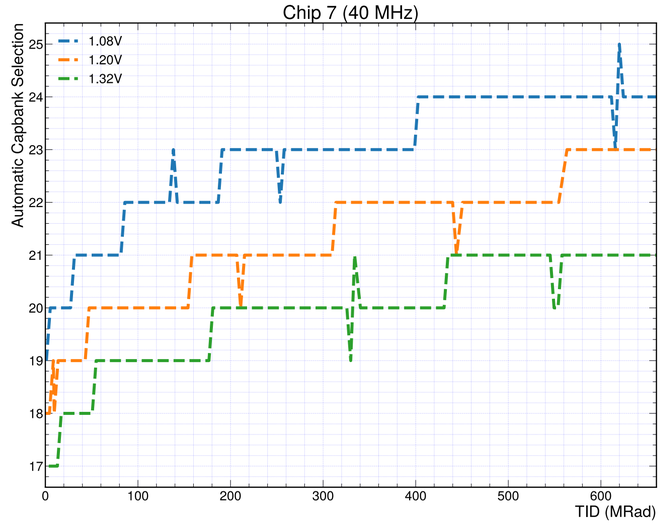
TID campaigns for ECON-T/ECON-D at CERN ObeliX X-ray:

- HGCAL requirement: 220 Mrad
- TID test: 660 Mrad/chip
- Observations:
  - Good behavior up to 660 Mrad, 1.2V
  - Evidence of small error rate (>450 Mrad for ECON-D-P1), 1.08 V

Evidence of slight degradation of width of good phase window at high TID, as expected

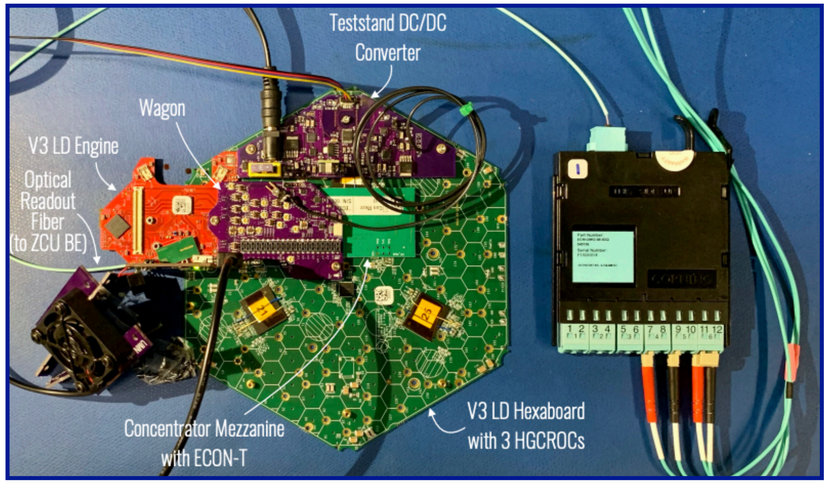


CapBank Selection for PLL as a function of TID (confirms lpGBT result)



ECON status summary

- All ECON-T and ECON-D P1 features (tested so far) are functional
  - Few bugs found, being fixed for the production run (Nov. 2023)
  - Verified functionality of standalone blocks and blocks using the lpGBT IP:
    - PLL issue with extra metal layer: ECON-D-P1 operates at 41-49 MHz.
    - Prototype run with mask respin will provide prototypes with corrected top metal (and good locking range)
- TID and SEE campaigns carried out successfully for both chips.
- Functionality of ECON-T and ECON-D P1being exercised in HGCAL test systems!

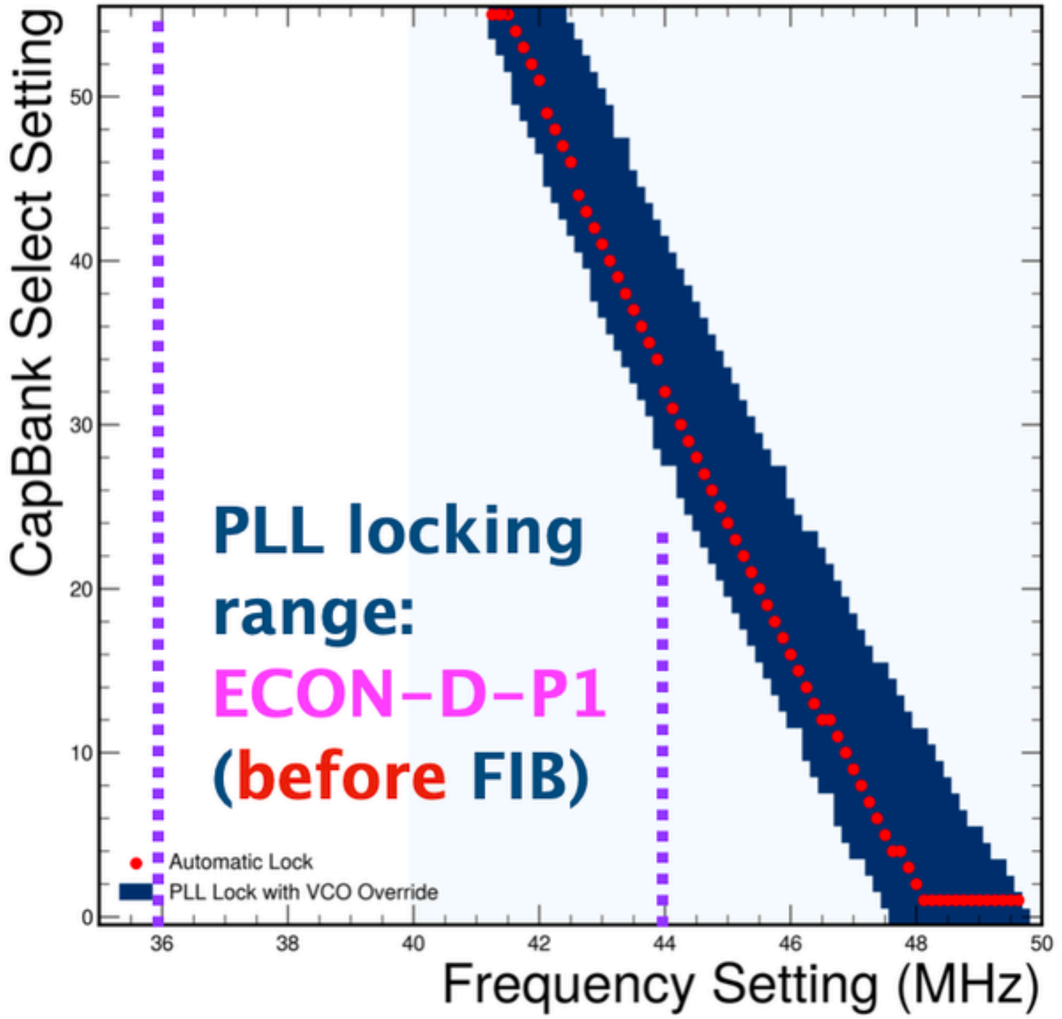


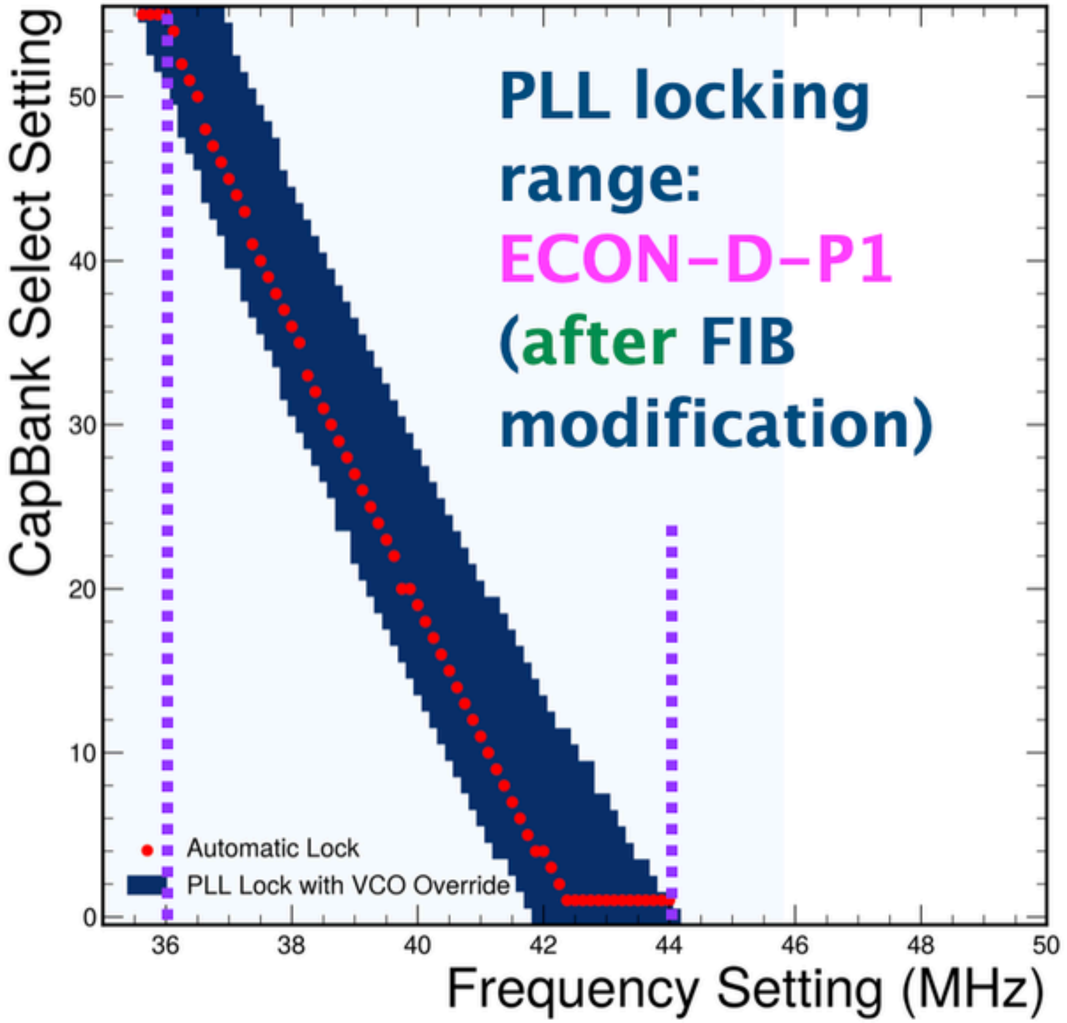
ECON-T-P1 in test system

Mezzanine with ECON-T-P1 and ECON-D-P1 (FIB modified)

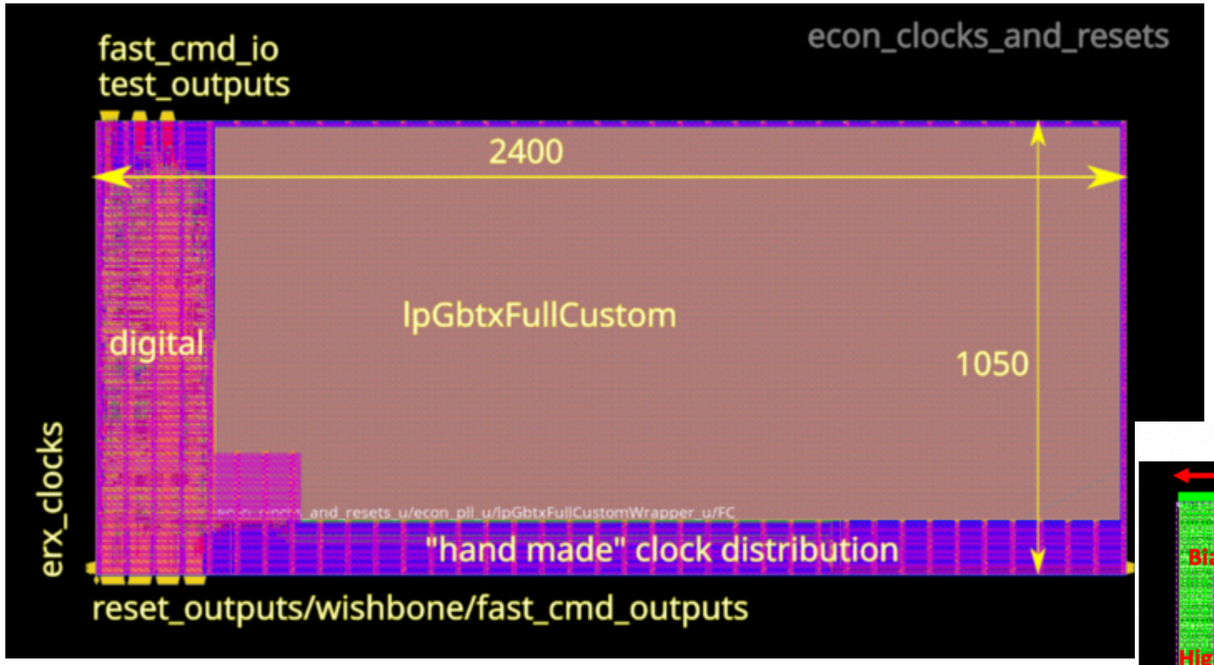
Backup

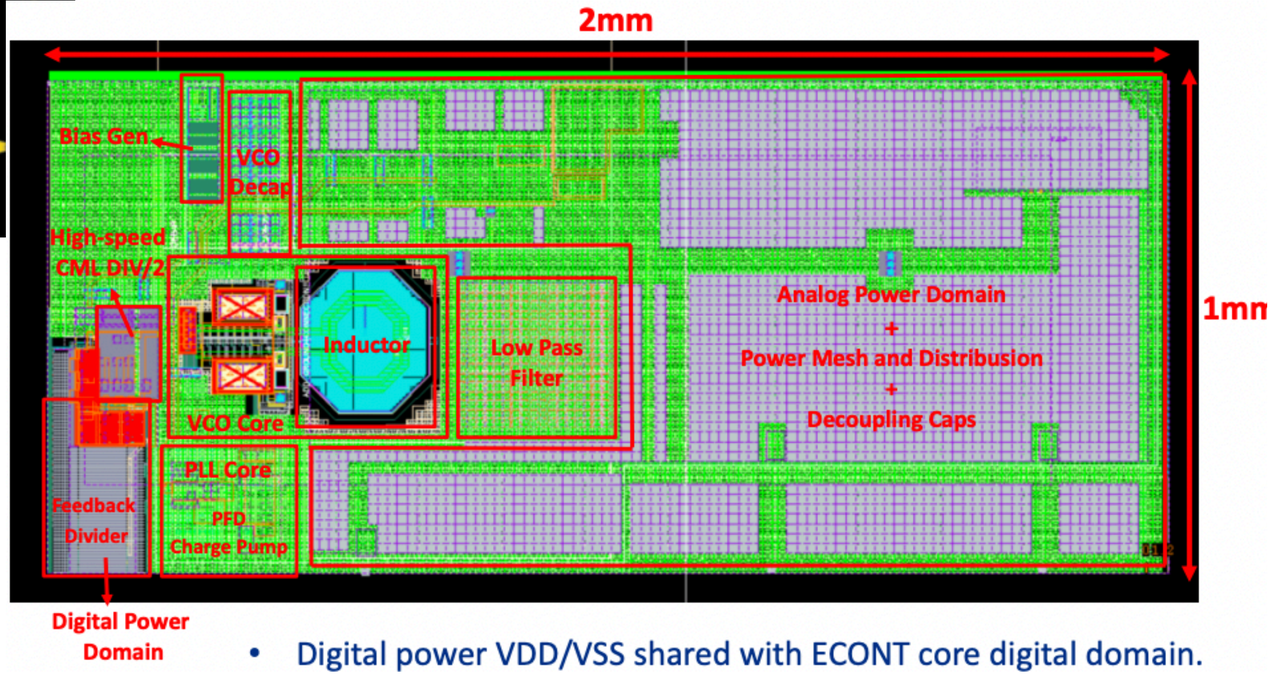
PLL locking range





Clocks and resets block

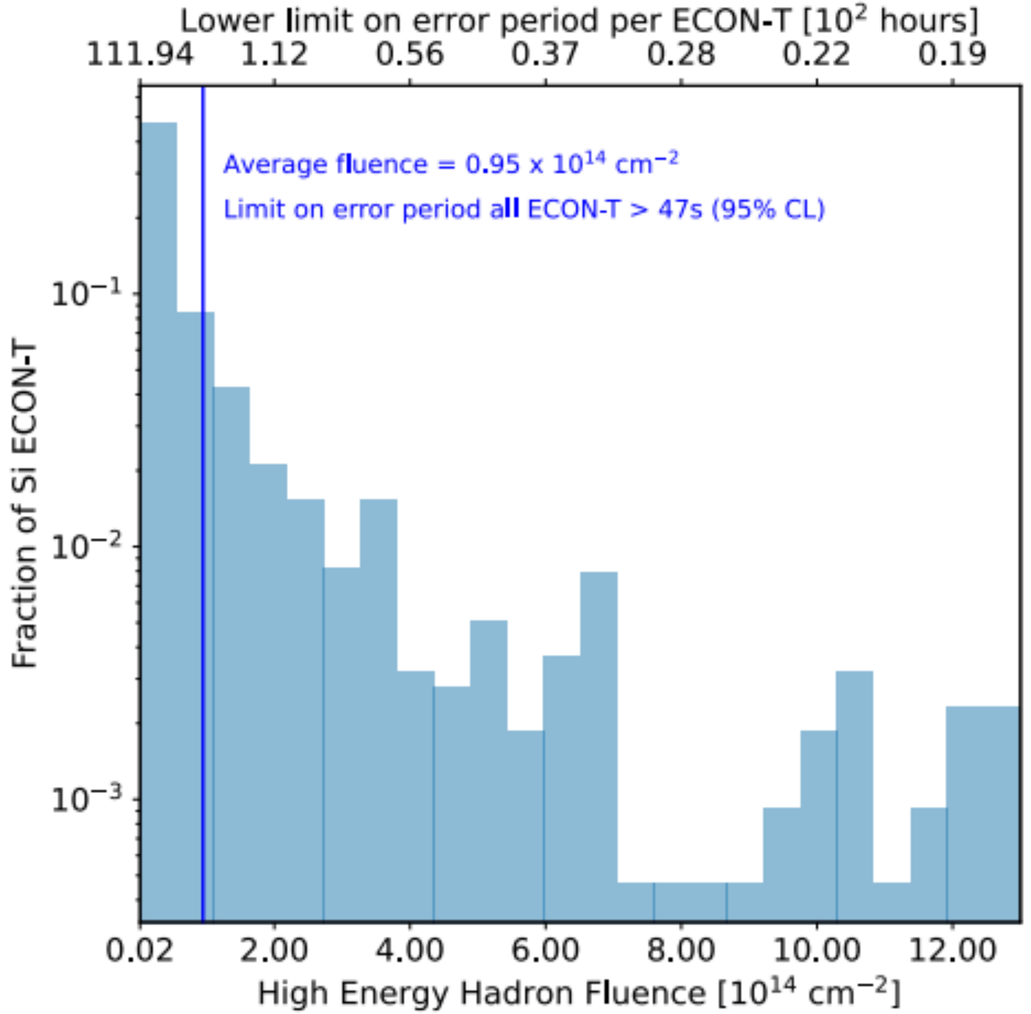




- Digital power VDD/VSS shared with ECONT core digital domain.

ECON-T-P1 limit

Limit on the period between errors requiring reset



Fluence for each ECON-T

About 50% of ECONs have fluence of 0.02 x 10^{14}

A few 0.1% of ECONs have fluence of 12 x 10^{14}

The average fluence is 0.95 x 10^{14}

The ECONs at the highest fluence will have a potential period of resets that is ~12x higher than the average rate

ECON-T-P1: measurements of SEU cross section/bit: internal monitoring of ECC error counters and data stream.

Single Event Effect testing

- ECON-T-P1: observed SET in serializer :
  - 32-bit shift registers were triplicated but not self-correcting
  - SEE introduced additional signals to begin serializing the 1.28 GHz clock
  - Full re-design of serializer for ECON-T-P2.