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First test results for ECON-T and ECON-D ASICs for CMS HGCAL

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With over 6 million channels, the High Granularity Calorimeter for the CMS HL-LHC upgrade presents a unique data challenge. The ECON ASICs provide a critical stage of on-detector data compression and selection for the trigger path (ECON-T) and data acquisition path (ECON-D) of the HGCAL. The ASICs, fabricated in 65nm CMOS, are radiation tolerant (200 Mrad) with low power consumption (<2.5 mW/channel). We report the first functionality and radiation tests for the ECON-D-P1 full-functionality prototype including a comparison of single event effect (SEE) cross sections measured for different methods of triple modular redundancy.

Summary (500 words)

The High Granularity Calorimeter (HGCAL) for the CMS HL-LHC upgrade is a sampling calorimeter that will feature fine readout segmentation. Amplitude and arrival time of analog sensor signals are digitized by the HGCROC ASIC, which also provides 12.5 us of trigger buffering of the digitized data. The transmission of digital data to the back-end electronics is handled by the ECON ASICs for data selection, compression, and concentration, and the lpGBT ASIC for data serialization to 10.24 Gbps.

The ECON-D ASIC manages data flow for events passing the 750 kHz L1 trigger. ECON-D specifically performs (a) zero suppression of raw HGCROC data with user-configurable corrections for common-mode front-end noise and contamination from out-of-time pileup and (b) autonomous generation of a front-end "reset request"based on highly configurable algorithms for time analysis of front-end error conditions. The ECON-T ASIC manages data flow on the HGCAL trigger path, which provides data to the L1 trigger at the full LHC 40 MHz bunch crossing frequency. ECON-T includes several user-selectable data compression algorithms, allowing the user to operate in modes with either fixed or variable latency and data format. In addition to traditional selection/compression algorithms, ECON-T features the first implementation of a radiation tolerant, low-power neural network (NN) for machine learning-based, on-detector data compression. Full reconfigurability of NN weights and biases allows reoptimization of the NN for changing detector and beam conditions.

Full functionality prototypes of both chips have been or are being produced: ECON-T-P1 was received in December 2021, and ECON-D-P1 will be received in June 2023. Both ASICs are produced in a 65nm CMOS process and designed to meet radiation tolerance requirements for SEE and TID (200 Mrad), low power consumption (less than 5 mW/channel for both ECON-D and ECON-T combined), and a programmable number of 1.28 Gbps inputs and outputs. The radiation hard IP blocks for the PLL, receivers, transmitters, and input phase alignment are taken from the lpGBT IP. SEE protection is achieved through triple modular redundancy: ECON-T-P1 includes triplication sequential logic with a single-voter strategy. ECON-D-P1 implements triplication of sequential and combinatorial logic, resets, and clocks in most of the design.

In this report, we summarize full test results for the ECON-T-P1 including functionality and radiation (SEE and TID) performance. We present first results from ECON-D-P1 functionality and radiation testing, and we show a unique comparison of the level of SEE protection provided by the different methods of triple modular redundancy used in the two ASICs.

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