Design and characterization of RD53C production chips for ATLAS and CMS pixel upgrades at HL-LHC

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on behalf of the RD53 Collaboration

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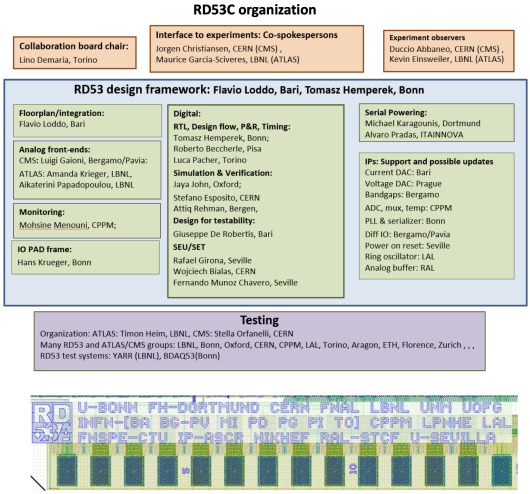
The RD53 collaboration on 65 nm CMOS technology

Initial mandate

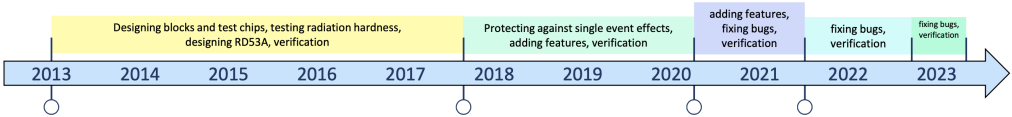
- **joint effort between ATLAS and CMS** established back in 2013 to develop new pixel readout chips for HL-LHC pixel detectors upgrades
- 24 partecipating institutes (Europe + USA)
- characterization of **65 nm CMOS technology** in radiation environment
- design of a **rad-hard IP library** (analog front-ends, A/D and D/A converters, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO)
- design and characterization of **half-size pixel chip demonstrator** with design variations (**RD53A**)

In 2018 the LHCC extended the collaboration for 3 years

- design of full-size **pre-production** (**RD53B**) and **production** (**RD53C**) pixel chips for ATLAS and CMS experiments
- ATLAS and CMS chips are two "instances" of a **common ASIC design infrastructure** with different size for mechanical integration and Analog Front-Ends according to specific requirements by the experiments
- request to LHCC to further extend the collaboration by 3 years to ensure necessary support for testing and to experiments

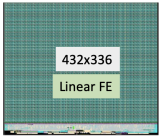


RD53 ASICs development



submitted in August 2017

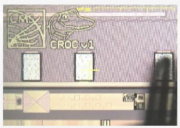
submitted in March 2020



submitted in June 2021

RD53A

RD53B-ATLAS (ItkPix_V1)

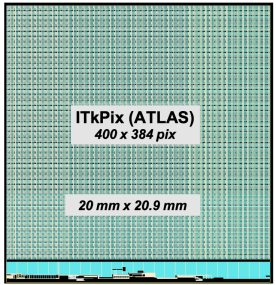


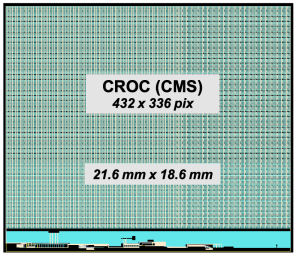
RD53B-CMS (CROC_V1)

Design strategy

Digital-on-top (DoT) approach:

- common digital-centric **design and verification framework** referred to as RD53B
- RTL code and digital implementation flows parameterized in terms of "experiment flavour"
- ATLAS and CMS chips are **two different instances of the same common design**
- **different chip-size** for mechanical integration **and analog front-end** according to specific requirements of the experiments
- **common digital synthesized logic**
- unused experiment-specific additional features simply turned off by configuration





- Final **RD53C-ATLAS (ITkPix_V2)** production chip submitted on Apr 2023 and currently under test !

- Final **RD53C-CMS (CROC_V2)** production chip assembled and ready for submission !

Design requirements and chip specifications

Parameter	Value (CMS/ATLAS)
Technology	65 nm CMOS
Max. hit rate	**3.5 GHz/cm^2**
Trigger rate	**750 kHz / 1 MHz**
Trigger latency	**12.5 µs**
Pixel size (chip)	**50 x 50 µm^2**
Pixel size (sensor)	50 x 50 µm^2 or 25 x 100 µm^2
Pixel array	432 x 336 pixels / 400 x 384 pixels
Chip dimensions	21.6 x 18.6 mm^2 / 20 x 21 mm^2
Detector capacitance	< 100 fF (200fF for edge pixels)
Detector leakage	< 10 nA (20nA for edge pixels)
Min. threshold	**< 1000 e-**
Radiation tolerance	**1 Grad** over 10 years at -15°C
SEE tolerance	**SEU rate, innermost: ~100Hz/chip**
Power	**< 1W/cm^2**, Serial powering
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Temperature range	-40°C ÷ 40°C

- RD53B Design manual and user guides: https://cds.cern.ch/record/2665301
- RD53B requirements: https://cds.cern.ch/record/2663161

Pixel ASIC functional overview

In short, extremely complex pixel readout ASIC designed to have a **minimal I/O interface** with the outside world with as fast as possible data links:

power

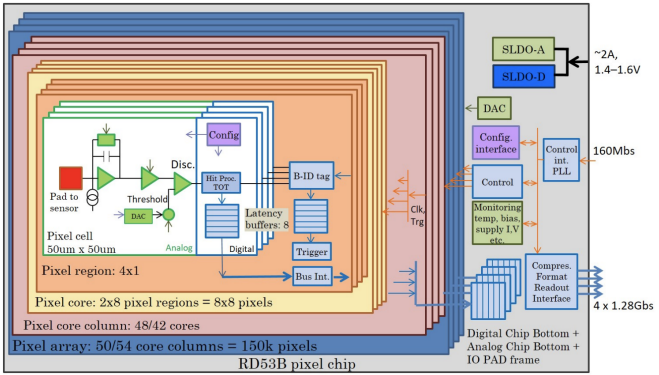
- input/output currents for **serial powering**

input data: commands, control and timing

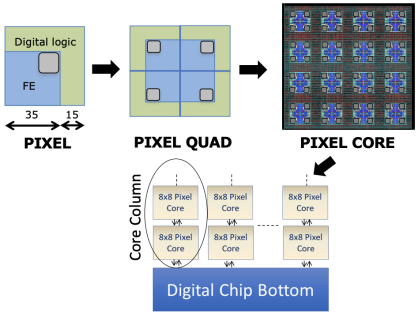
- one single 160 Mb/s differential serial input link used for all chip operations (synch/PLL lock and CDR, trigger, configuration commands, etc.)
- no external clock, no external reset

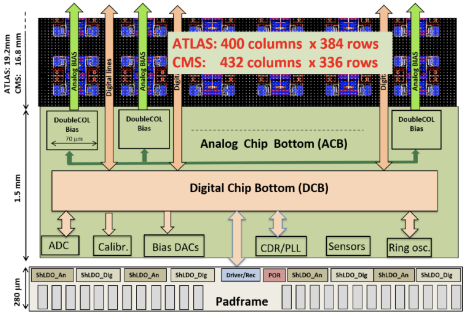
output data

- up to 4x 1.28 Gb/s CML output links for data readout (hit data + service data) compatible with LpGBT
- Aurora 64b/66b encoding



Logical design hierarchy





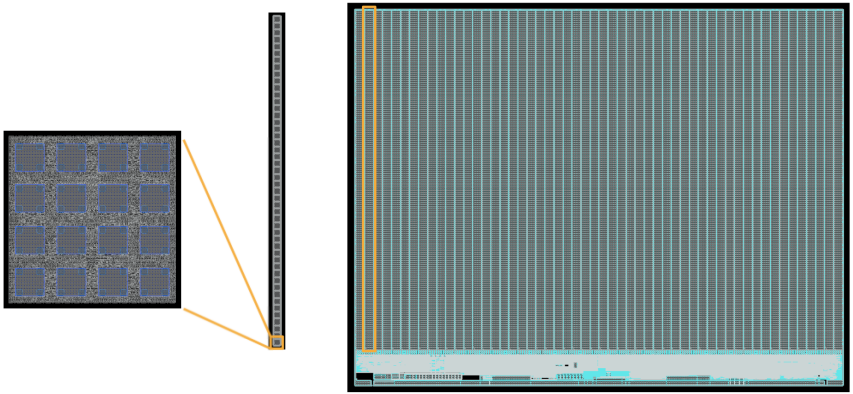
Pixel array

- 50 μm $\times$ 50 μm pixel size, approx. 50% analog and 50% digital
- digital logic synthesized for 8x8 pixels to form a **pixel core**
- all cores are identical $\rightarrow$ efficient hierarchical verification and implementation
- one digital readout block for each PixelCoreColumn in the chip periphery

Chip periphery

- **Analog Chip Bottom (ACB)**: contains all analog and mixed-signal blocks (bias DACs, CDR/PLL, ADC etc.)
- **Digital Chip Bottom (DCB)**: synthesized logic containing communication to/from the chip, readout and global configuration
- Common **padframe**: complex macro containing all I/O blocks with ESD protection and distributed Shunt-LDOs for serial powering

Floorplan and physical design hierarchy



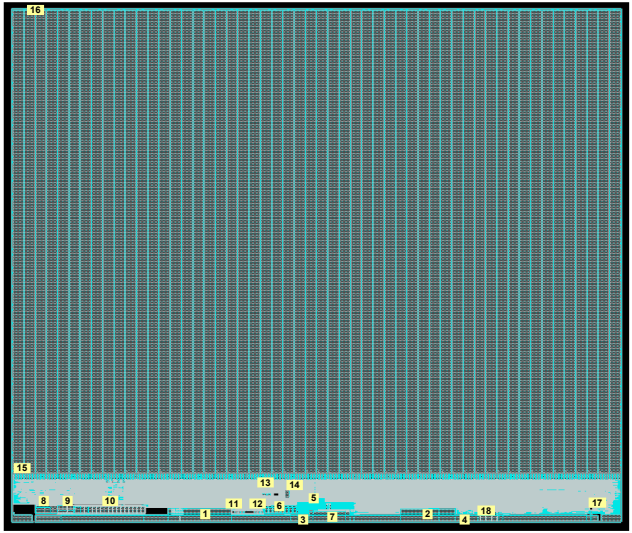
Chip assembling strategy:

- assemble "pixel core" (8x8 pixels) → abstract/Liberty
- step-and-repeat cores to form a "column of pixel cores" (core-column) → abstract/Liberty
- chip-periphery/top-level flat (historical choice)
- assemble top-level (synthesized logic + hard-macros + complex padframe macro)

Analog and M/S blocks summary

Block	Description
Analogue front end	The ATLAS chip versions use a differential front end. The CMS chip versions use a linear front end.
Shunt LDO	Enables start-up and serial powering. Constant input current shared between chips, modules on serial chains. 1 LDO for digital power, 1 LDO for analogue power.
Clock & Data Recovery (CDR)/PLL	Recovers a 160MHz clock and command/trigger stream. The PLL generates internal clocks: 160 MHz, 64 MHz, 640 MHz and 1.28 GHz.
Bias circuit	Provides biases to the pixel array. Based on bandgap references.
Calibration circuit	Injects hits into the pixel array, to calibrate its response.
Monitoring block	Digitises analogue quantities using a voltage mux, current mux and 12-bit ADC
Temperature and Radiation sensors	Temperature sensors: polysilicon resistors. Radiation sensors: based on PMOS devices with a linear variation in voltage in the dose range 10 - 1000 Mrad.
LVDS pads/drivers	Pads and drivers for differential inputs/outputs

Top-level layout with analog and M/S blocks



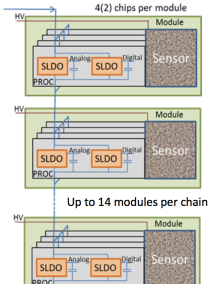
1. ShuLDO-A (master)
2. ShuLDO-D (master)
3. 160 Mb/s serial input LVDS RX
4. 4x DataMerge (DM) LVDS RX
5. PLL/CDR/DM
6. PLL biasing DACs
7. 4x 1.28 Gb/s serializers + CML drivers
8. monitoring block (V-MUX + I-MUX + 12-bit SAR ADC)
9. calibration block + CAP measurement circuit
10. Front-End specific biasing DACs
11. temp/rad sensor (ShuLDO-A hotspot)
12. temp/rad sensor (ShuLDO-D hotspot)
13. temp/rad sensor (middle of the chip periphery)
14. ring oscillators (monitor STD cell speed RAD degradation)
15. bottom-array temp sensor
16. top-array temp sensor
17. 32-bit E-FUSEs block (foundry IP)
18. 4x GPO LVDS TX

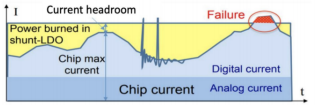
Selected implementation details

Serial powering

Both ATLAS and CMS will adopt the innovative **serial-powering scheme**

- based on complex **Shunt-LDO regulators** inside the chip
- one regulator for each power domain (1x analog + 1x digital)
- **constant input current** shared among more chips (2-4) on the same module (less cables)
- modules are in serial chains: "recycle" current from one module to another
- in case of chip failure, its current can be absorbed by the other chips of the module
- not sensitive to voltage drops
- **on-chip regulated supply voltages**
- radiation hardness (> 500 Mrad) silicon proven in RD53A and next prototypes

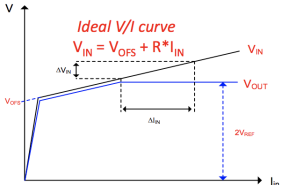




Example current consumption of one readout chip

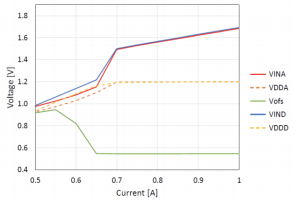
Protections:

- *Over-voltage protection*: V_{IN} clamped to 2 V
- *Under-shunt protection*: V_{OUT} decreased in case shunt current goes below a certain threshold (due to excess load current)

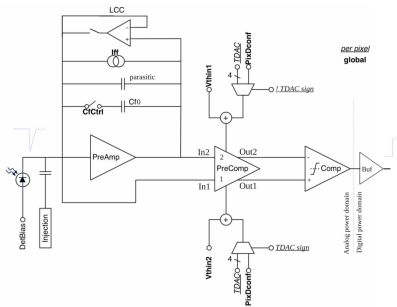


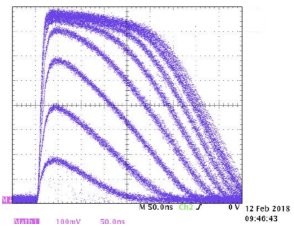
- V/I curve parameters (Voffset, slope) defined by external resistors
- V_{OUT} tunable by chip configuration

ITkPixV1.1 measurement at room T, pre-rad

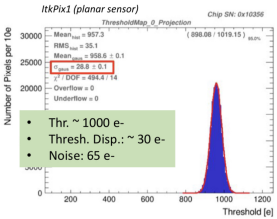


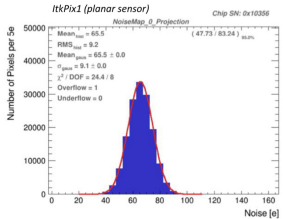
Differential analog front-end (ATLAS)



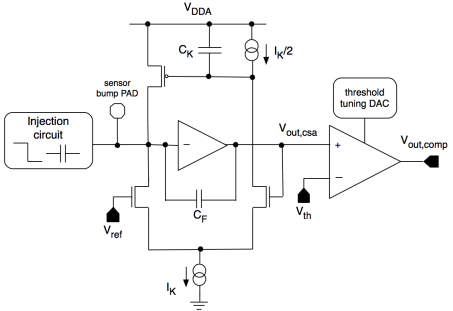


- single-stage **charge-sensitive amplifier (CSA)**
- continuous-reset integrator with tunable feedback current (global setting)
- dedicated leakage-current compensation circuit
- DC-coupled **differential pre-comparator** stage
- per-pixel **threshold adjustment** with local 4+1 bit DAC
- fully-differential comparator

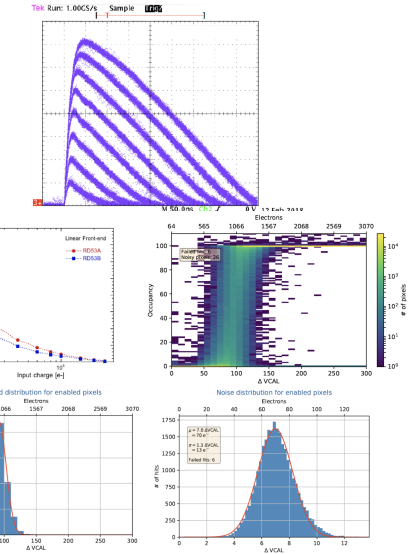




Linear analog front-end (CMS)



- single-stage **charge-sensitive amplifier (CSA)**
- **Krummenacher feedback** for triangular pulse-shaping and leakage-current compensation
- low-power asynchronous fast comparator for hit discrimination
- 10-bit DAC for global threshold
- per-pixel **threshold adjustment** with local 5-bit DAC



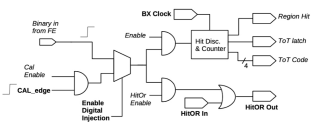
Pixel digital architecture

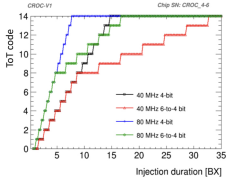
Per-pixel digital logic

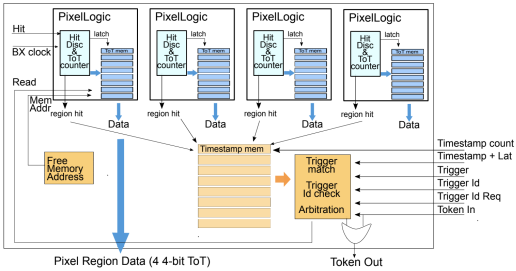
- selectable **synchronous or asynchronous hit-sampling mode**
- charge measurement by means of **Time-over-Threshold (ToT)**
- hits stored as ToT values + BX time-stamp
- per-pixel 6-bit ToT ripple counters, then mapped to 4-bits only
- selectable **dual-slope 6-to-4 ToT mapping** for **digital charge compression** (useful in case of elongated clusters)
- selectable ToT clock frequency (40 MHz or dual-edge 80 MHz)
- **digital and analog injection**

Region-based digital logic

- pixels readout organized into 1 ($r\phi$) x 4 (z) **pixel regions**
- per-pixel 4x8 ToT memory slots
- **shared timestamp memory** among 4x pixels in the same pixel-region
- **trigger-matching** performed at pixel level with programmable 9-bit trigger latency (max. 12.5 μs)
- **token-based readout** of hits
- **hit-OR** path + 11-bit **Precision ToT (PTOT)** counting at 640 MHz in the chip periphery for precise front-end and sensors characterization







Data-flow architecture

Command, control and timing

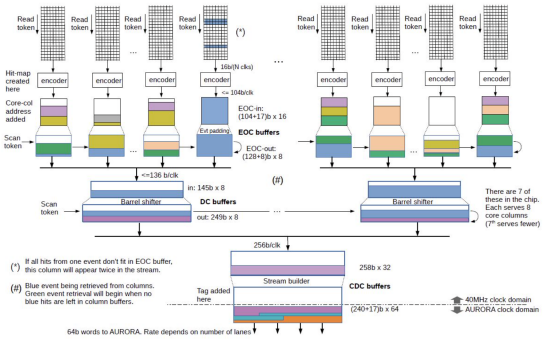
- one single 160 Mb/s differential control link with a custom developed protocol driving up to 15 chips (4-bit addressing + broadcast)
- CDR/PLL recovers Data and Clock

Readout via high-speed CML serial links

- **token-based readout** of hits
- hit data read in parallel for each core-column as soon as a valid trigger is received
- **multiple levels** of data processing, event building, data buffering and formatting
- **service data** collection and formatting (e.g. ADC motoring data, pixel configuration readback values) interleaved with Physics data in a set ratio (default 1:50)
- **Aurora 64b/66b encoding** (on-chip Aurora transmitter)
- building an Aurora frame based data stream to be send to **high-speed serializers** (4x 1.28 Gb/s)

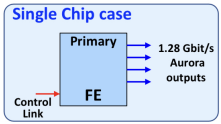
Design For Testability (DFT)

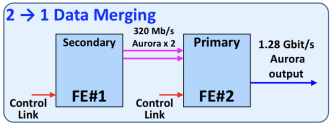
- entire chip-periphery covered by **scan-chain**
- industry-standard methodology adopted to speed-up Wafer Level Testing (WLT) for massive production

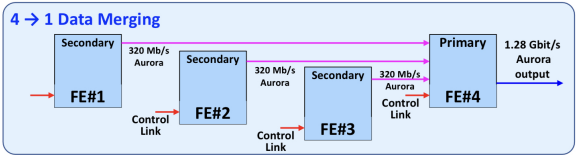


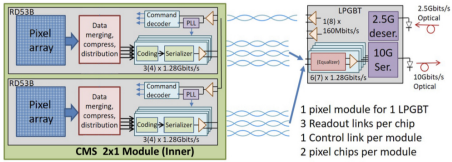
Multi-chip Data Merging (DM)

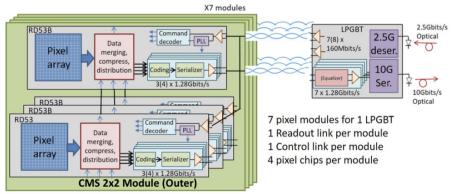
- additional 4x LVDS inputs up to 320 Mb/s
- allows to **reduce the number of e-links** to read out data in the **outer layers** (reduced per-chip hit-rates)
- one chip can be configured as "primary" to **aggregate serial data** coming from one or more "secondary" chips and merge them with its own output
- data from the secondary chip(s) merged with data from the primary chip in a simple **round robin** scheme











SEU/SET mitigation strategy

SEU protection (chip-periphery)

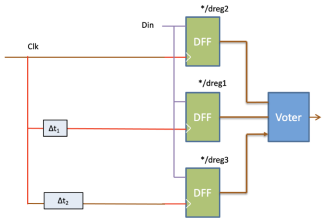
- approx. 100 Hz expected SEU rate per chip for the innermost layer
- **protect vital circuitry and data** as far as feasible within space limits
- priorities: protect **configuration data, state machines and memory pointers**
- semi-custom flow developed by the RD53 Collaboration
- TMR automatically inserted during synthesis based on register name (all FlipFlops are triplicated unless marked as `_notmr` in RTL)
- placement spacing constraint between FlipFlops then applied during place-and-route
- after TMR, low-enough SEU rate to allow **continuos re-programming** of global configuration registers and pixel configuration registers

SEU protection (pixel level)

- not enough space available to TMR all FlipFlops in the 8x8 pixel core
- TMR performed only on a **limited set of per-pixel configuration latches**, then rely on **continuos reconfiguration**
- extensive SEU/SET simulations to validate the design at both RTL and GL

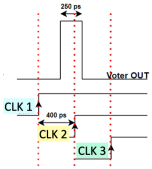
SET mitigation

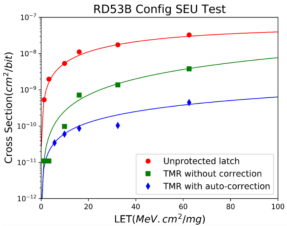
- usage of **synchronous reset** (almost) everywhere
- **SET filtering** achieved by means of automatically-inserted extra delays close to clock pins to locally spread the clock between FlipFlops



SEU cross-section comparison from heavy-ion testing

SET filtering





Design verification

Don't miss Adi's talk on this crucial topic!

Best Practices in Design Verification of ASICs for High Energy Physics Experiments

https://indico.cern.ch/event/1255624/contributions/5445241

Digital verification

Verification standard adopted in RD53 is UVM

- Universal Verification Methodology (IEEE Std. 1800.2-2020)
- industry-like approch, well-supported by tool vendors

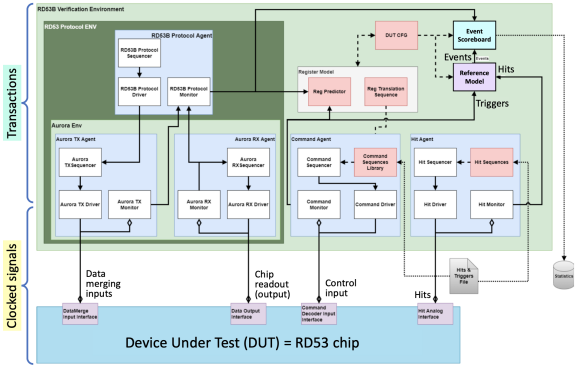
RD53 verification framework

- use of UVM concepts → implement design-specific UVM Verification Components (UVC)
- **Command** UVC: send commands according to protocol
- **Aurora** UVC: receive data, send data for DataMerging
- **Hit** UVC: send random hits or from distributions
- **Reference model**: predicts events, receive hits and triggers, read registers mirror
- **Scoreboard**: receive predictions from the Reference Model, receive data readouts from the DUT

Metric Driven Verification (MDV)

- simulate until the desired coverage is reached
- verification goal is always 100%
- **Code Coverage**
- **Functional Coverage**
- use **constrained randomization** to test all feasible combinations of configuration and inputs
- randomize sets of tests and learn which set is optimal (fewest runs) to reach coverage goals

RD53 verification framework (UVM)



Preliminary results from RD53C-ATLAS (ItkPixV2) testing

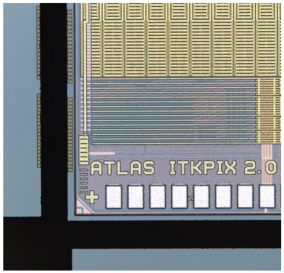
More results presented by *M. Mironova* a few weeks ago at *PSD13* !

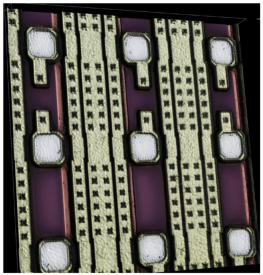
First results from the RD53 ATLAS pixel production readout ASIC (ITkPixV2) for HL-LHC

https://indico.cern.ch/event/1230837/contributions/5555586

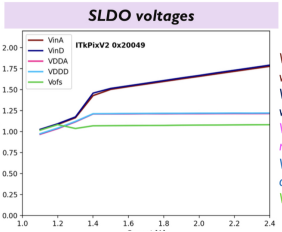
First start-up of ItkPixV2

- final RD53C-ATLAS (ItkPix_v2) production chip submitted on Apr 2023
- wafers received back from the foundry at the end of July
- extensive test campaigns immedialtely started at differet RD53 collaboration sites (CERN, Bonn, LBNL, Torino)
- initial results very promising !
  - Shunt-LDO and current measurements
  - injection circuit caibration
  - digital and analog injection scans
  - threshold scans and trimming
  - digital configurations
  - implemented bug fixes works

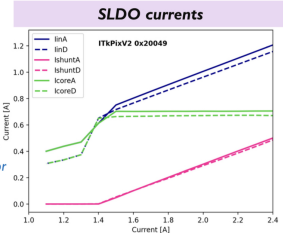




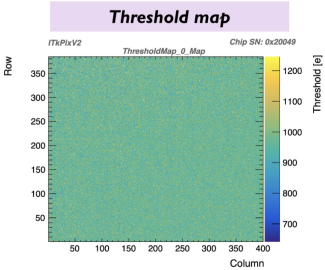
First start-up of ItkPixV2 (cont'd)

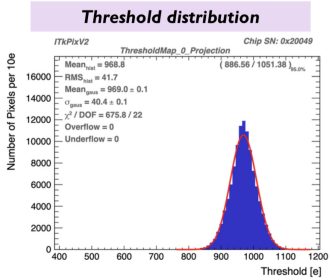


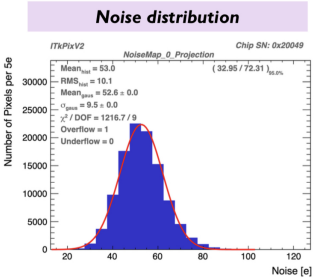
VinA – analog input voltage
VinA – digital input voltage
VDDA – analog regulator output voltage
VDDD – digital regulator output voltage
Vofs – offset voltage



Iin – chip input current
Icore – current consumed by chip
Ishunt – current consumed shunt element







Conclusions

- The readout chips for the ATLAS and CMS HL-LHC pixel detectors are being developed by the **RD53 Collaboration** on 65 nm CMOS technology since 2013
- Very big collaboration (24 institutions from Europe and USA) lasting for almost 10 years ...
- ... and (extremely) rare example of engineers and physicists of two experiments working together !
- The first **half-size prototype RD53A** has been crucial to initially explore design variations and to understand how to cope with the complexity of implementing such large and complex pixel chips
- Development of a common design and verification framework to implement **final chips** as two different "instances" of a common design having different sizes and different Analog Front-End
- Full-size **pre-production** chips **RD53B-ATLAS (ITkPixV1)** and **RD53B-CMS (CROC_V1)** implementing all functionalities requested to operate into real experiments have been submitted though 2020 and 2021
- The ATLAS **final** production chip **ITkPixV2** has been submitted in Apr and characterizations have started
- All measurements up to now indicate that the chip works fine, more results to come
- The CMS final production chip **CROCv2** has been already assembled and verified and it is ready for sumbission

Thank you

for your attention !