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Design and characterization of RD53C production chips for ATLAS and CMS pixel upgrades at HL-LHC

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The RD53 Collaboration, established in 2013 as a joint effort between ATLAS and CMS pixel ASIC communities on 65nm CMOS technology, is now in the phase of implementing final pixel readout chips, referred to as RD53C revisions, that will be used into upgraded pixel detectors at HL-LHC. The purpose of this work is to provide a comprehensive review of most important architectural design choices, enhancements, implementation details and verification flows adopted to submit final ATLAS and CMS production chips, along with preliminary test results and measurements.

Summary (500 words)

New hybrid pixel detectors will be installed into ATLAS and CMS experiments to cope with unprecedented data rates and radiation levels foreseen for the High-Luminosity LHC upgrade at CERN. New machine operations will increase the instantaneous luminosity up to 7.5 x 10^{34} cm^{-2}s^{-1}, delivering an average of approximately 200 inelastic proton-proton collisions per beam crossing at the 40 MHz bunch-crossing rate.

The RD53 Collaboration was established in 2013 and extended in 2018 with the final goal to develop new pixel readout chips to be installed into ATLAS and CMS pixel detectors at HL-LHC. The chosen implementation technology has been a commercial 65nm CMOS which in the last decade has been extensively qualified and has been demonstrated to be radiation tolerant and able to cope with HL-LHC radiation levels.

A first large scale prototype chip, referred to as RD53A, was fabricated in August 2017. This chip allowed the experiments to evaluate different pixel readout architectural choices and analog front-end solutions fitting a 50 um x 50 um pixel size.

Later on a common design environment, referred to as RD53B, as been developed to implement pre-production versions of the ATLAS (ItkPix_v1) and CMS (CROC_v1) chips with parameters and IP blocks that can be instantiated into physically different chips by changing parameters. These chips have been submitted in 2020 and 2021 respectively, resulting into two physical instances of the common RD53B environment with different design choices such as pixel-array size and front-end flavour based on specifications driven by the experiment, while keeping all other system-level digital and mixed-signal functionalities in common. Extensive measurements and system characterizations have demonstrated these chips to be able to operate in the extremely harsh radiation environment (1 Grad) with very high hit rate (up to 3 GHz/cm2), trigger rates (4 MHz) and a high data rate readout (5 Gb/s) foreseen in the innermost pixelated layers at HL-LHC.

Final production chips, referred to as RD53C revisions and implementing minor fixes for known bugs from previous chips and further enhancements, will operate into ATLAS and CMS pixel detectors. At the time of writing the final version of the ATLAS pixel chip (ItkPix_v2) has been submitted in April 2023, while the submission of the final CMS chip (CROC_v2) is foreseen for July 2023.

The aim of this contribution is to provide a comprehensive review of RD53C production chips, summarising most important architectural features (global floorplan, front-end choice, serial powering, clock data recovering, slow control and configuration, trigger scheme, data processing, readout interface, multi-chip data merging, SEU/SET mitigation strategy) along with details on physical implementation and verification flows adopted by the RD53 Collaboration to design and verify such complex pixel chips. Preliminary test results on submitted chips will be also presented.

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