Testing and characterisation of the prototype readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker

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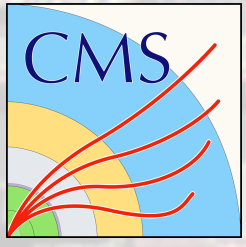
TWEPP 2023

2 October 2023



Introduction

- Topics:
  - Upgrade of the **CMS Inner Tracker** for **High-Luminosity LHC**
  - **The CMS Readout Chip (CROC)**
  - Testing and characterisation of the **prototype chip (CROCv1)**
    - Selected results from the testing and characterisation campaign
  - Status of the production chip (**CROCv2**)

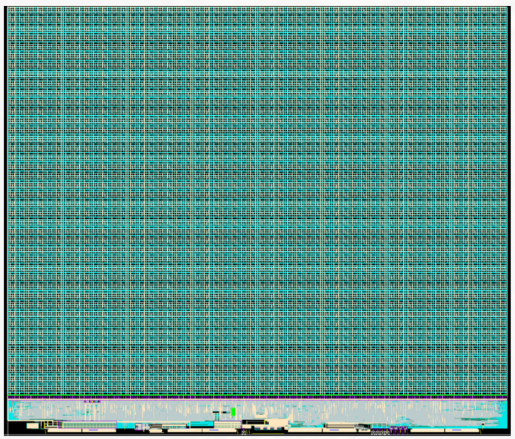
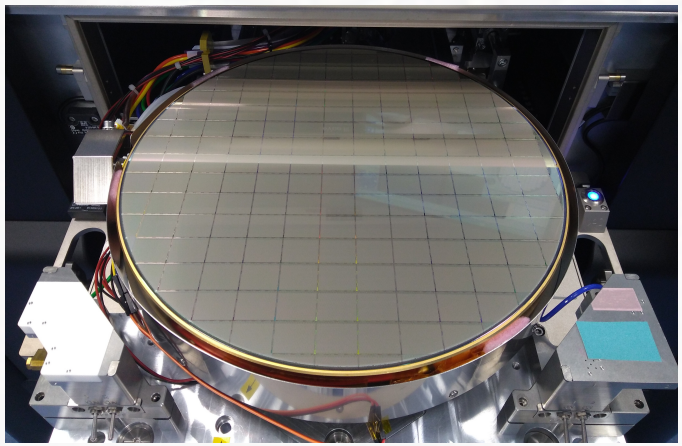
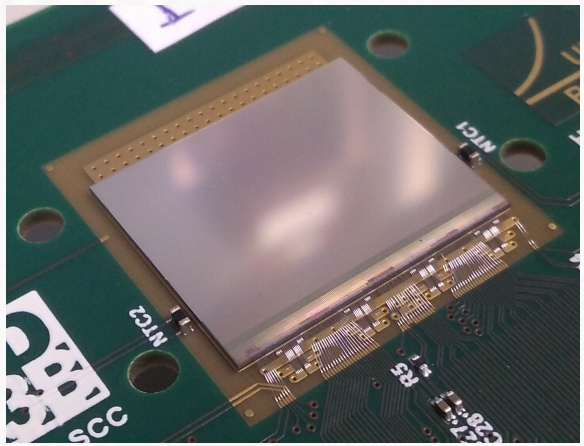
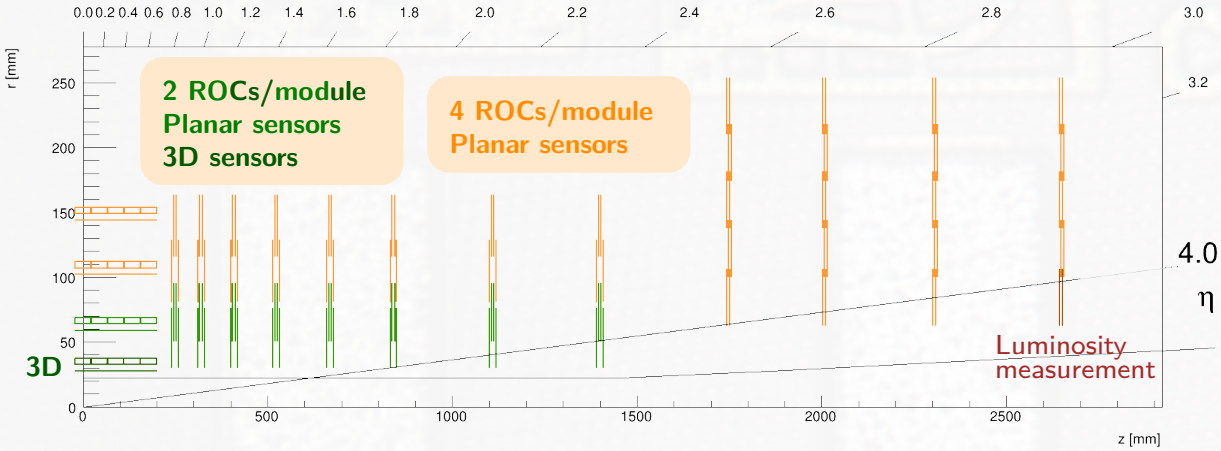




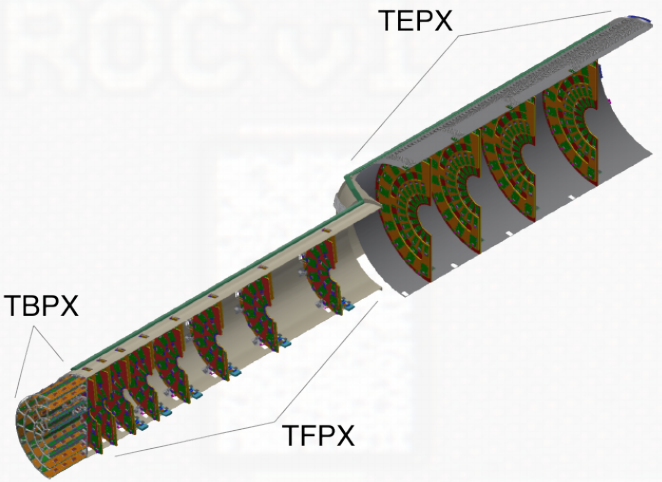
Figure: CROCv1 floorplan, 30 cm wafer, and diced chip wire-bonded to a testing board.

Upgrade of the CMS Inner Tracker for High-Luminosity LHC

- The **CMS detector** will be significantly upgraded for **High Luminosity LHC**
  - Instantaneous luminosity [$10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$]: 2 (LHC) $\rightarrow$ up to 7.5 (HL-LHC)
  - Average pileup (number of pp interactions per bunch crossing): 50 (LHC) $\rightarrow$ up to 200 (HL-LHC)
- The **Inner Tracker** will be completely replaced (2026-2028)
  - Target: maintain **high tracking performance** with **large pileup** and **harsh radiation environment**
  - **Hybrid pixel detector** with **high segmentation** (25 µm $\times$ 100 µm pixels)
  - Thin (150 µm) silicon sensors to improve radiation hardness
  - Active surface of about 4.9 m^2 and $|\eta|$ coverage up to $\sim$ 4 (2° to 178°)
  - Three sections: Barrel (TBPX), Forward (TFPX), and Endcap (TEPX)



(a) Layout of one quarter of the upgraded CMS Inner Tracker for High-Luminosity LHC. The **green**/**dark green** layers are instrumented with **2** readout chips (ROCs) per detector module, whilst **orange** layers have **4**. The **first TBPX layer** is also equipped with 3D sensors instead of planar ones.



(b) Three-dimensional view of one quarter of the upgraded Inner Tracker.

Figure: Layout of the upgraded CMS Inner Tracker for High-Luminosity LHC.

Pixel readout chip requirements for High-Luminosity LHC

- **Very harsh requirements for the pixel readout chip at High-Luminosity LHC:**
  - **High radiation hardness ▲**
  - **High hit rate capability ▲**
  - **High granularity ▲**
  - **Low detection threshold ▼**
  - **Low power consumption ▼**
  - **Low material budget ▼**

Parameter	Value
Technology	**65 nm CMOS**
Chip size	22 mm × 19 mm
Pixel bump pitch (chip)	50 µm × 50 µm
Pixel size (sensor)	**25 × 100 µm^2 or 50 × 50 µm^2**
Detector capacitance (per pixel)	< 100 fF (200 fF for edge pixels)
Detector leakage current (per pixel)	< 10 nA (20 nA for edge pixels)
Radiation hardness	**1 Grad** and **2 × 10^{16} (1 MeV n eq.) cm^{-2}** at −15 °C
Hit rate	**≤ 3.5 GHz cm^{-2}**
Hardware trigger rate (CMS)	750 kHz
Hardware trigger latency (CMS)	12.5 µs (500 bunch crossings)
Minimum threshold	**< 1000 *e***
Single-event upset (SEU) rate	**≤ 100 Hz**
Readout data rate	1 to 4 links at 1.28 Gb s^{-1} each
Powering mode	**Serial powering**
Power consumption	< 1 W cm^{-2}
Operating temperature	−40 to 40 °C

Table: Design requirements for the readout chip of the CMS Inner Tracker for HL-LHC.

The CMS Readout Chip (CROC)

- Developed by the **RD53 Collaboration**
  - Common framework for both ATLAS and CMS readout chips for HL-LHC
  - Three phases: **RD53A** (demonstrator chip); **RD53B** (prototypes); **RD53C** (final chips)
  - RD53B-CMS/CROCv1 submitted in June 2021
  - **More information on the CROC and on RD53C in the next presentation by Luca Pacher**

- **65 nm CMOS process**
  - Technology studied with RD53A chip
  - Avoided use of minimum size transistors in digital circuits (radiation hardness)
- **Pixel matrix**
  - 145 152 readout channels
  - Basic building block: 8 × 8 pixel core with synthesised digital logic
  - Most of the pixel configuration bits are protected with **triple-modular redundancy (TMR)** without self-correction
- **Analogue chip bottom (ACB)**
  - Contains analogue and mixed-signal circuits (bias, clock and data recovery, calibration, monitoring)
- **Digital chip bottom (DCB)**
  - Manages communication, configuration, data compression, and readout
  - Global configuration registers and state machines protected with **TMR** with self-correction and triplicated clocks

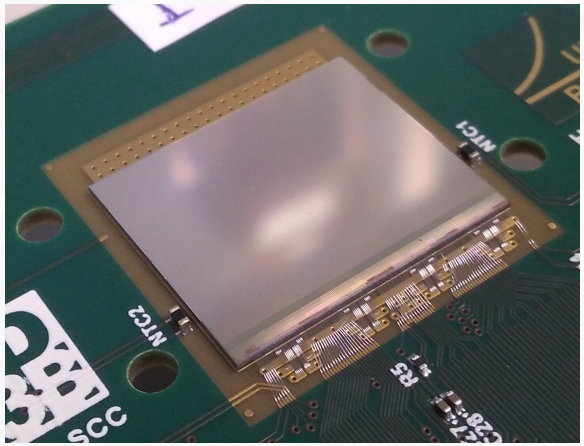


Figure: CROCv1 chip wire-bonded to a testing board. It covers an area of $2.2 \times 1.9\,\mathrm{cm}^2$.

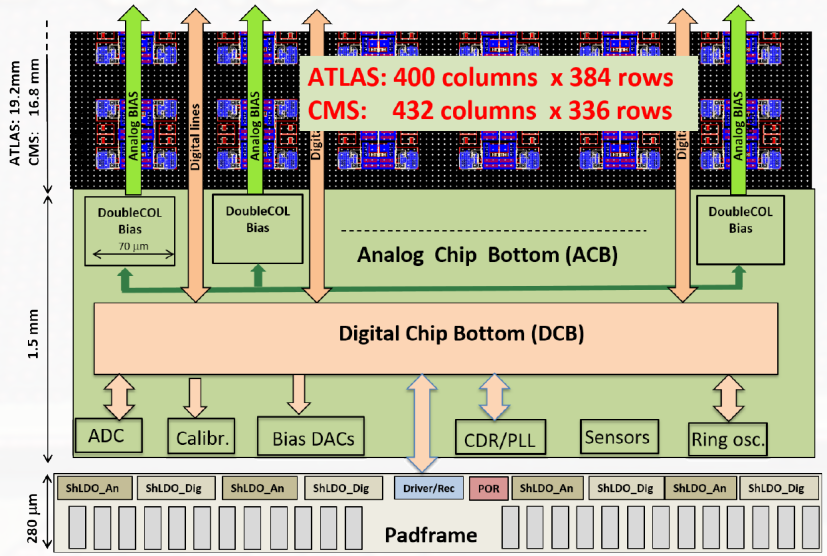


Figure: RD53B floorplan.

The CMS Readout Chip (CROC) / 2

- **Front-end**
  - Charge-sensing amplifier with Krummenacher feedback
  - Global and local (per pixel) threshold adjustment
  - 4 bit time-over-threshold (ToT) measurement
- **Inputs**
  - 160 Mb s^{-1} differential serial input for receiving commands and clock
  - Four 320 Mb s^{-1} differential serial inputs for merging data from other chips (**data merging**)
- **Outputs**
  - Four output lanes with current-mode logic (CML) drivers
  - Bitrate as high as 4 $\times$ 1.28 Gb s^{-1}
  - Aurora protocol with 64b/66b encoding
  - Output contains both *hit data* and *service data*
- **Powering**
  - **Serial powering scheme** with **on-chip shunt-LDO regulators**
  - Detector modules are powered in *series* with a current generator
  - Chips on a module are powered in *parallel* (current sharing)
  - Significant reduction in material budget from cabling

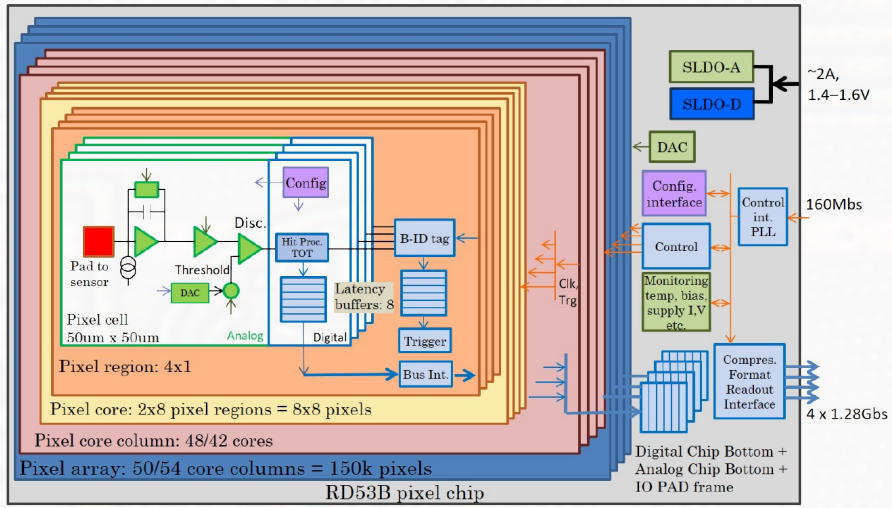


Figure: RD53B data flow architecture.

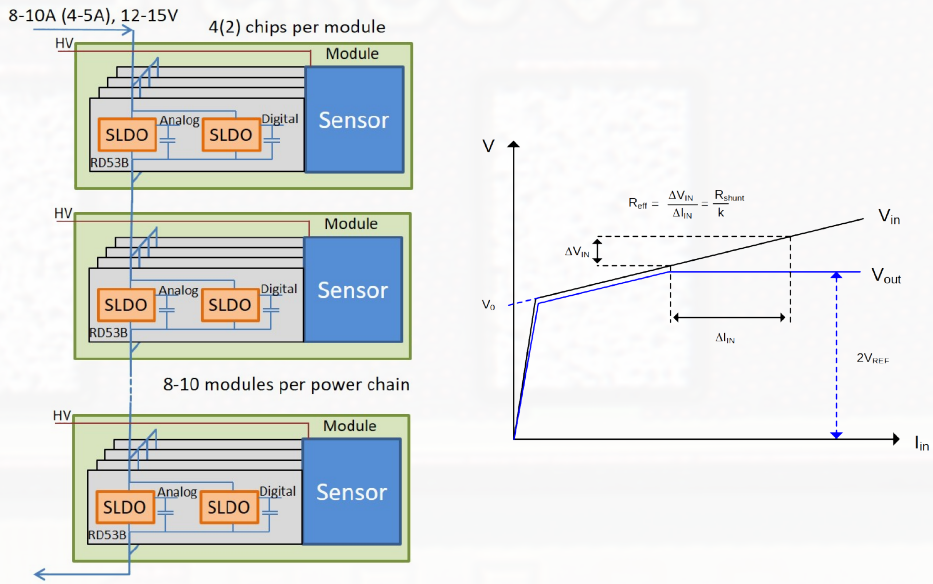
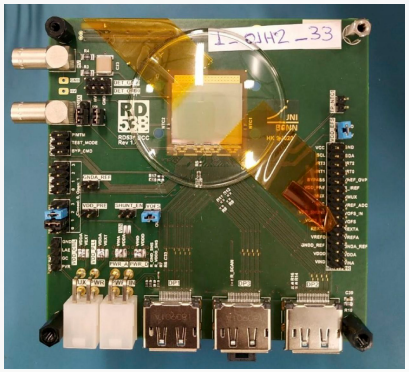


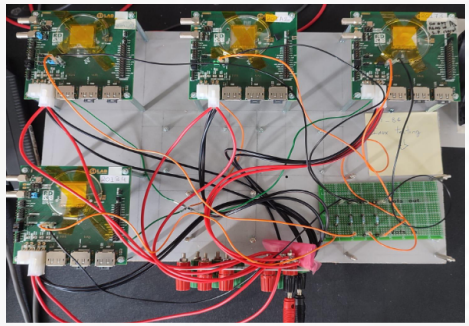
Figure: Serial powering scheme and shunt-LDO *IV* curve.

CROCv1 testing campaign

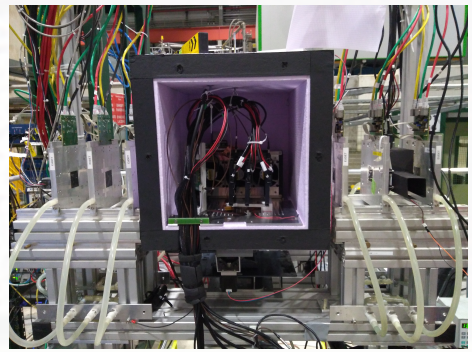
- **Extensive testing and characterisation campaign to validate the CROCv1, including:**
  - **Bench tests**
    - Front-end characterisation
    - Chip bottom testing
    - Serial powering tests
  - **Irradiation and SEE campaigns**
    - Reached 1 Grad TID with high dose rates
    - Fluences up to ca. 2×10^{16} (1 MeV n eq.) cm^{-2} have been obtained
    - Tested SEE sensitivity with proton, ion, and laser beams
  - **Beam tests**
    - Characterised both irradiated and unirradiated chips, with different sensor technologies (planar and 3D pixels)
  - **Wafer-level tests**
    - Very large dataset (138 chips/wafer $\times$ 14 tested wafers $\simeq$ 2000 chips)
    - Obtained chip yields, failure rates, characterisation data, calibration data



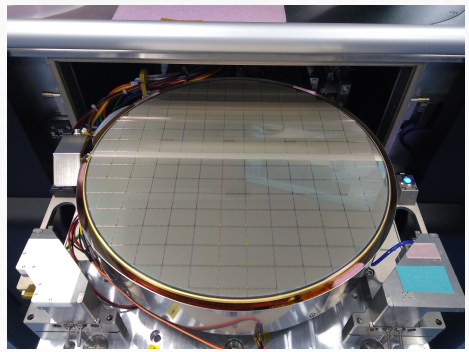
(a) Example of single-chip card used for characterisation.



(b) Testing setup with 4 single-chip cards in a serial powering chain in INFN Firenze.



(c) AIDA telescope and cold box at the SPS test beam area at CERN.



(d) CROCv1 wafer in the waferprobing facility in INFN Torino.

Figure: Testing of the CROCv1 in different configurations.

Front-end performance before irradiaton

- **Analogue front-end performance of bare chips, not irradiated**
  - **Tuned threshold**: down to 1.0 ke
  - **Threshold dispersion** after tuning: $\lesssim 50\,e$
  - **Equivalent noise charge**: $\sim 80\,e$
  - Adequate stability over a wide temperature range (-30 to $20\,^{\circ}$C)

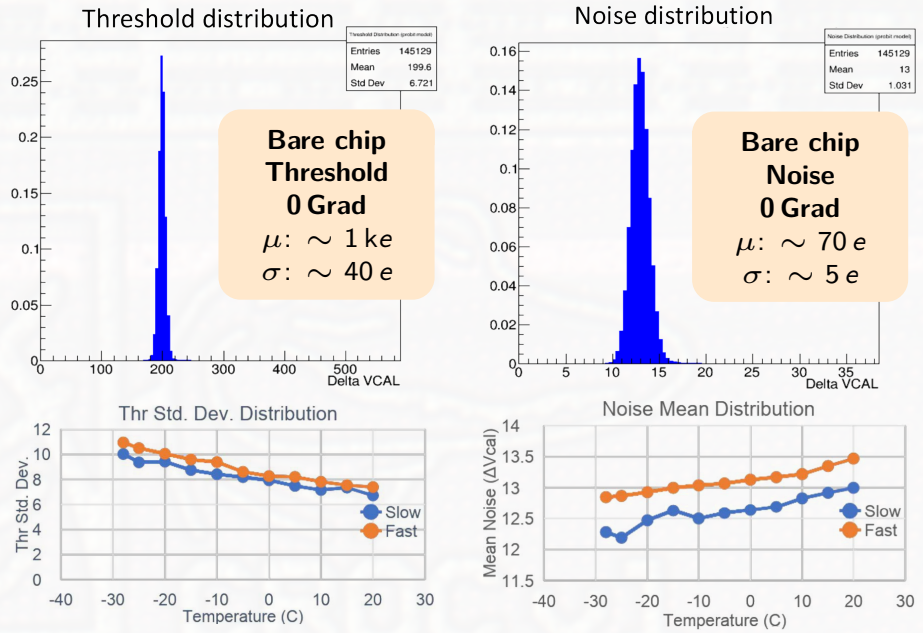


Figure: Threshold and noise distributions for a bare CROCv1 chip tuned to a threshold of 1 ke (top). Standard deviation of the threshold and mean noise as a function of temperature (bottom). One ΔVCAL unit corresponds to approximately 5 e. "*Fast*" and "*slow*" refer to different Krummenacher current settings.

- **Front-end efficiencies at high hit rates**
  - Tested with **X rays**
    - Analogue efficiency limited by dead time during ToT counting
    - Digital efficiency limited by hit data buffer overflow
  - Threshold tuning at 1.5 ke
  - Results matching simulations; higher efficiencies expected for charged particles
  - **Analogue ε (3.5 GHz/cm^2): $> 99\,\%$**
  - **Digital ε (3.5 GHz/cm^2): $\geq 95\,\%$**

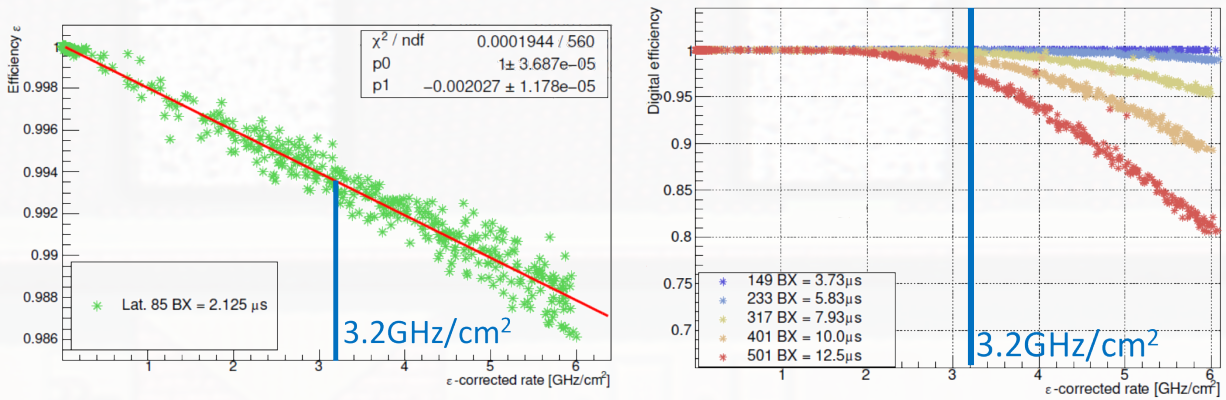


Figure: Analogue and digital front-end efficiencies at high hit rates.

Radiation hardness

- Verified **radiation hardness requirements** up to about **1 Grad** TID (high dose rates) and **2×10^{16} (1 MeV n eq.) cm^{-2}** fluences
  - **Chip remains functional and performant after irradiation at the required TID**
  - **Both the ACB and the DCB perform well up to 1 Grad**
  - TID damage mainly affects digital part of the chip (small area devices) but within requirements
  - DCB: gate delay degradation monitored with on-chip **ring oscillators** ($\lesssim 40\,\%$ decrease in frequency)
  - ACB: small or moderate variations in relevant chip currents/voltages
  - ACB: increase in analogue/digital `VDD` can be mitigated with 4 bit trimming DACs
- Several **SEE testing campaigns** performed (protons, ions, photons)
  - **Input link always functional** (can always send commands and write registers)
  - **Hard resets or power cycles not needed for recovery** (fast clearing of data path with `CLEAR` command suffices)

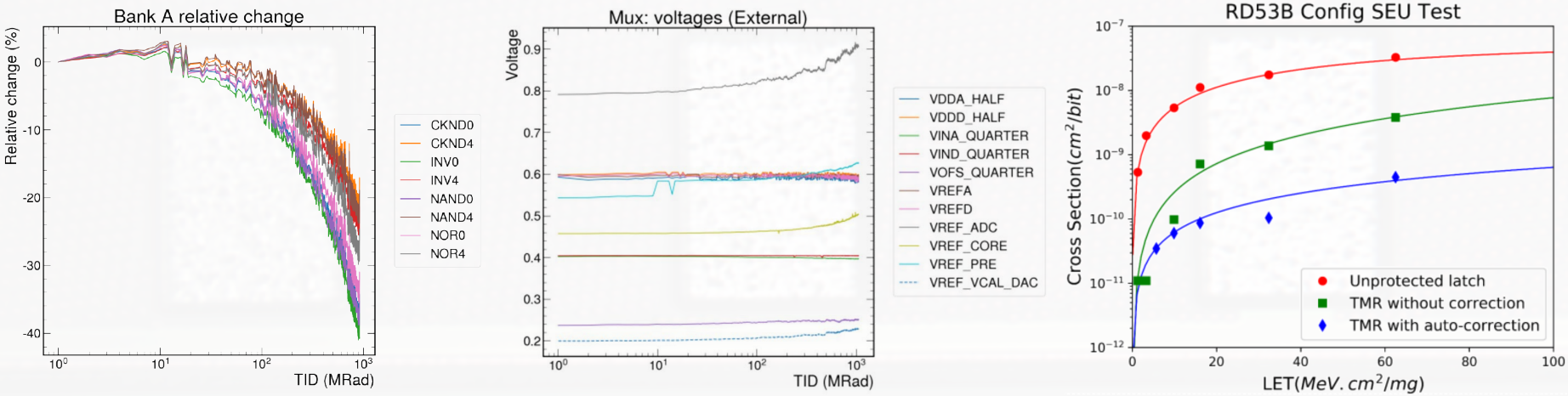


Figure: Relative change in ring oscillator frequency as a function of TID (left); Variations in several monitored chip voltages as a fucntion of TID (centre); SEU cross-sections with heavy ions (right).

Front-end performance after irradiation

- **Analogue front-end + sensor performance after irradiation to ca. 0.5 Grad**
  - Fluence: ca. 1×10^{16} (1 MeV n eq.) cm^{-2}
  - Irradiation performed at PS-IRRAD facility (CERN) with 24 GeV protons
  - Data from both **planar** and **3D sensors** from SPS test beam (November 2022)
  - **Tuned threshold**: down to 1.0 ke
  - **Threshold dispersion** after tuning: $\sim 80\,e$
  - **Equivalent noise charge**: $\sim 150\,e$

- **Analogue front-end + sensor performance after irradiation to ca. 1 Grad**
  - Fluence: ca. 2×10^{16} (1 MeV n eq.) cm^{-2}
  - Irradiation performed at PS-IRRAD facility (CERN) with 24 GeV protons
  - Data from **3D sensors** from SPS test beam (September 2023)
  - **Tuned threshold**: down to 1.0-1.1 ke
  - **Threshold dispersion** after tuning: $\sim 100\,e$
  - **Equivalent noise charge**: $\sim 160\,e$

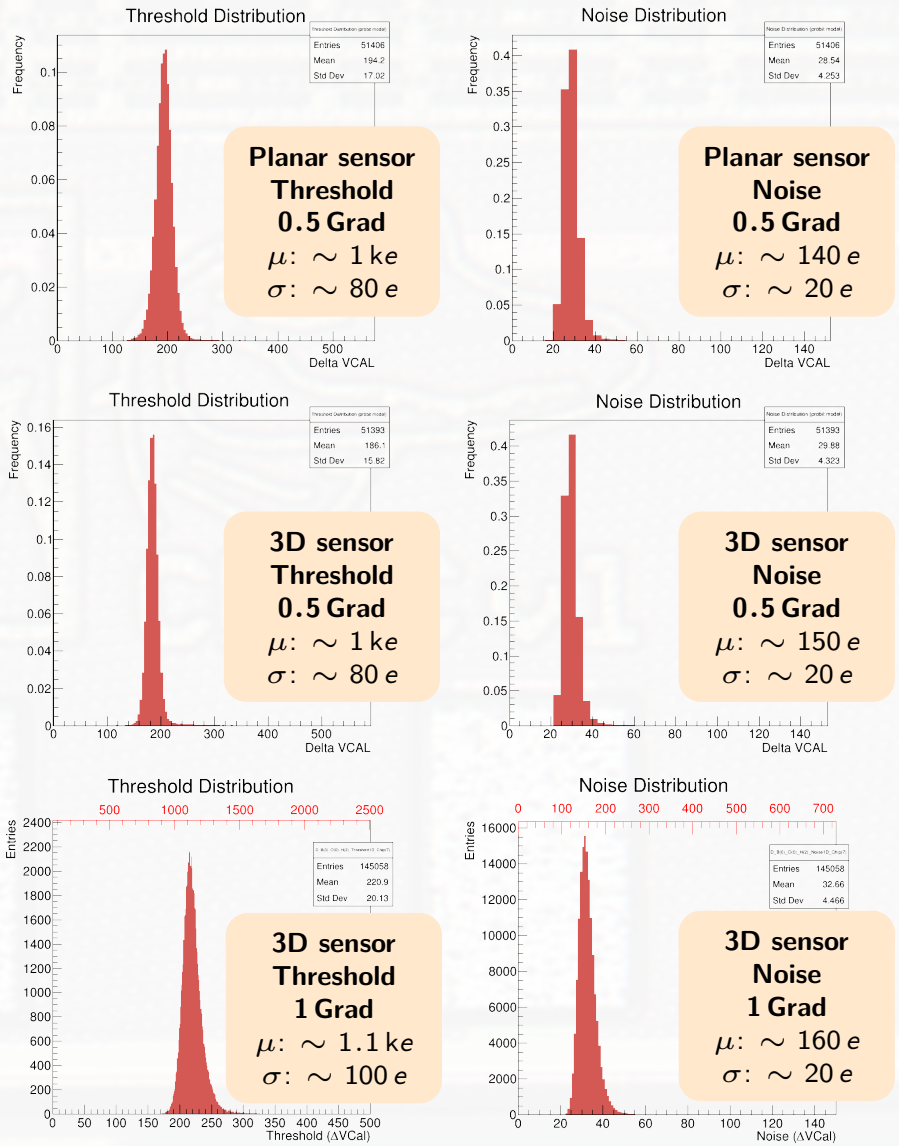


Figure: Threshold and noise distributions for different CROCv1 chips tuned to a threshold of about 1 ke. One ΔVCAL unit corresponds to approximately 5 *e*.

Shunt-LDO and serial powering tests

- Tested **serial powering scheme** using both single-chip boards and prototype detector modules
  - Serial powering appears to **function as expected**
  - Position in the serial powering chain does not appear to negatively affect chip performance
  - Process variations in shunt-LDO parameters seen during wafer-level testing are small ($\lesssim 1\,\%$)
- **Internal over-voltage protection circuit** (OVP) verified both with diced chips and at wafer level
  - The chip must be able to withstand up to **4 times the nominal current** ($4 \times 2\,\mathrm{A}$) in case of other chips *failing open* in a module in order **not to disrupt the whole powering chain**
  - Input voltage must remain below 2 V in any case

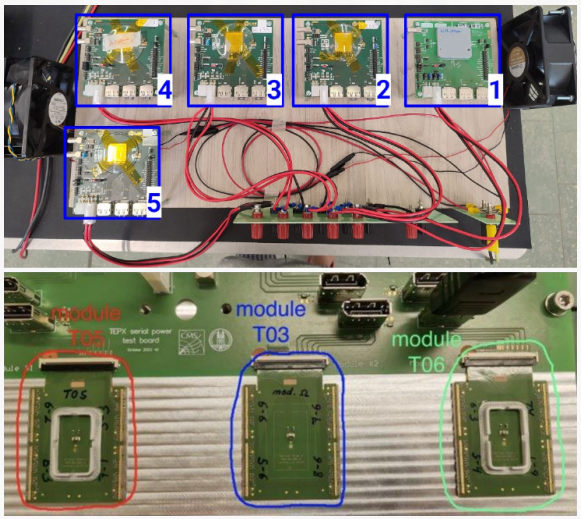
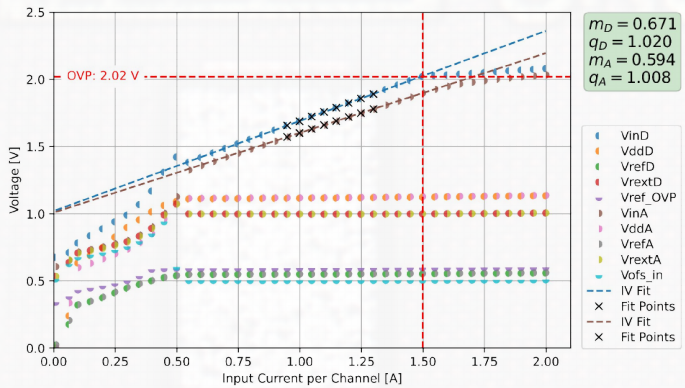
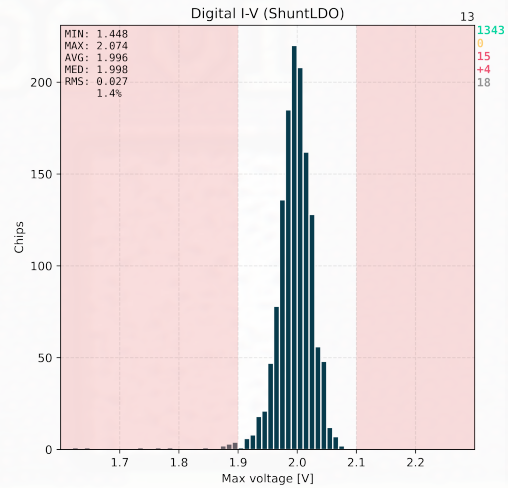


Figure: Serial powering test setups with single-chip cards (top) and with prototype detector modules (bottom).



(a) Example of IV curves obtained for a chip in a serial chain of 10 single-chip cards.

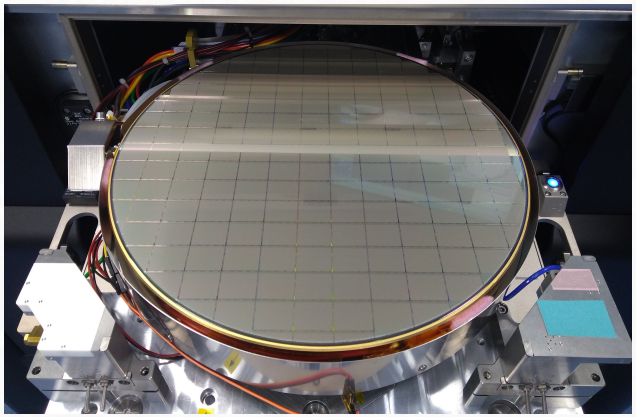


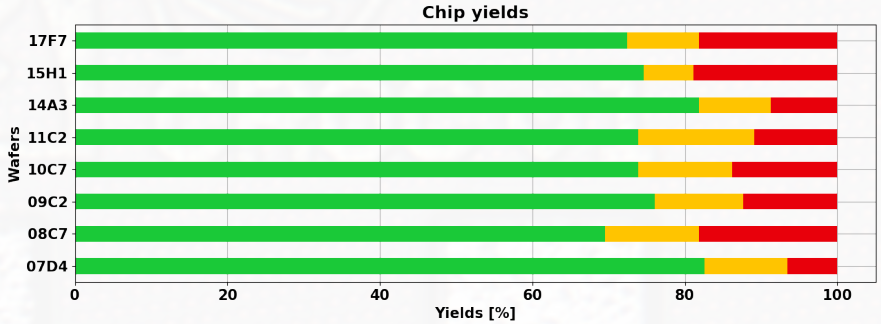
(b) Wafer-level OVP test. Maximum `VIND` (digital domain) distribution on 10 CROCv1 wafers.

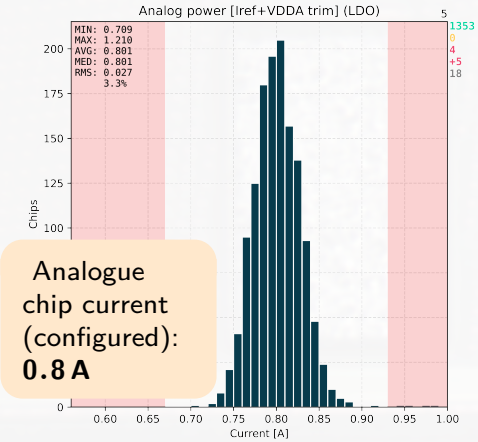
Figure: Shunt-LDO testing results from single-chip cards and from wafer-level testing.

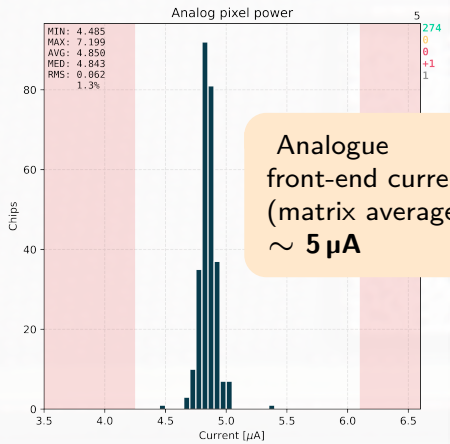
Wafer-level testing

- Engineering run with 20 wafers (2021)
- Tested **14 CROCv1 wafers** in 2022/2023 at INFN Torino
  - Used to produce testing boards and prototype detector modules
  - Additional waferprobing site at Kansas State University under commissioning
- Most important chip functionalities verified at wafer level
- Extensive dataset of **1932 chips**!
- **No major problems found with large statistics measurements**
- **Average chip yield** is approximately **70 %**









Analogue chip current (configured): **0.8 A**

Analogue front-end current (matrix average): $\sim$ **5 µA**

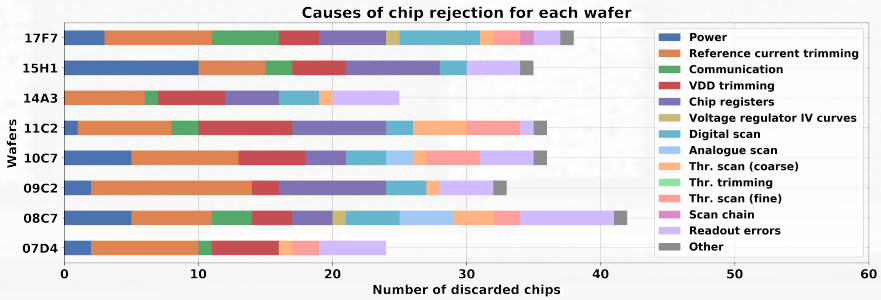


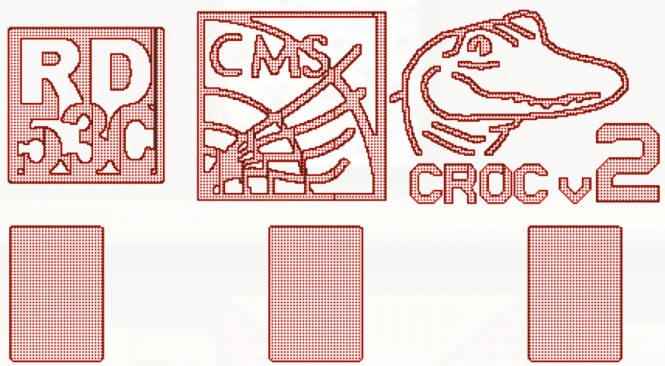
Figure: Examples of wafer-level testing results. Analogue current drawn by the whole chip (left) and by a pixel (average) after configuration (right). Data from 10 wafers (left) and 2 wafers (right).

Figure: **CROCv1 wafer** (138 chips; $\varnothing = 30$ cm); **Chip yields** for several tested wafers; Breakdown of **chip rejection causes**.

Towards the CROCv2

- Successful testing and characterisation campaign on the CROCv1 chip
  - Thoroughly tested and characterised the prototype chip
  - A few improvements have been introduced in the **production version (CROCv2)**
- Currently testing the **RD53C-ATLAS/ITkPixV2** chip (wafers received in July 2023)
  - First of the two RD53C chips to be submitted (March 2023)
  - Promising first results: several improvements in common with the **RD53C-CMS/CROCv2** chip have been verified
- (Brief) **CROCv2** status:
  - **Sign-off review recently performed (29 September)**
  - **CROCv2 will be submitted soon**
- More information on **RD53C and CROCv2 development** in the presentation by Luca Pacher:

Design and characterization of RD53C production chips for ATLAS and CMS pixel upgrades at HL-LHC



Conclusions

- The **CMS Readout Chip** is the result of 10 years of development by the **RD53 Collaboration**
- **Extensive testing and characterisation campaign** for the **prototype chip** (2021-2023)
  - Its requirements have been verified in several different operating conditions
  - Tests and characterisation performed with single-chip cards, prototype detector modules, and at wafer-level
  - Several irradiation, SEE, and test beam campaigns have been carried out
- The chip **satisfies the requirements** for operating at **High-Luminosity LHC**
  - The chip is radiation tolerant at least up to 1 Grad ✓
  - Fast recovery from single-event upsets always possible; no power cycles needed ✓
  - The analogue front-end can be operated at low thresholds, low temperatures, and high TID ✓
  - Very high hit rates can be efficiently processed ✓
  - Serial powering mode can be used to reduce material budget from cabling ✓
- The **production version** of the chip (**CROCv2**) will be **submitted soon**

Backup slides

The CMS detector at the Large Hadron Collider

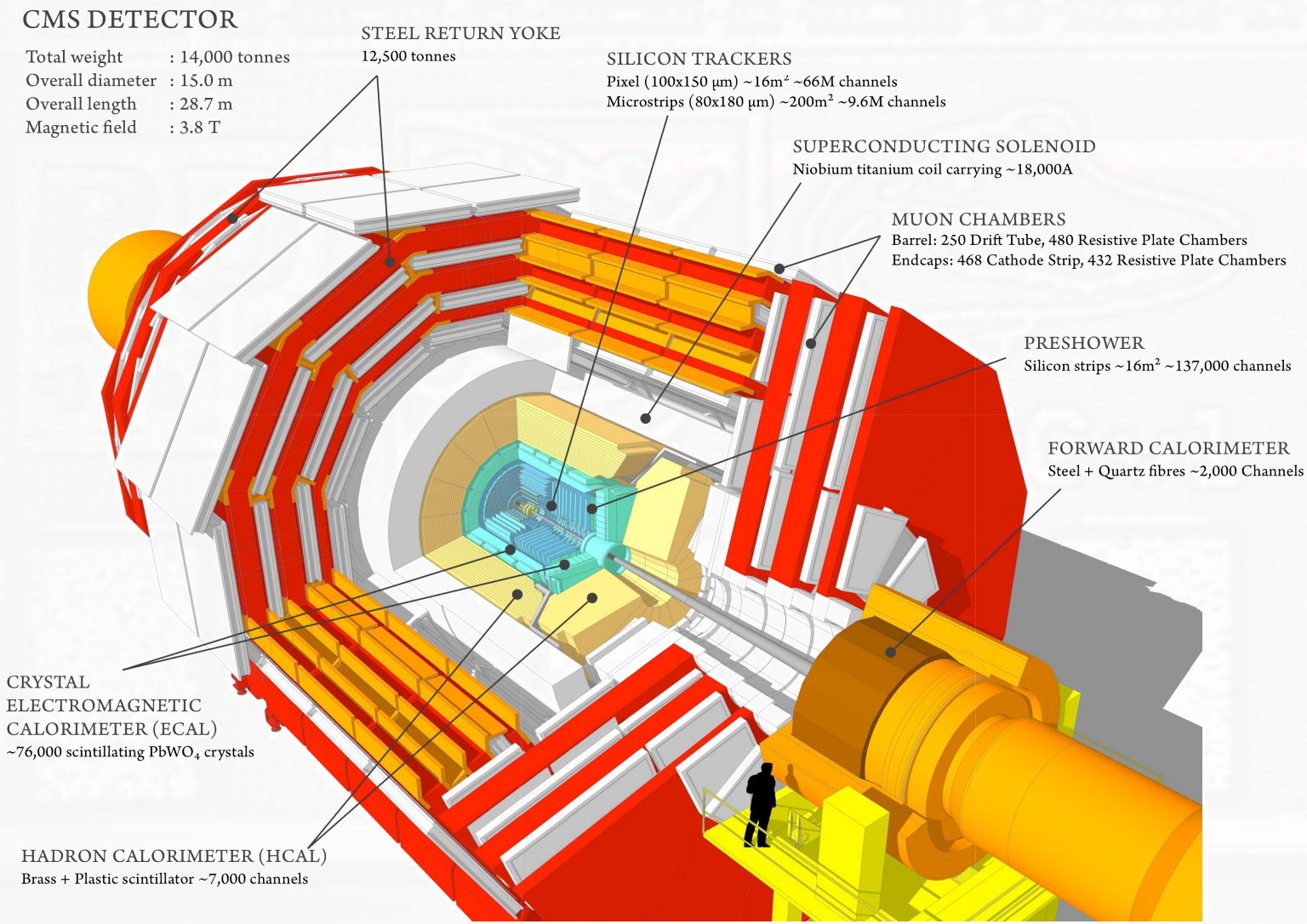


Figure: Layout of the CMS detector at the LHC.

The High-Luminosity LHC upgrade at CERN

- Instantaneous luminosity $[10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}]$: $2 \rightarrow 5$ to 7.5
- Concurrent interactions (pileup) in pp collisions: $\sim 50 \rightarrow 140$ to 200
- Long Shutdown 3: 2026-2028
  - ATLAS and CMS upgrades

Figure: High-Luminosity LHC schedule as of February 2023.

LHC long-term schedule

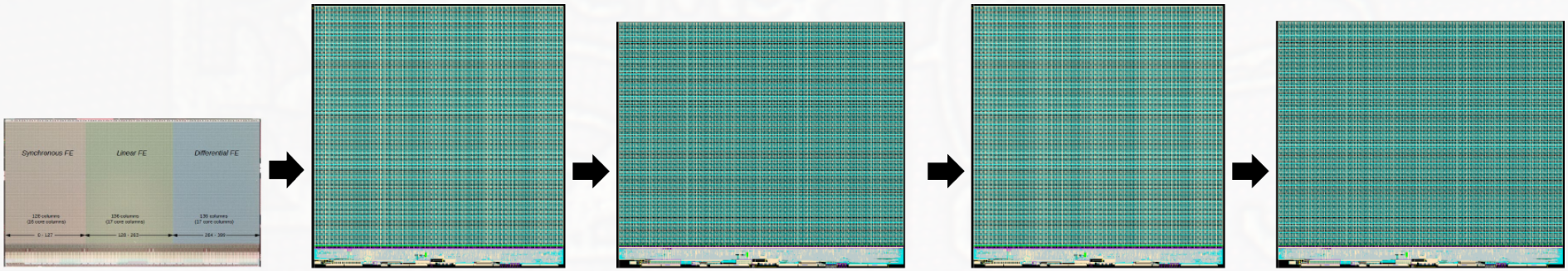
Figure: Long-term schedule for the Large Hadron Collider as of April 2023.

Radiation hardness requirements for High-Luminosity LHC

	RUN 4 (800 fb^{-1})		RUN 5 (1300 fb^{-1})		RUN 4+5 (2100 fb^{-1})		RUN 4+5+6 (3000 fb^{-1})		Not in Chamonix 2022 (4000 fb^{-1}) For reference only	
	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad	1E16 1 MeV neq	Grad
TBPX L1	0.69	0.36	1.12	0.58	1.81	0.93	2.58	1.34	3.44	1.78
TBPX L2	0.18	0.11	0.29	0.17	0.48	0.28	0.68	0.40	0.98	0.54
TFPX R1	0.46	0.31	0.75	0.49	1.22	0.79	1.74	1.13	2.32	1.5
TFPX R2	0.21	0.14	0.35	0.23	0.57	0.37	0.82	0.53	1.09	0.71

Figure: Radiation hardness requirements for the CMS Inner Tracker for High-Luminosity LHC.

RD53 chip versions



RD53A
- August 2017

RD53B-ATLAS (ItkPix_V1)
- March 2020

RD53B-CMS (CROC_V1)
- June 2021

RD53C-ATLAS (ItkPix_V2)
- March 2023

RD53C-CMS (CROC_V2)
- Sept. 2023

Figure: RD53 chip versions.

The CMS Readout Chip (CROC): hit readout

- Signals are amplified by the in-pixel **analogue front-end**
  - **Charge-sensitive amplifier** (CSA)
  - **Krummenacher feedback** to return to baseline and for leakage current compensation
- CSA output fed to low-power, in-pixel **comparator**
  - Global threshold set with 10 bit DAC
  - Local (per pixel) threshold adjustment with 5 bit DAC
- In-pixel **4 bit time-over-threshold (ToT)** information
  - 40 MHz clock with single or dual-edge counting
  - 8 × (4 bit) ToT memories per pixel
- 8 × (9 bit) **timestamp/latency memories** per pixel region (4 pixels)
  - Maximum configurable latency: 511 bunch crossings
- **Token-based readout** of pixel regions; core columns (8 pixels wide) are read out in parallel
- Hits are compressed with **binary-tree encoding** and further processed by the digital chip bottom until Aurora frames are built

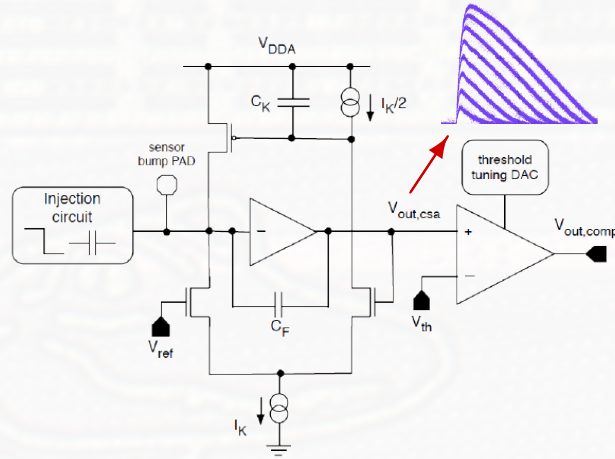


Figure: Simplified schematic diagram of the analogue front-end of the CMS Readout Chip.

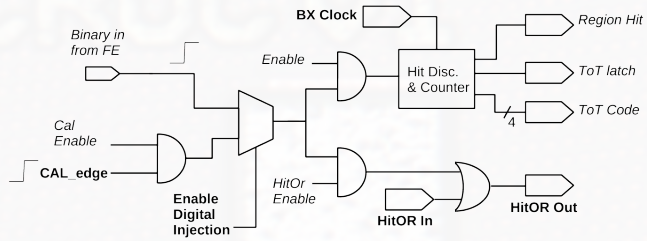


Figure: Pixel hit logic.

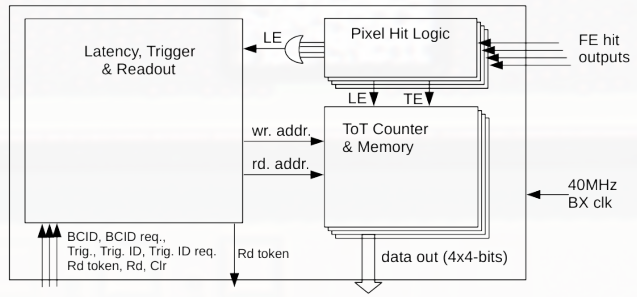


Figure: Pixel region logic.