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Testing and characterisation of the prototype readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker

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This talk describes the characterisation and validation campaign of the prototype of the CMS Readout Chip (CROC), a 65 nm CMOS pixel readout ASIC for the CMS Inner Tracker upgrade for High Luminosity LHC. This validation campaign includes tests with single-chip and multi-chip modules, irradiation campaigns, test beams and wafer-level tests. The main results obtained in the testing of the CROC prototype will be outlined. Key improvements and fixes that have been implemented in the final version of the chip before the summer 2023 submission will be described.

Summary (500 words)

The CMS Readout Chip (CROC) is a 65 nm CMOS hybrid pixel readout chip for the High Luminosity LHC upgrade of the CMS Inner Tracker. The new detector will be instrumented with approximately 13e3 of these readout chips, covering an area of about 5.2 mˆ2.

The chip must be able to withstand very high radiation doses (500 Mrad) and hit rates (3 GHz/cmˆ2 on the innermost tracking layer) during operation. Moreover, it must handle an increased sensor granularity (2500 µmˆ2 pixels) with respect to current detectors and operate at low detection thresholds (1000 e-).

In order to fulfill these challenging requirements, the RD53 collaboration has been established in 2013, with the task of developing the readout chips for both the CMS and ATLAS inner tracker upgrades for HL-LHC. The collaboration first studied the radiation hardness of the 65 nm CMOS technology and found it suitable for the development of the chip. After that, the required radiation-hard IP blocks (ADC, DACs, PLL, analogue pixel front-end, ...) were developed and validated.

A prototype (CROCv1) has been submitted in 2021. The chip includes a low-power, linear analogue front-end, charge measurement with a time-over-threshold counter, several mitigations for radiation-induced problems (such as the triplication of important storage elements) and a novel powering scheme designed to reduce the material budget of the detector. The mitigation of radiation-induced effects in storage elements is particularly important, given that, during operation, it is estimated that the data in about 100 storage elements will be corrupted by radiation every second even with triple redundancy.

Twenty wafers of the prototype chip have been produced, amounting to 2760 chips. Several of these wafers have been used to produce single-chip cards, detector module prototypes, and for sensor hybridisation. More than half of these wafers have been subjected to wafer-level testing in order to discard the dies with manufacturing problems or insufficient performance and to commission the waferprobing facilities for production testing.

The prototype chip has been thoroughly studied and its suitability for operation at HL-LHC has been assessed. The chip has been studied in single-chip assemblies, in prototype detector modules with bump-bonded sensors, and at wafer-level. The performance of fresh and irradiated CROCv1 ASICs has also been studied in several beam tests, bump-bonded to sensors with different technologies (planar, 3Ds). The characterisation and verification campaign has, overall, demonstrated the radiation resistance of the chip and its performance, but a few important improvements have been identified. These improvements have been implemented in the final version of the chip, before the summer 2023 submission.

In this talk, key results from the characterisation and validation of the CROCv1 will be described. The submission of the final version of the chip will also be mentioned, along with the most important improvements and fixes that have been implemented in the CROCv2.

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