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SET sensitivity study of a VCRO-based PLL for HL-LHC ATLAS HGTD

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We report the characterization of the Single Effect Transient (SET) sensitivity of an analogue Phase-Locked Loop under a 63 MeV proton beam of instantaneous fluence 10ˆ10 protons/cm^2/s. The clock generator is embedded in a front-end ASIC, namely ALTIROC designed in CMOS 130 nm, reading out Low-Gain Avalanche Diode (LGAD) for the High-Luminosity Large Hadron Collider (HL-LHC). Observed SET-induced phase jumps allow the estimation of the total cross-section of the PLL. Results are extrapolated to the HL-LHC radiation conditions.

Summary (500 words)

As part of the ATLAS experiment Phase-II upgrade, the High Granularity Timing Detector (HGTD) will offer a time resolution better than 35 ps RMS per hit for collected charges over 10 fC. An internal PLL provides 1.28 GHz clock from which is derived a 40 MHz clock used for the timing measurement. Designed in CMOS 130 nm as part of the front-end read-out ASIC ALTIROC, the PLL must therefore exhibit a low sensitivity to Single-Event Transient (SET) so as not to corrupt the clock reference and thus the timing data. Furthermore, output data are serialized at a maximum rate of 1.28 Gbps, but serializer logic is prone to failures such as bit flips when the clock exhibits transient phase errors. Thus, the reliability of the serializer depends on the SET sensitivity of the PLL. Therefore, the phase detector and the feedback clock divider were triplicated while the charge pump, the low-pass filter and the voltage-controlled ring oscillator were not specifically SEE-hardened.

Proton-beam campaigns were conducted in the ARRONAX facility (Nantes, France) which provides a 63 MeV proton with an instantaneous fluence of 10ˆ10 protons/cm^2/s (i.e. 2 to 3 orders of magnitude higher than HL-LHC conditions). The proton flux was estimated measuring both the beam diameter with a radio-chromic film and the current of a photomultiplier from an ionization chamber. Tests reported a large variety of SET occurring predominantly in the VCO, identified as frequency transients and in other parts of the design. Peak phase errors up to several tens of nanoseconds were measured with a total cross-section of 4 10-12 cm^2 (accounting for all phase error amplitudes observed).

With a 10 ps RMS dominant random jitter, the PLL jitter envelop can easily be disturbed by SET, even by low amplitude phase errors. Consequently, the peak phase error is not an appropriate metric for the figure of merit of the SET sensitivity for HGTD. Instead, the timing requirements call for reducing the fraction of the time the PLL provides a wrong clock phase. This estimation can be obtained knowing both the total cross-section and the recovery time of the phase error. Measurements have shown a recovery time below 5 µs. Using conservative data regarding the HL-LHC radiation environment (safety factor of 3 for SEE, giving a flux of 1E8 cm-2s-1 for hadrons above 20 MeV), the time corruption rate can be extrapolated to 5 minutes per year of operation of the full HGTD detector (16k PLL running simultaneously). Note that the cross-section estimation relies strongly on the phase error sensitivity. As SET affecting the VCRO produce large phase deviations due to its intrinsic large voltage-to-frequency gain, SET phase jumps were detected using a Lecroy Waverunner 640Zi. Using the "smart trigger"time interval functionality, the oscilloscope allowed for a period deviation sensitivity of ±200 ps around the nominal period of the 40 MHz clock monitored.

Details of the triplication implemented in this PLL along with characterisation results will be presented.

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