UK Research and Innovation

UNIVERSITY OF LIVERPOOL

Measurement of UKRI–MPW0 after irradiation: An HV–CMOS prototype for high radiation tolerance

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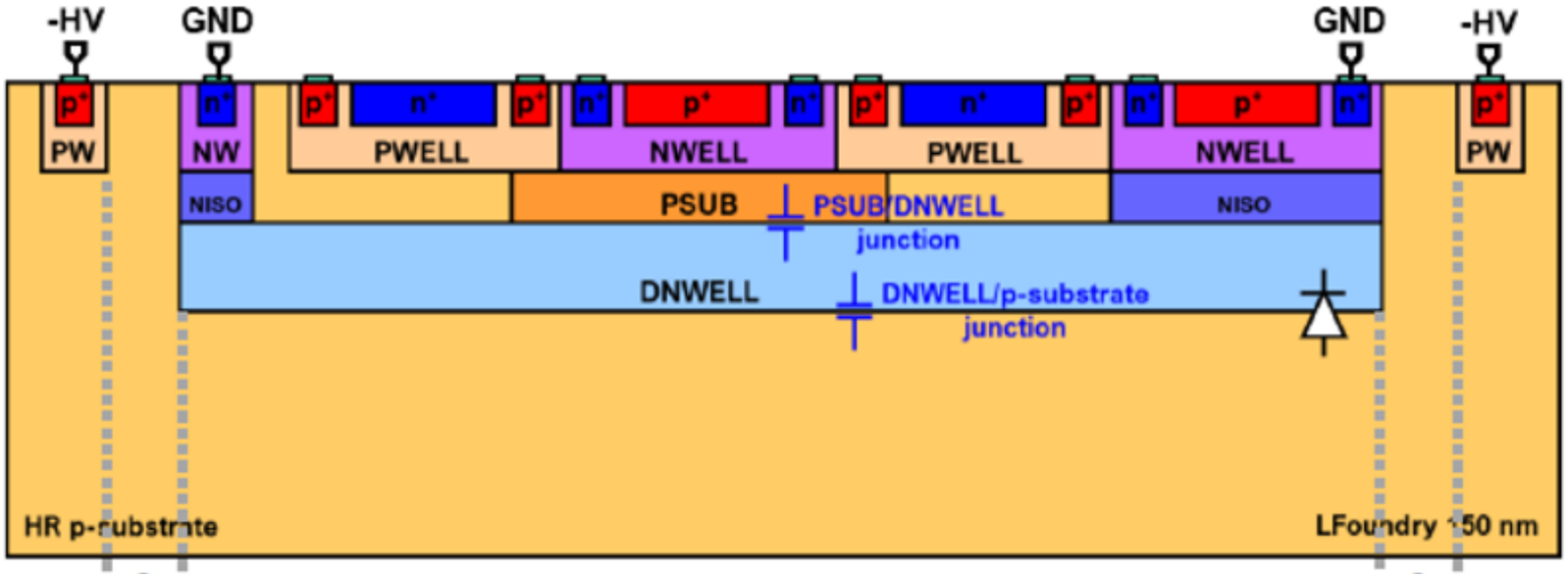
Introduction: HV-CMOS sensor

- Sensing diode and readout electronics are in the same substrate (monolithic).
- High bias voltage forms a wide depletion region (radiation tolerant).
- Single layer structure → low cost, low material budget.
- Both NMOS and PMOS transistors can be implemented (full CMOS).



Cross-section of a typical large fill-factor HV-CMOS sensor

Motivation: radiation tolerance

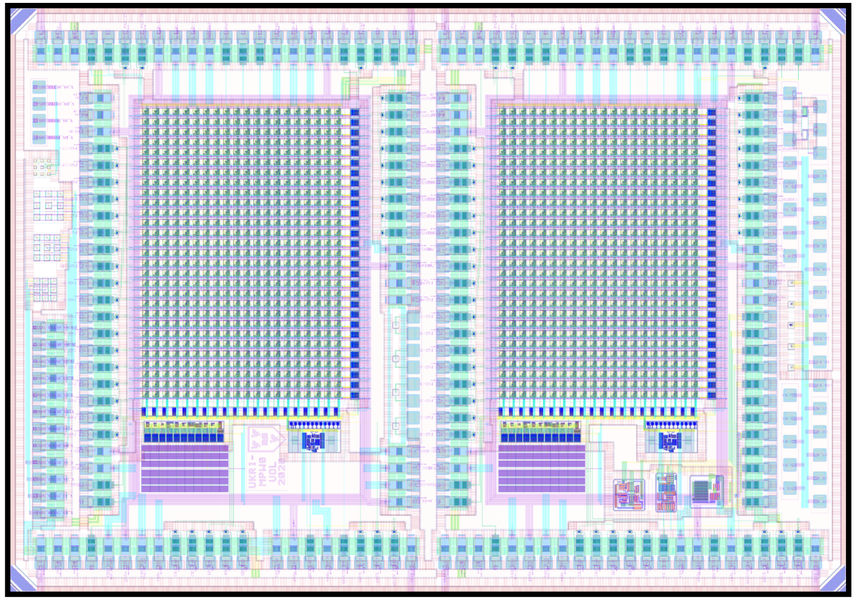
- Much higher luminosity ($> 5\times10^{34}$ $cm^{-2}s^{-1}$) in future experiments.
- To survive radiation damage after long operation, pixel trackers must have higher radiation tolerance.
- The table below compares the best achieved HV-CMOS performance with the tracking detector requirements for future experiments.

	HV-CMOS performance	**HL-LHC**	**FCC-hh**
Radiation tolerance	2×10^{15} n_{eq}/cm^2	10^{16} $n_{eq}/cm^2/y$	10^{16} - 10^{17} $n_{eq}/cm^2/y$
Pixel size	50×50 μm^2	50×50 μm^2	25×50 μm^2
Time resolution	3.7 ns	0.2* - 1000 ns**	~ 100 ps
Thickness (material budget)	50 μm	0.1%** - 2% X_0/layer	1% X_0/layer

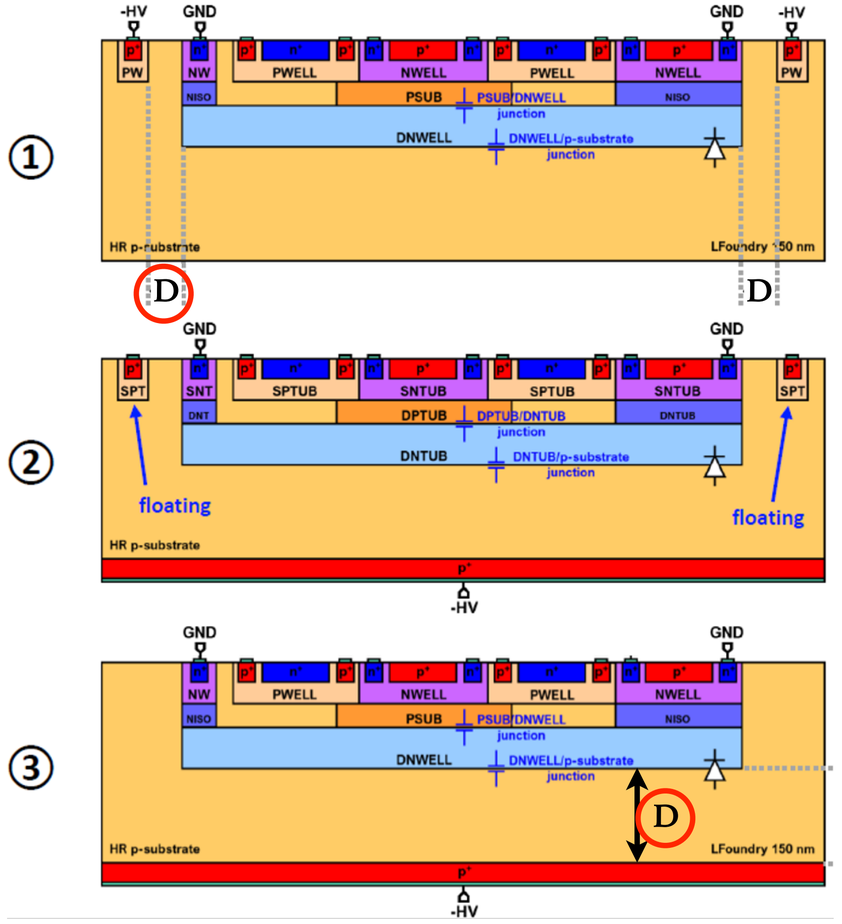
*LHCb requirement; **ALICE requirement

UKRI-MPW0: new cross-section

- 3 different schemes for high voltage biasing:
  - ① HV biased from the topside only (commonly used);
  - ② HV biased from the backside with floating topside contacts (has been tested);
  - ③ HV biased from the backside, no topside contacts (first use in UKRI-MPW0).



UKRI-MPW0



- Depletion depth $d \propto \sqrt{\rho \,.\, V_{bias}}$.
- High V_{bias} maintains a wide depletion region after radiation → better radiation tolerance.

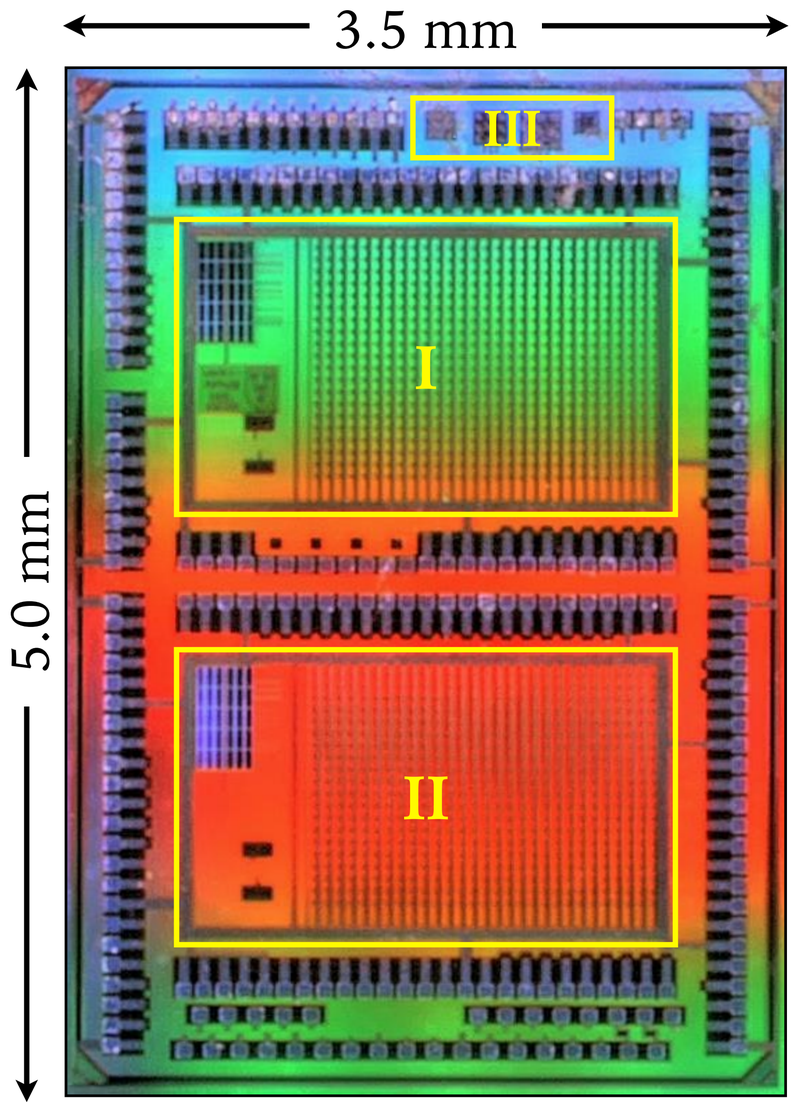
UKRI-MPW0: chip details

I. A 20 × 29 pixel matrix with 3 pixel flavours (using traditional linear transistors);

II. Pixel matrix with 2 Enclosed Layout Transistors (ELT) inside each pixel for TID tolerance;

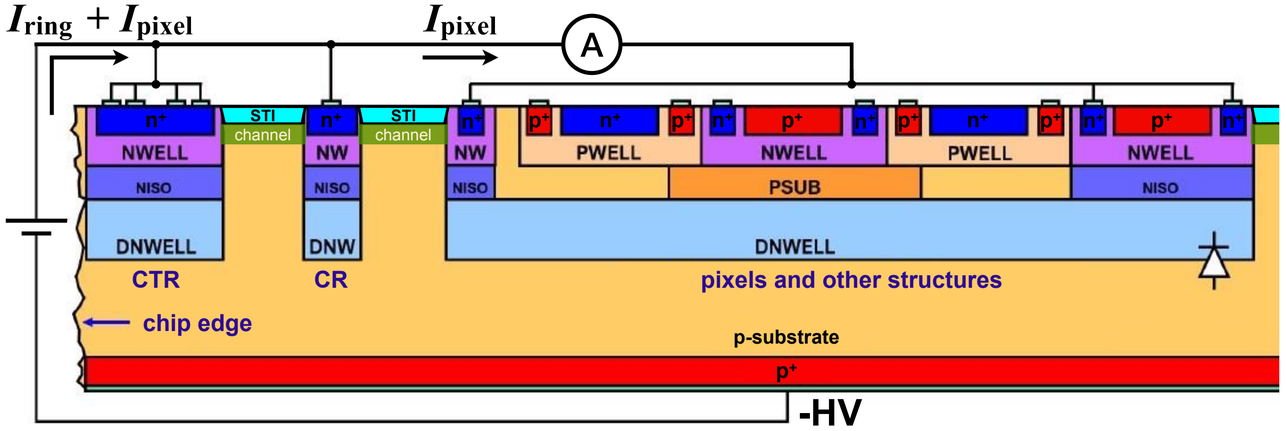
III. Test structures for I-V and Edge-TCT.

- LFoundry LF15A process (150 nm).
- Two wafers with high resistivity of 1.9 kΩ·cm.
- Thinned to 280 μm using TAIKO grinding.
- Wafer 1: p^+ on the backside was implanted using **beamline** and activated with **Rapid Thermal Annealing (RTA)**.
- Wafer 2: p^+ was implanted by **plasma** and activated with **laser annealing**.

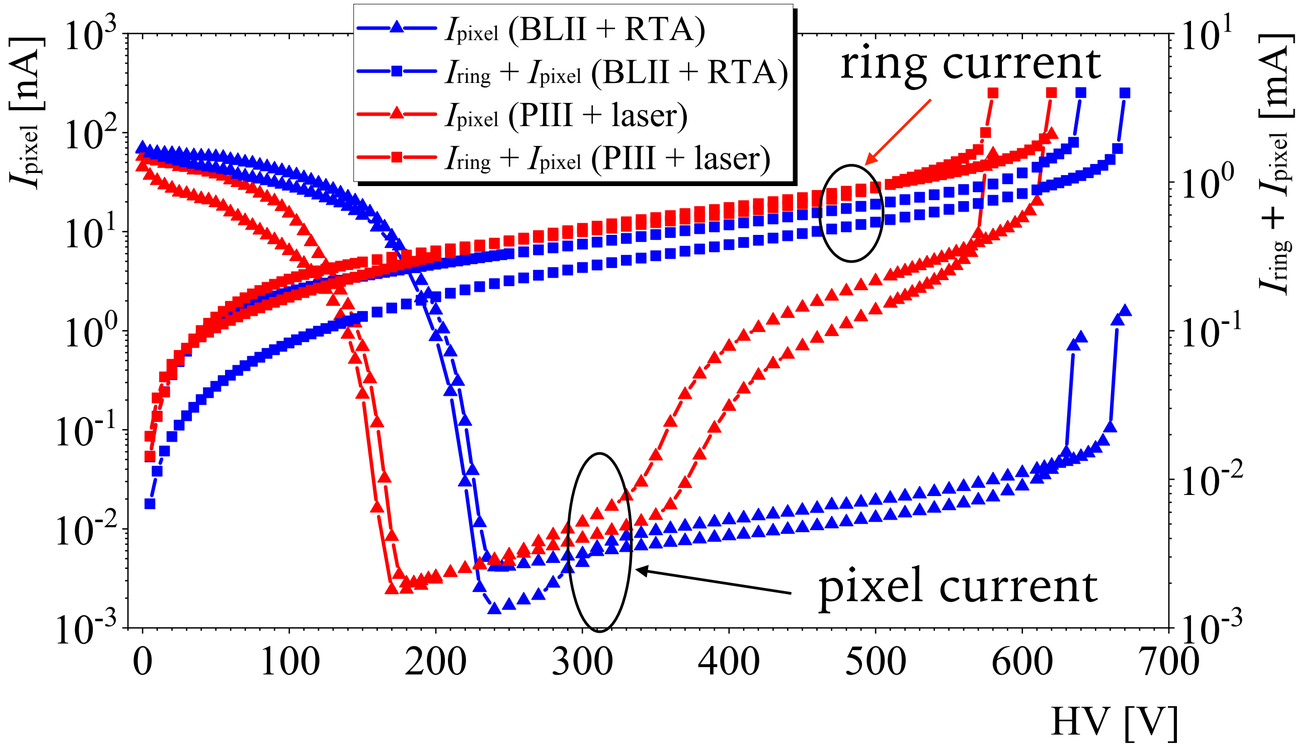


UKRI-MPW0: I-V before irradiation

- N-type rings:
  - ➤ Current Terminating Ring (CTR)
  - ➤ Clean-up Ring (CR)



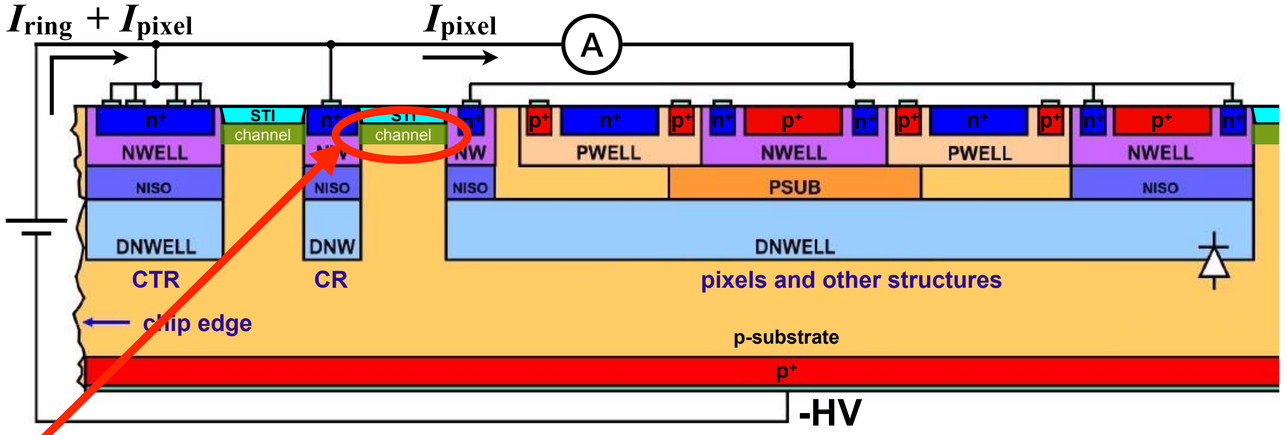
un-irradiated

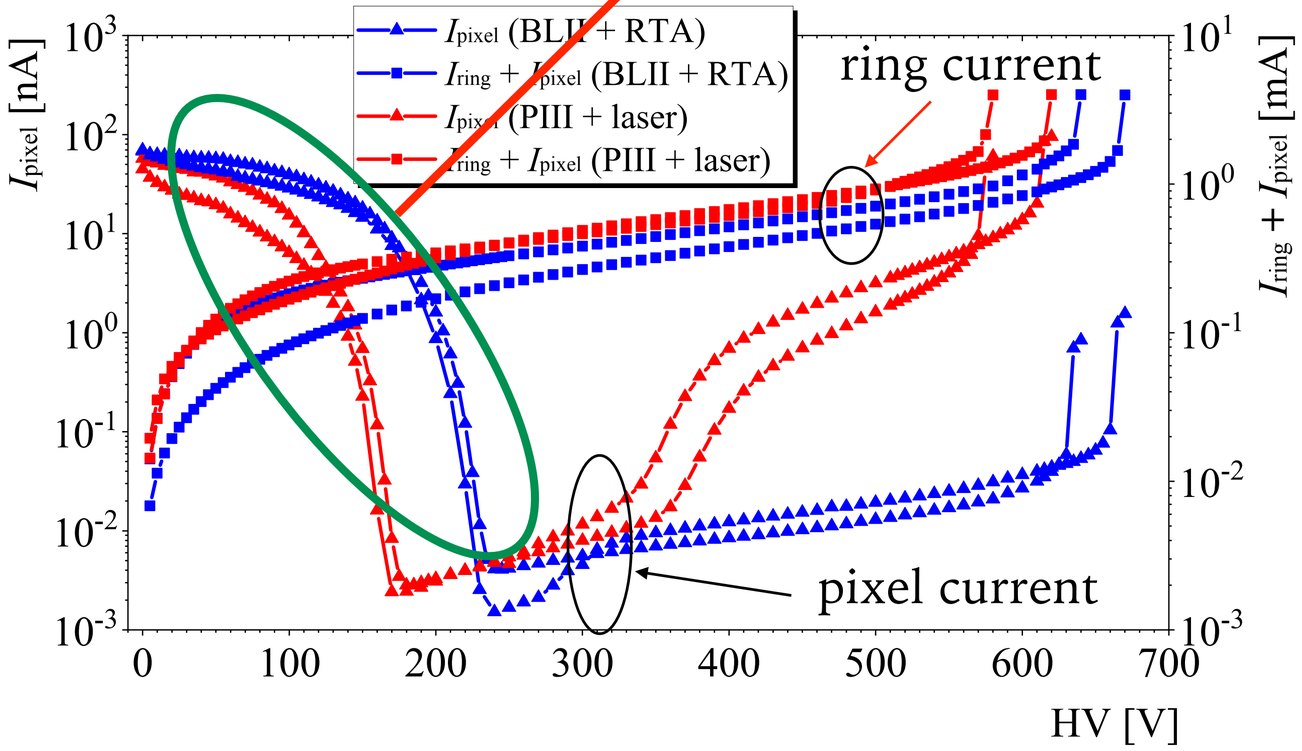


- Reach 4 mA compliance at > 600 V (thermal runaway, not real breakdown).

UKRI-MPW0: parasitic channel

- High pixel current at low bias, caused by a parasitic channel under STI.
- Channel is closed by high bias voltage.

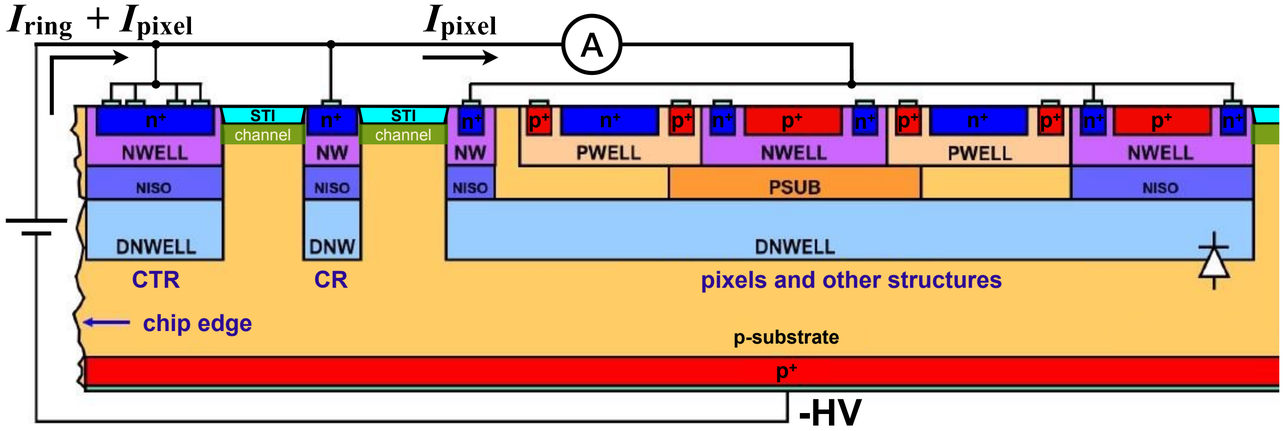




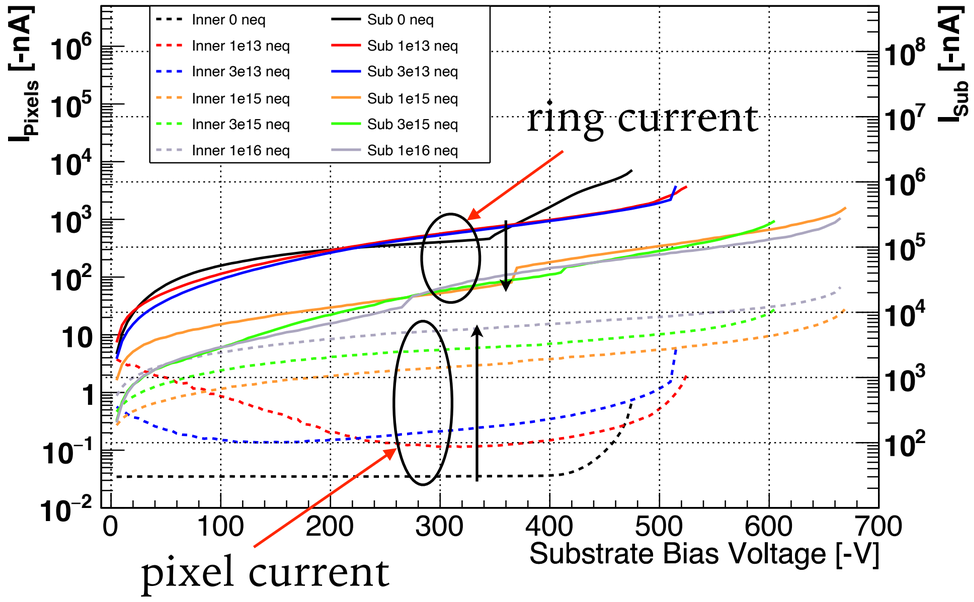
un-irradiated

UKRI-MPW0: I-V after irradiation

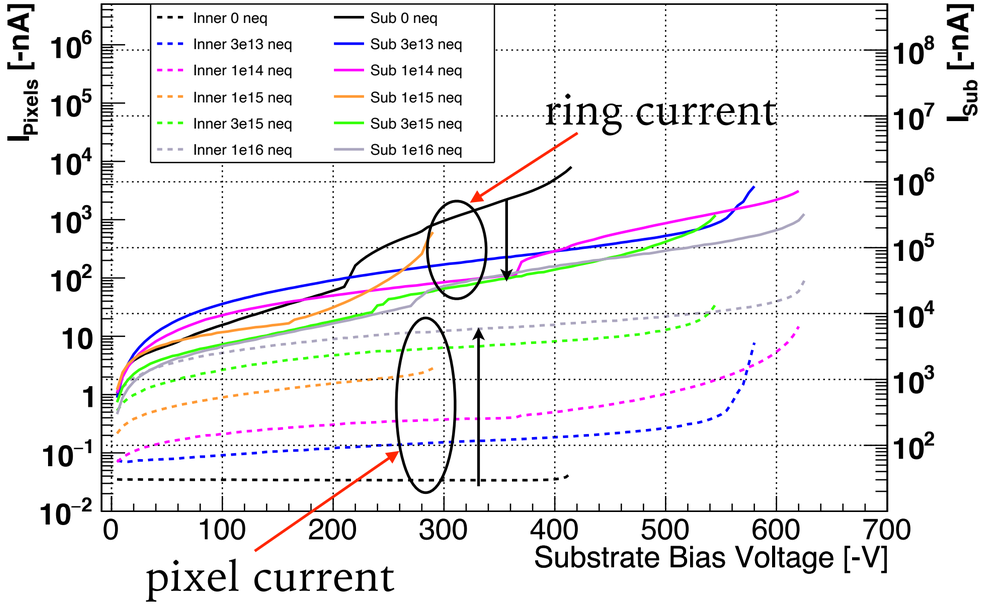
- N-type rings:
  - ➤ Current Terminating Ring (CTR)
  - ➤ Clean-up Ring (CR)
- Higher fluence —> higher pixel leakage current and lower ring leakage current.
- Reach compliance at larger bias voltage.



Plasma + laser annealing

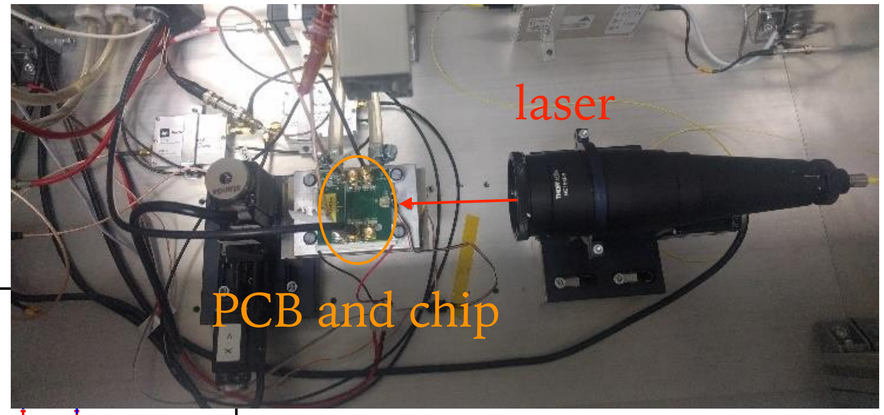


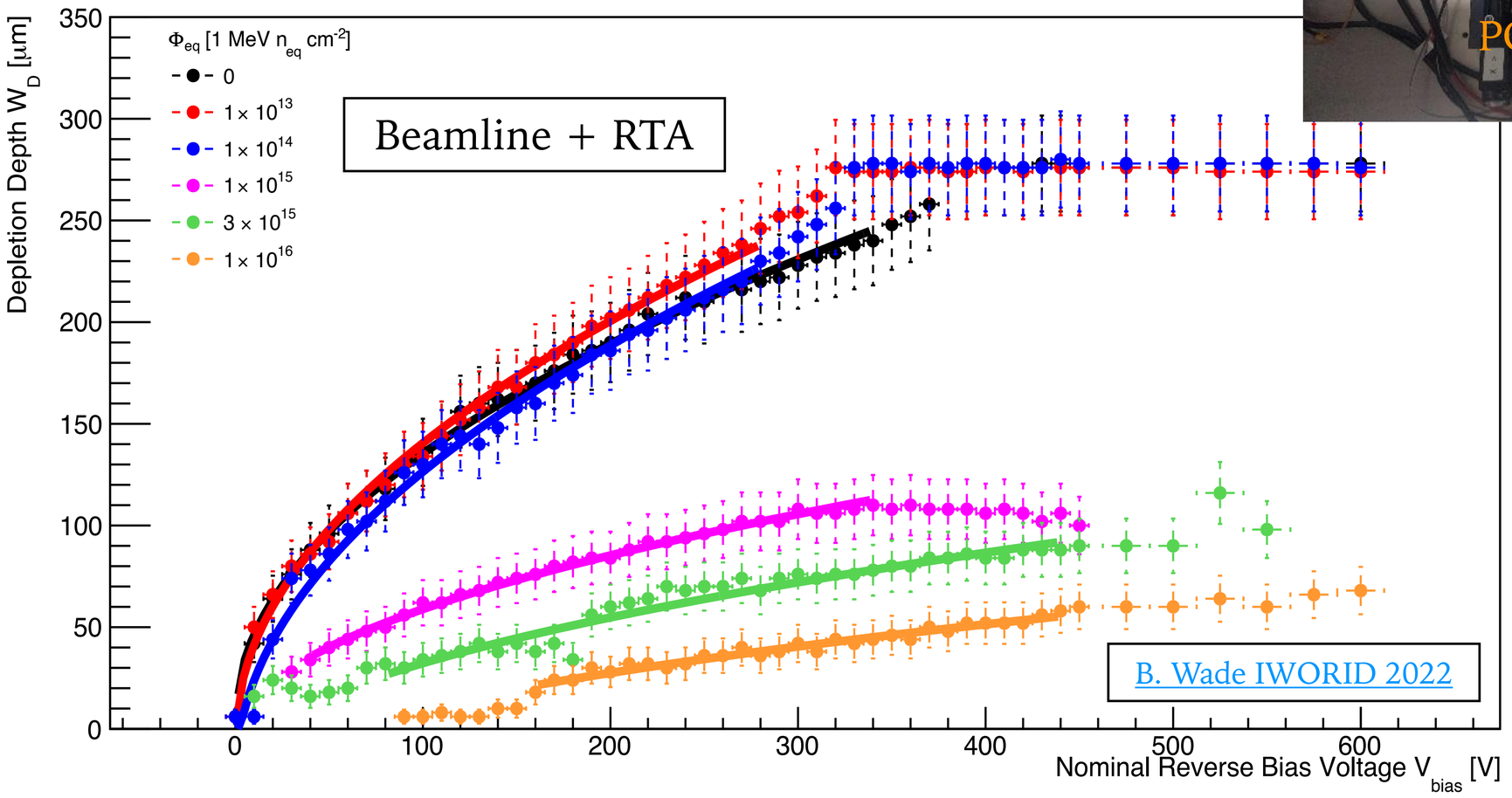
Beamline + RTA



UKRI-MPW0: depletion depth

- Edge-TCT to measure depletion depth at different bias and fluence.

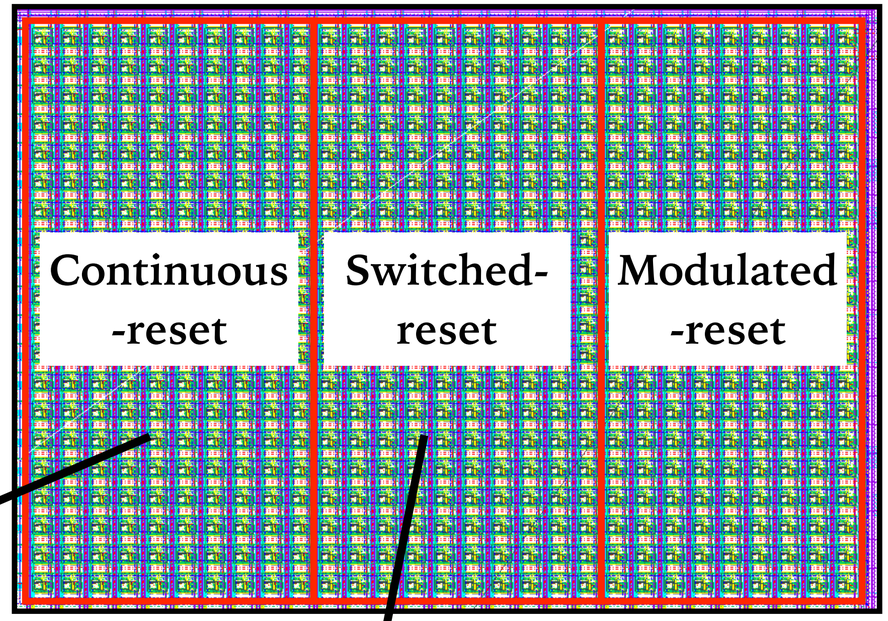


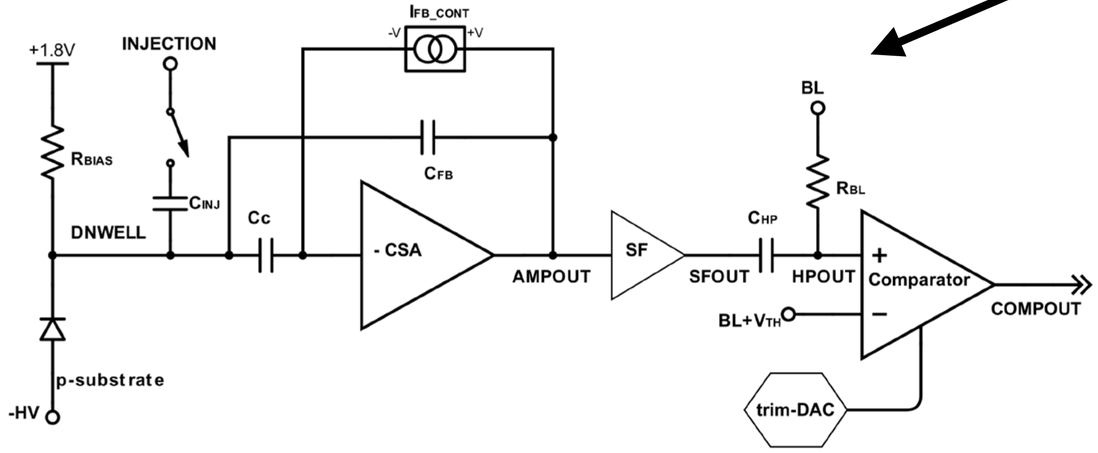


- Chip is fully depleted at 300 V for 1×10^{14} n_{eq}/cm^2 (chip thickness: 280 μm).
- Depletion depth > 50 μm is achieved with 1×10^{16} n_{eq}/cm^2.

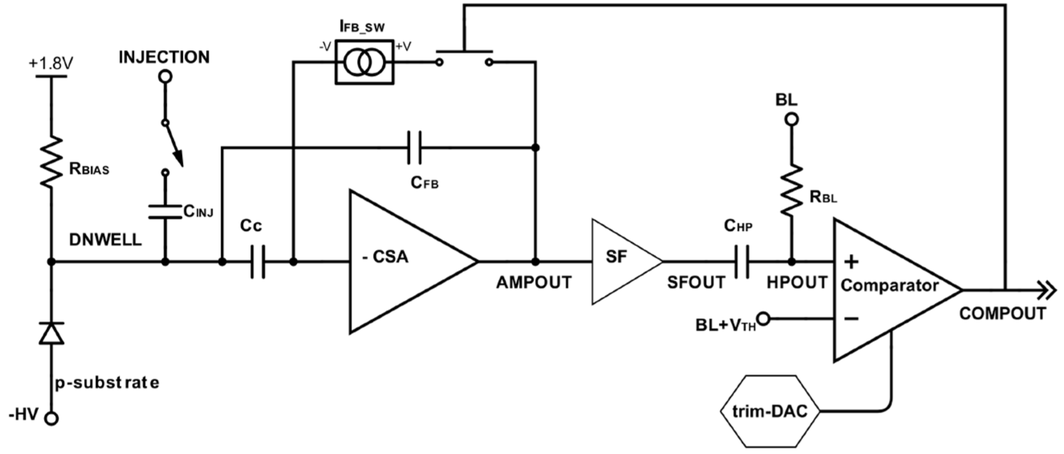
UKRI-MPW0: pixel matrix

- Pixel matrix has three pixel flavours:
  1. Continuous-reset pixel
  2. Switched-reset pixel
  3. Modulated-reset pixel
- Pixel flavours 1. and 2. have been implemented in a previous HV-CMOS prototype RD50-MPW2 (C. Zhang TWEPP 2019).
- Pixel flavour 3. modulates the reset speed based on input charge.



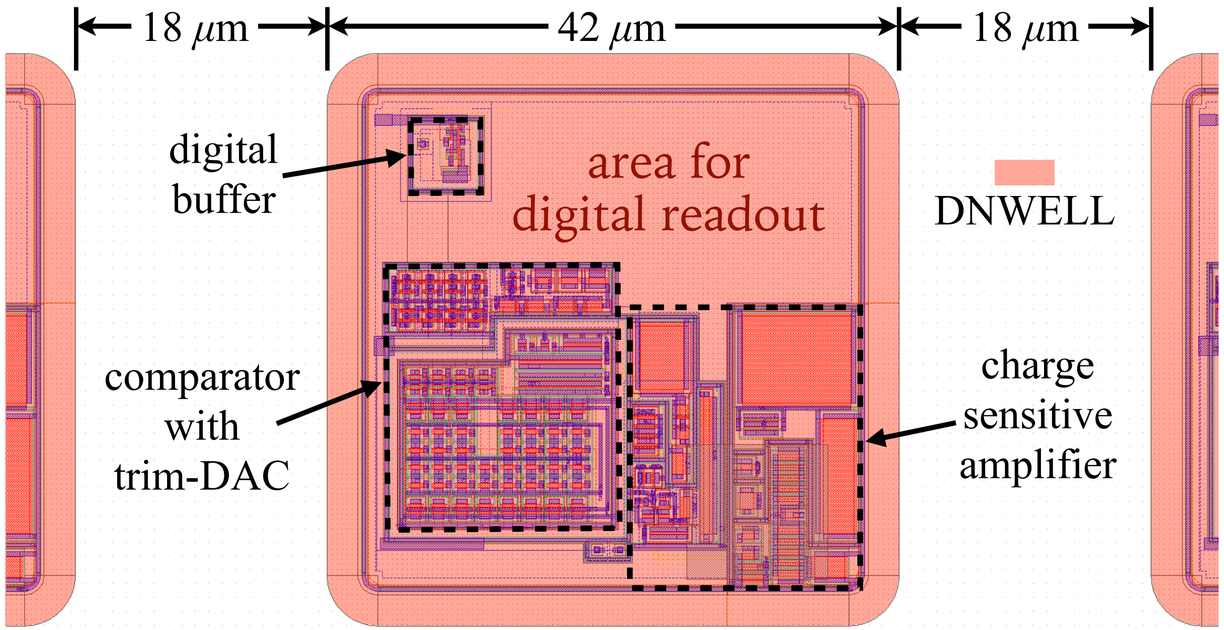


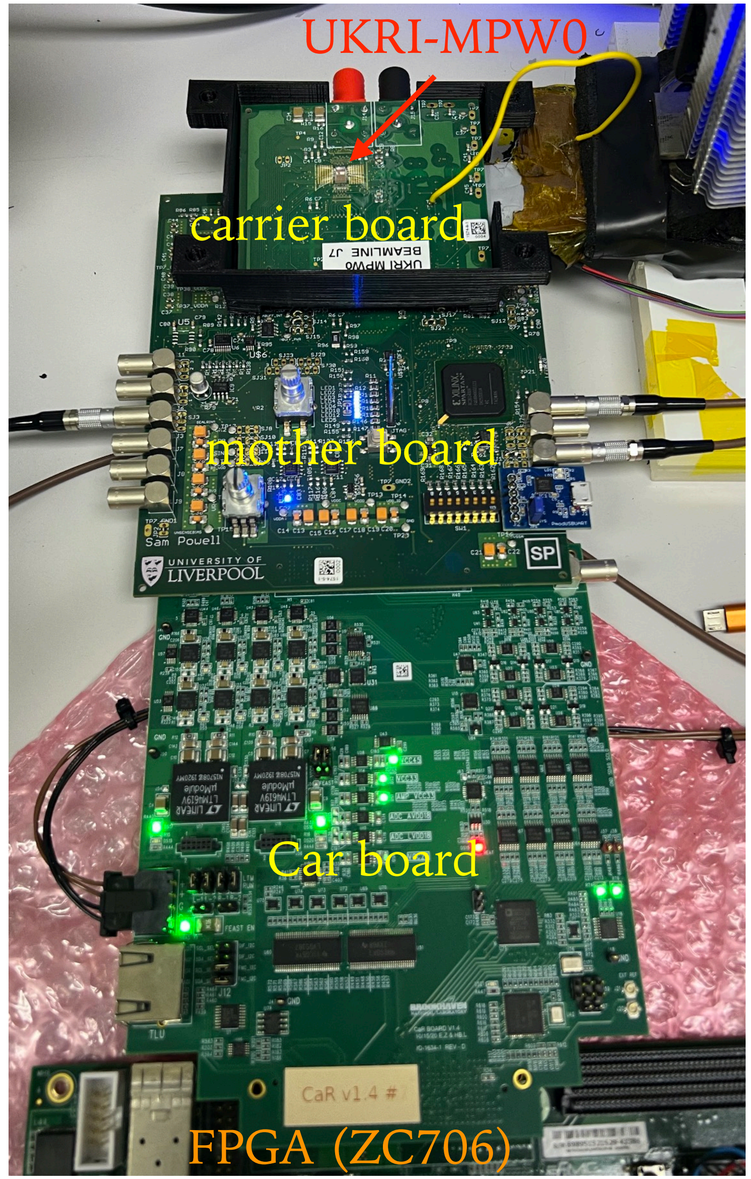
Continuous-reset pixel



Switched-reset pixel (faster response)

UKRI-MPW0: pixel and DAQ

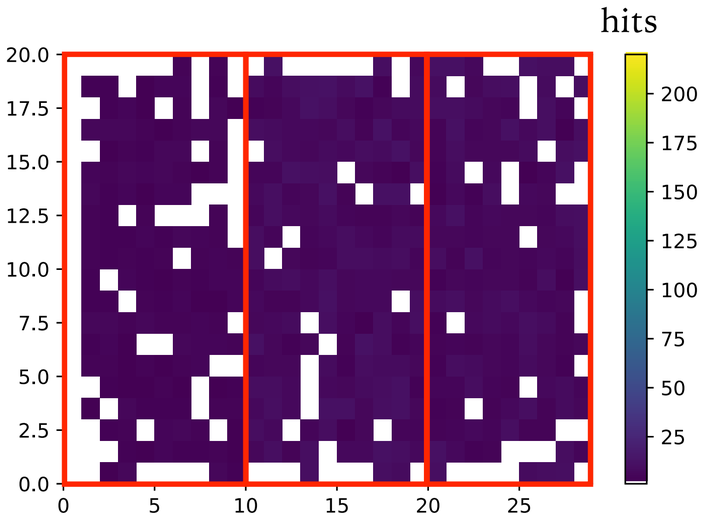




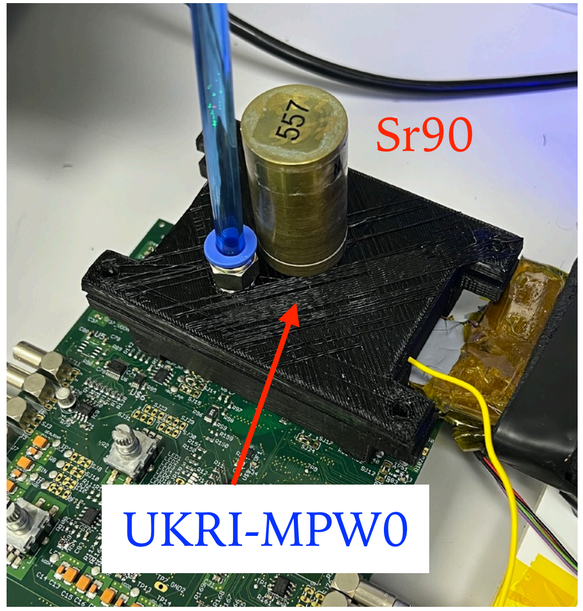
- Pixel comparator output is buffered for readout.
- Each column has own readout pad.
- DAQ is based on **Caribou**.
- Time parameters (ToA, ToT) are digitised off-chip.

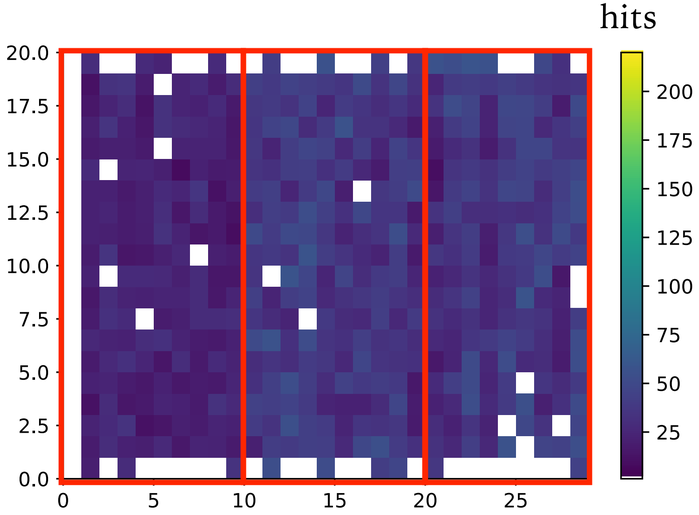
Source hit map

- Used a Sr90 source to plot the number of hits received by pixels over a shutter window of 20 s.
- Hits number increases with High Voltage.
- Pixel flavour in the milder (Switched-reset) detects more hits due to higher gain.

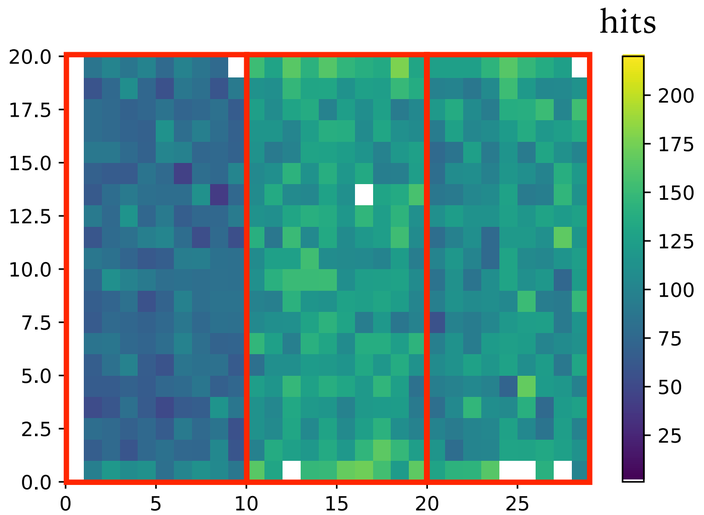


HV = 100 V

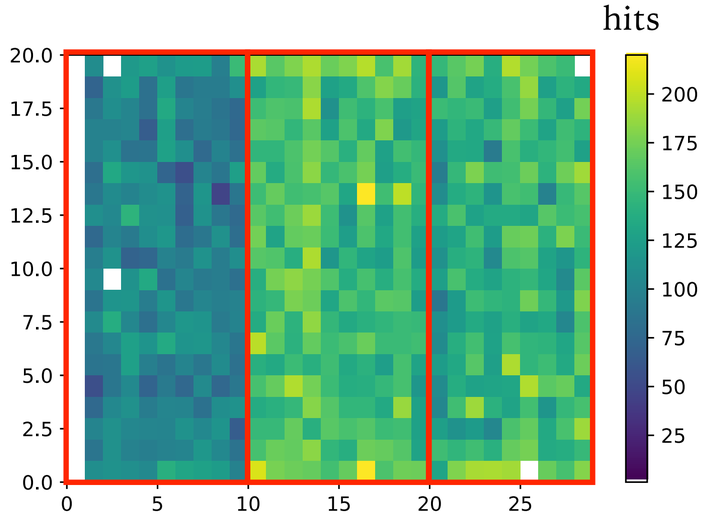




HV = 200 V



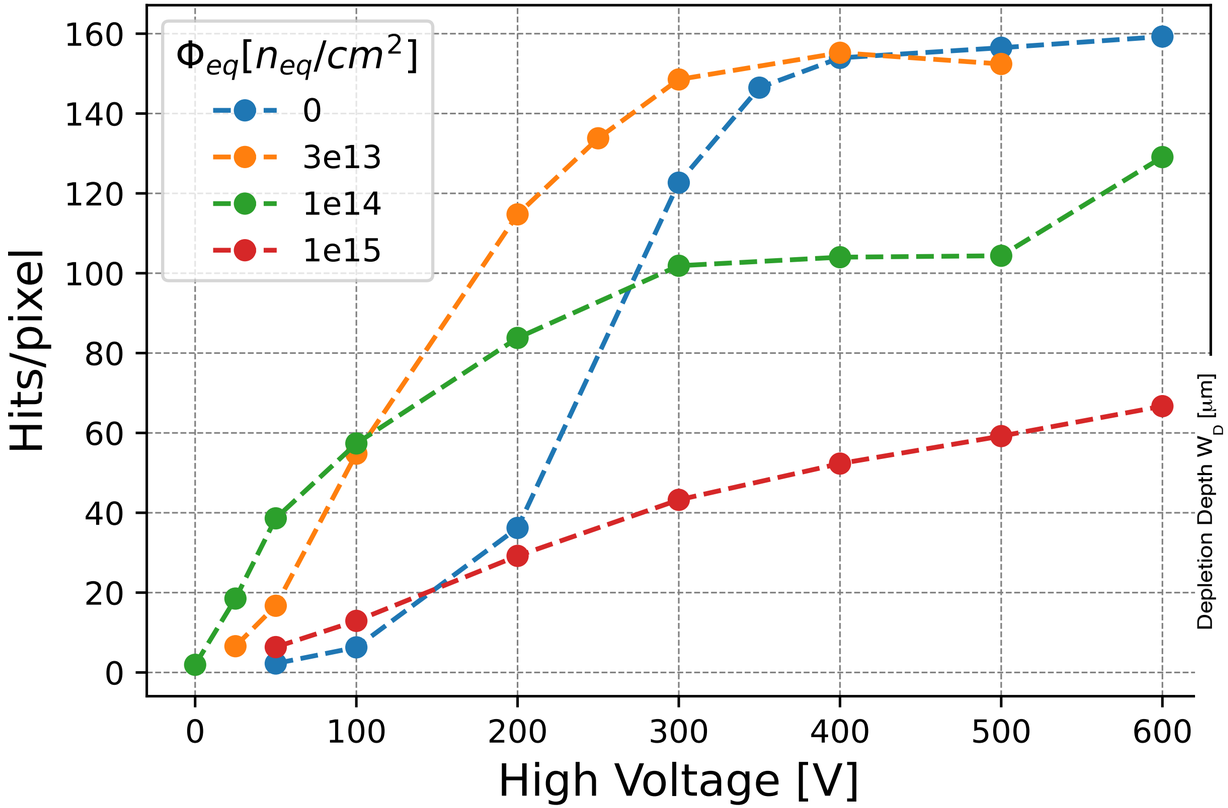
HV = 300 V

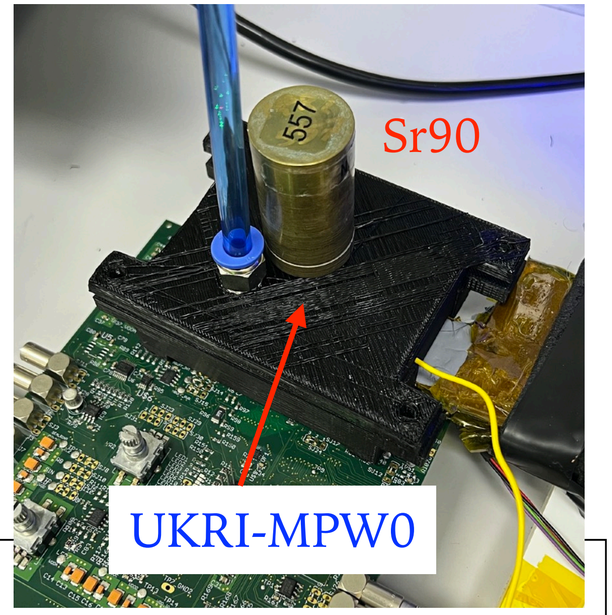


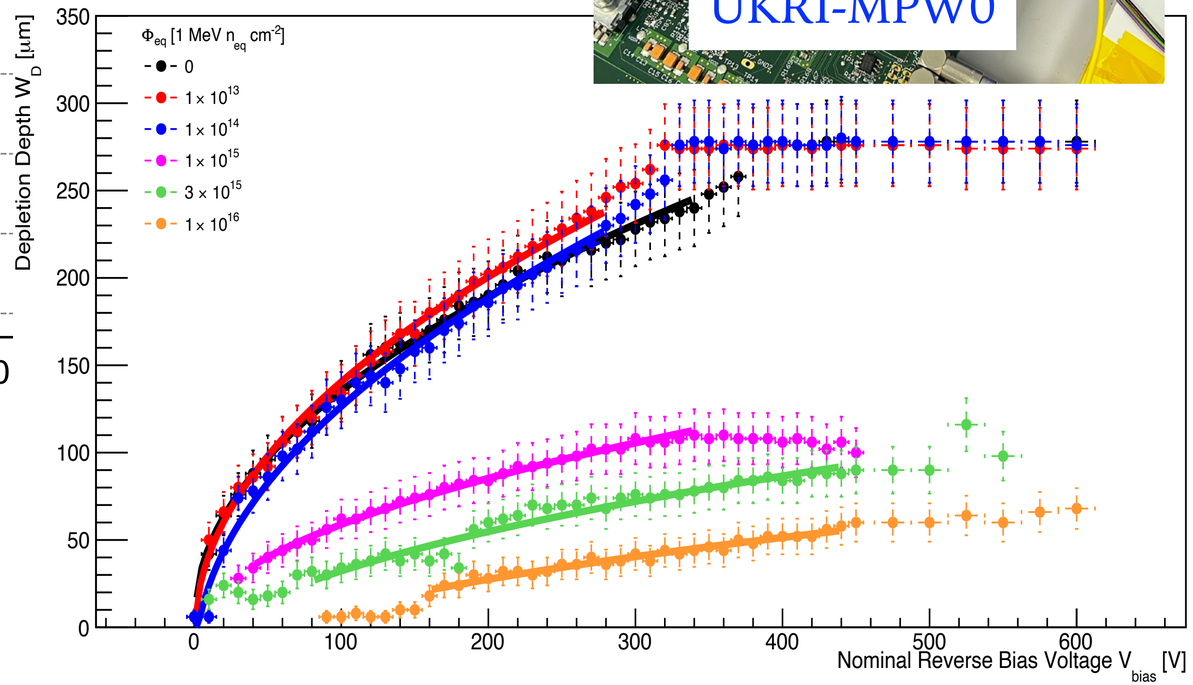
HV = 400 V

Source hits vs HV

- Plot mean hits per pixel with different High Voltages and for different radiation fluence.





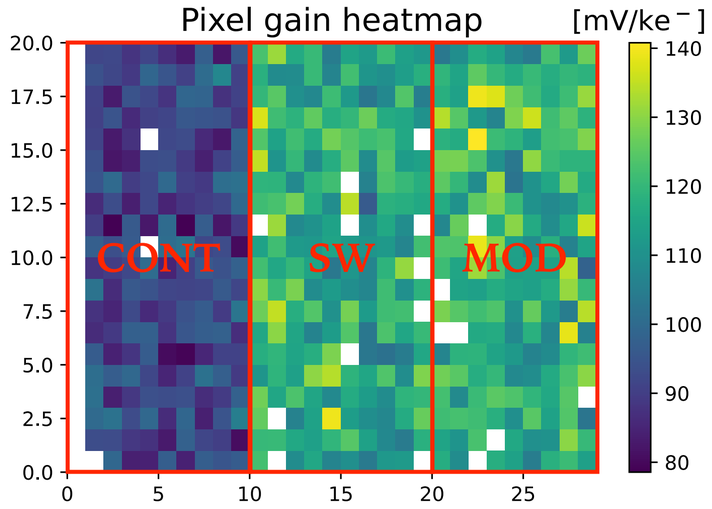


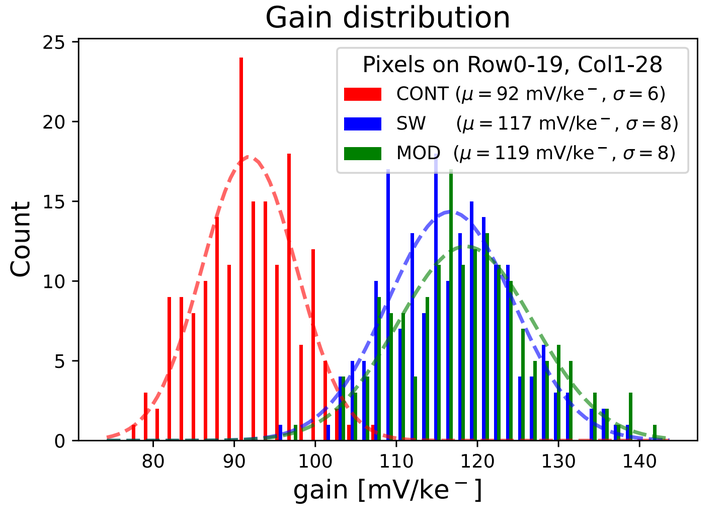
- Agrees with edge-TCT results.

Pixel characterisation

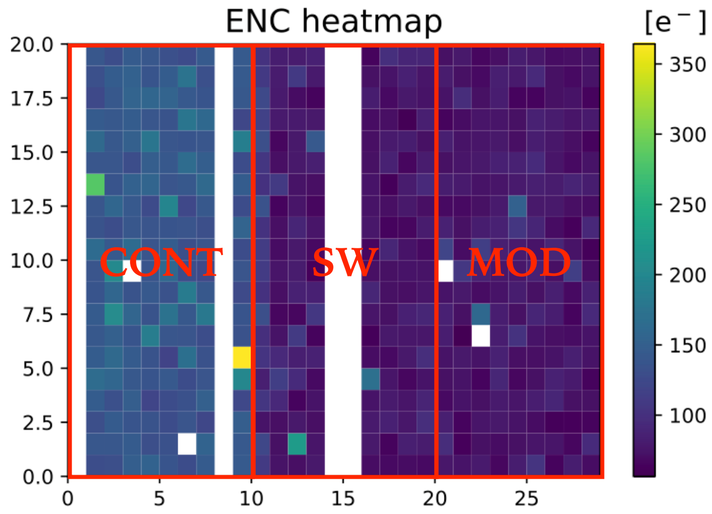
- Pixel performance is measured using S-curve scans.

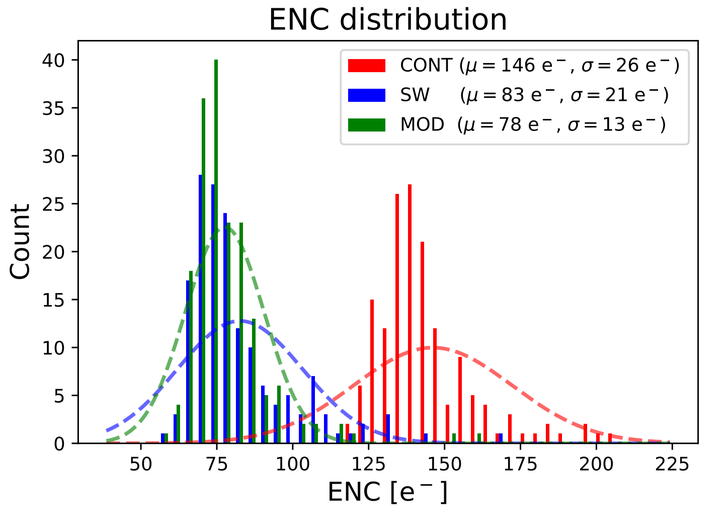
pixel gain





pixel noise

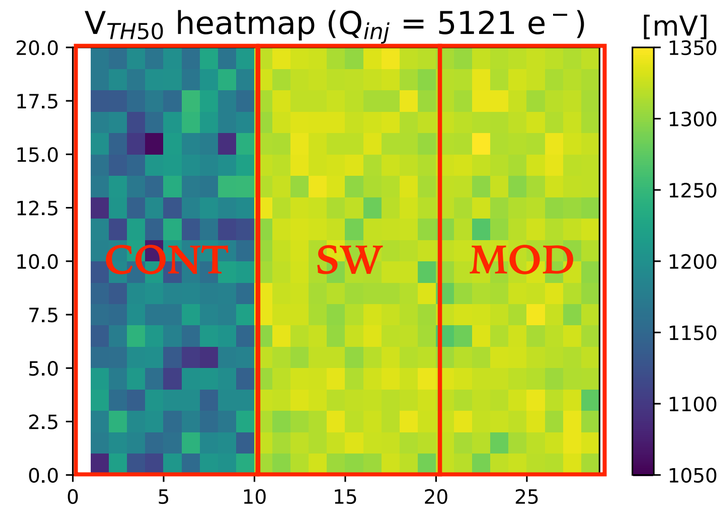


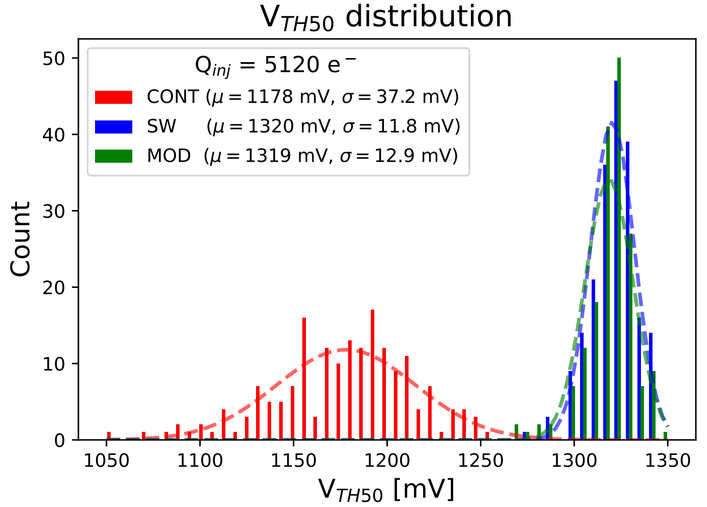


Pixel characterisation

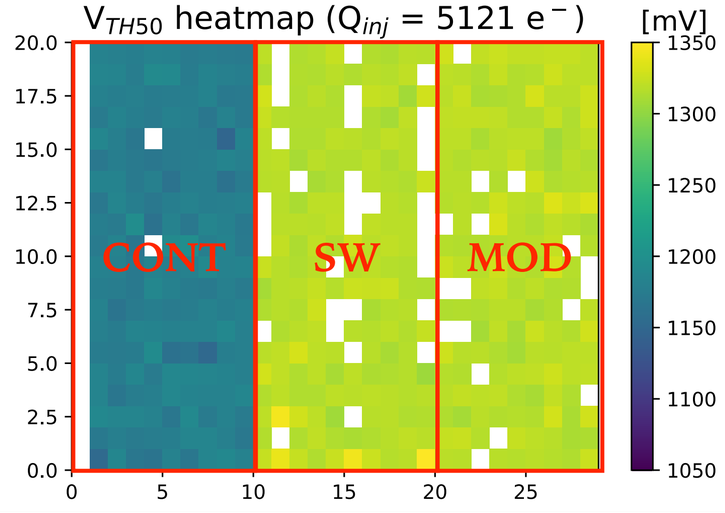
- Threshold before and after trimming:

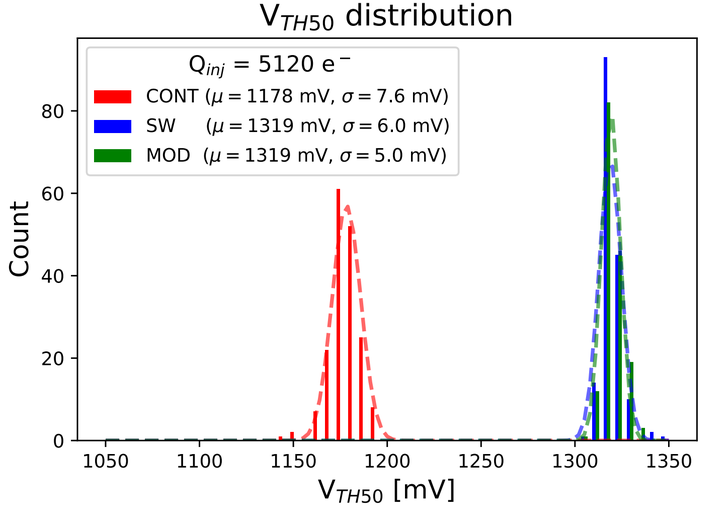
threshold before trimming





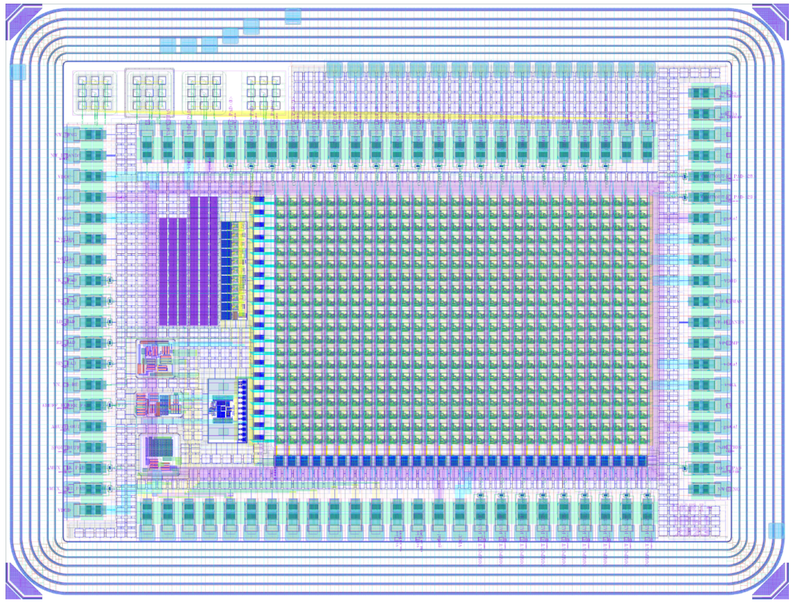
threshold after trimming

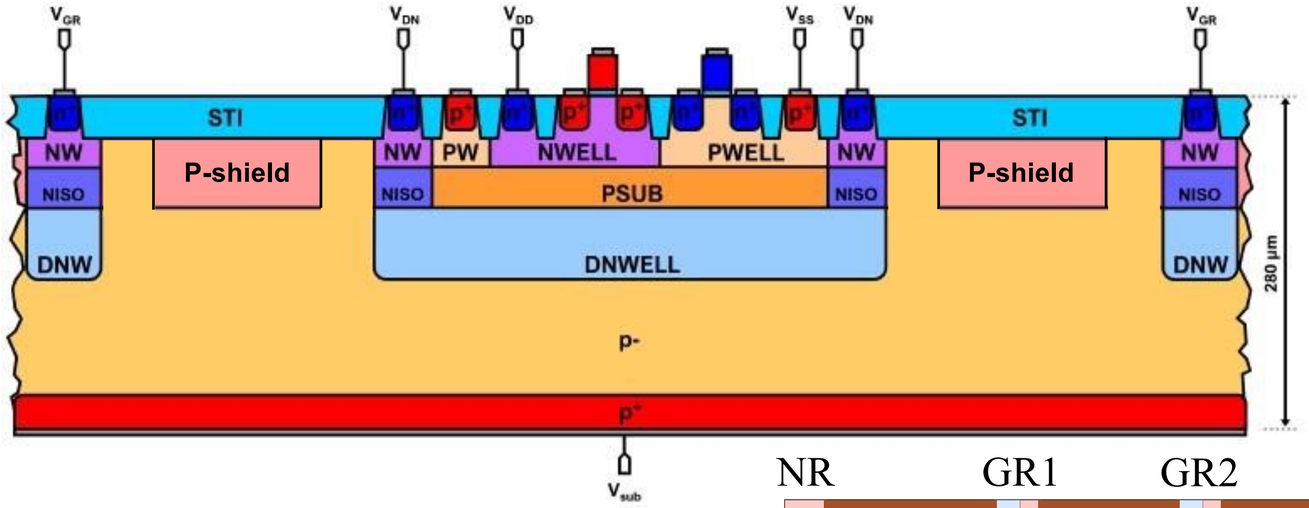


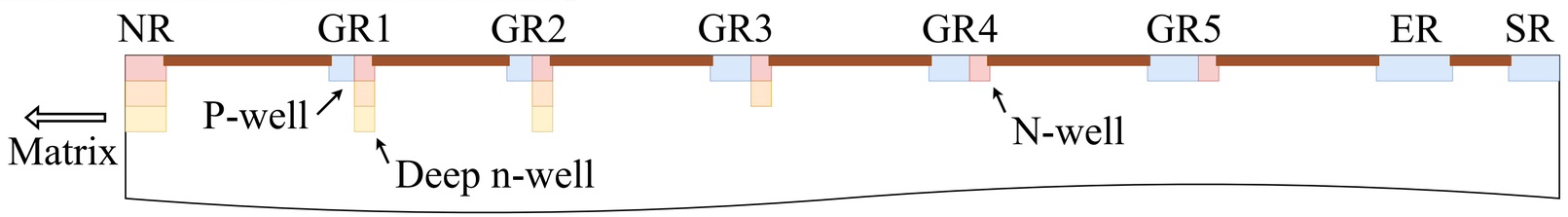


UKRI-MPW1

- Succeeding UKRI-MPW1 is designed.
- Add a customised low-doped shallow p-type layer (P-shield) beneath STI to prevent parasitic channel.
- Use a new chip ring structure for lower leakage.
  - ➤ Guard Rings (GR) have both P-type and N-type wells.
- High voltage can be applied from topside (Seal Ring (SR) and Edge Ring (ER)) or backside.







Conclusion and outlook

- **Conclusions:**
  - ➤ UKRI-MPW0 is a proof-of-concept HV-CMOS chip with backside-only biasing.
  - ➤ Breakdown voltage > 600 V.
  - ➤ After 1e16 n_{eq}/cm^2 neutron irradiation, depletion depth > 50 μm.
  - ➤ pixel performance after irradiation has been evaluated.
  - ➤ In UKRI-MPW1: improve the high leakage current by modifying the chip rings; prevent the channel under STI by adding P-shield.
- **Outlook:**
  - ➤ Evaluate UKRI-MPW0 pixel matrix in testbeam.
  - ➤ UKRI-MPW1 will be delivered in November 2023.