Contribution ID: **162** Type: **Oral**

Lab measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype detector with a large breakdown voltage

Tuesday 3 October 2023 16:00 (20 minutes)

An HV-CMOS (High-Voltage CMOS) prototype detector for particle detection in high energy physics experiments, named UKRI-MPW0, has been developed. This chip implements a novel sensor cross-section optimised for biasing the chip from the backside only and achieves an unprecedented breakdown voltage (> 600 V). With such a high breakdown voltage, UKRI-MPW0 is expected to achieve much improved radiation tolerance. The chip contains test structures for edge-TCT measurements and a matrix of monolithic pixels with integrated readout electronics. The design and detailed lab measurements of its pixel matrix after irradiation is presented in this contribution.

Summary (500 words)

The industry standard High-Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments that have extreme requirements, such as the Mu3e experiment, future upgrades of the Large Hadron Collider (LHC) and the Circular Electron Positron Collider (CEPC). As opposed to traditional hybrid silicon sensors that require bump-bonding assembly, the HV-CMOS pixel sensors integrate sensing elements and readout electronics into single pieces of silicon, thus making this technology efficient in material, production time and cost. The sensor substrate is biased to high voltages, which brings the benefits of fast charge collection by drift and high radiation tolerance up to a few 10^15 1 MeV neq/cm^2.

To meet the needs of future experiments, for example in HL-LHC: single point resolution (25 × 50 μm^2), time resolution (50 ps) and radiation tolerance (5 × 10^15 neq/cm^2), the HV-CMOS pixel sensor performance needs to be further improved. The Liverpool HV-CMOS group has developed an HV-CMOS prototype chip, named UKRI-MPW0, which aims at addressing some of these challenges. This chip is developed using the 150 nm HV-CMOS process from LFoundry. It implements a novel sensor cross-section with no substrate contacts on its top-side for backside-only biasing. I-V measurements have shown the chip is able to sustain unprecedented high bias voltages (> 600 V), thus promising a large improvement in radiation tolerance. A pixel matrix of 20 rows and 29 columns (pixel size of 60 × 60 μm^2) and several test structures are included in the chip.

UKRI-MPW0 chips are fabricated on two high-resistivity (1.9 kΩ·cm) wafers which are thinned to 280 μm and backside processed using different methods: one with Beam-Line Ion Implantation (BLII) and Rapid Thermal Annealing (RTA), and the other one with Plasma-Immersion Ion Implantation (PIII) and UV laser annealing. Samples have been irradiated to different neutron fluences up to 1 × 10^16 neq/cm^2.

This contribution covers the design details and evaluation of UKRI-MPW0 before and after irradiation, including IV, edge-TCT measurements and the characterisation of its pixel matrix. Initial measured results show the chip can be biased to 600 V and 400 V before and after irradiation (1 × 10^16 neq/cmv2) with leakage currents of ~1 μA and ~100 μA. The chip substrate of samples irradiated to fluences < 1 × 10^14 neq/cm^2 is fully depleted with bias voltages larger than 300 V. A depletion depth of > 50 μm can be achieved in samples irradiated to the fluence of 1 × 10^16 neq/cm^2. Pixels have Equivalent Noise Charge (ENC) < 100 e- and gain > 100 mV/ke- before irradiation. Figures showing the listed performance are included in the attachment. The performance of the active pixel matrix after irradiation will be presented.

A succeeding chip, UKRI-MPW1, has been designed and submitted for fabrication, which includes improvements to reduce the leakage current and eliminate parasitic channels between pixels.

Author: ZHANG, Chenfan (University of Liverpool (GB))

Co-authors: Mr WADE, Benjamin (University of Liverpool (GB)); VILELLA FIGUERAS, Eva (University of Liverpool (GB)); HAMMERICH, Jan Patrick (University of Liverpool (GB)); POWELL, Samuel (University of Liverpool (GB))

Presenter: ZHANG, Chenfan (University of Liverpool (GB))

Session Classification: ASIC

Track Classification: ASIC